APLUS

APU8051/8052

8 - Bit Micro-controller

with 4/8KB ROM embedded

Product List

APU8051, 25 MHz 4KB internal ROM MCU
APU8052, 25 MHz 8KB internal ROM MCU

Description

The APU8051/8052 series product is an 8 - bit single chip microcontroller with 4/8 KB ROM and 128/256 bytes RAM embedded.
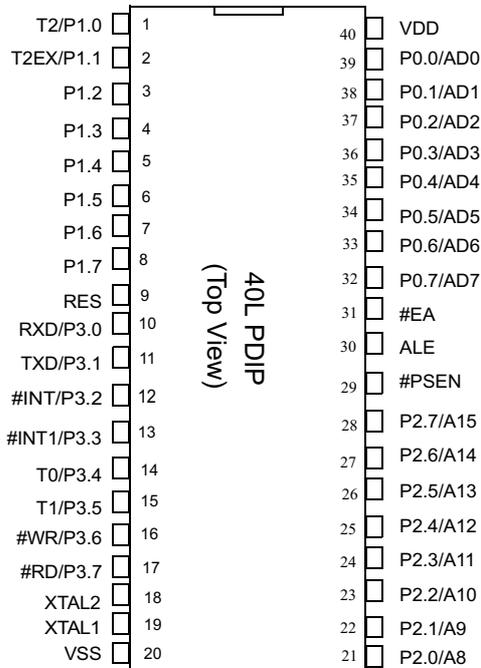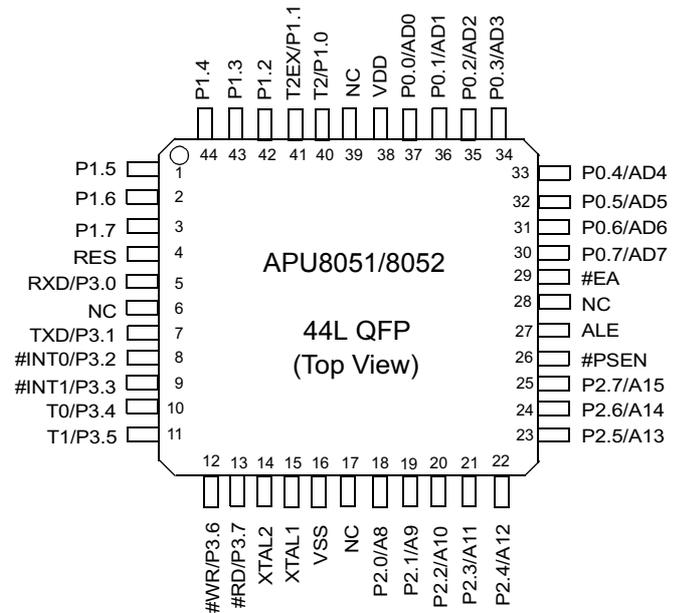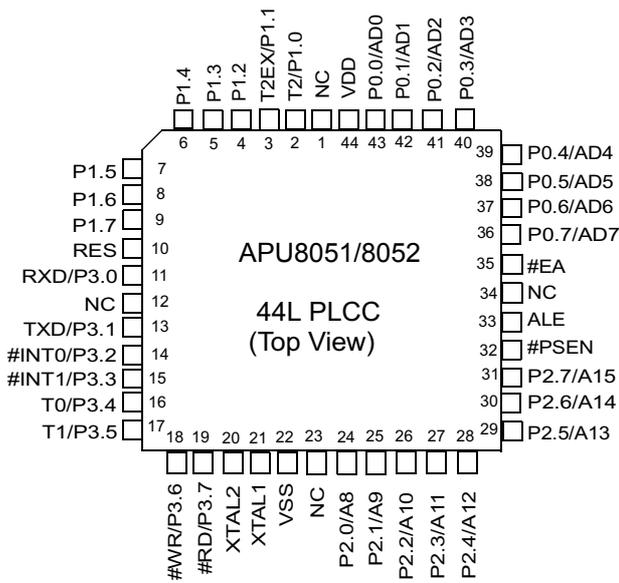
It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 64 KB external memory either for program or for data or mixed.

A serial input / output port is provided for I/O expansion, inter-processor communications, and full duplex UART.
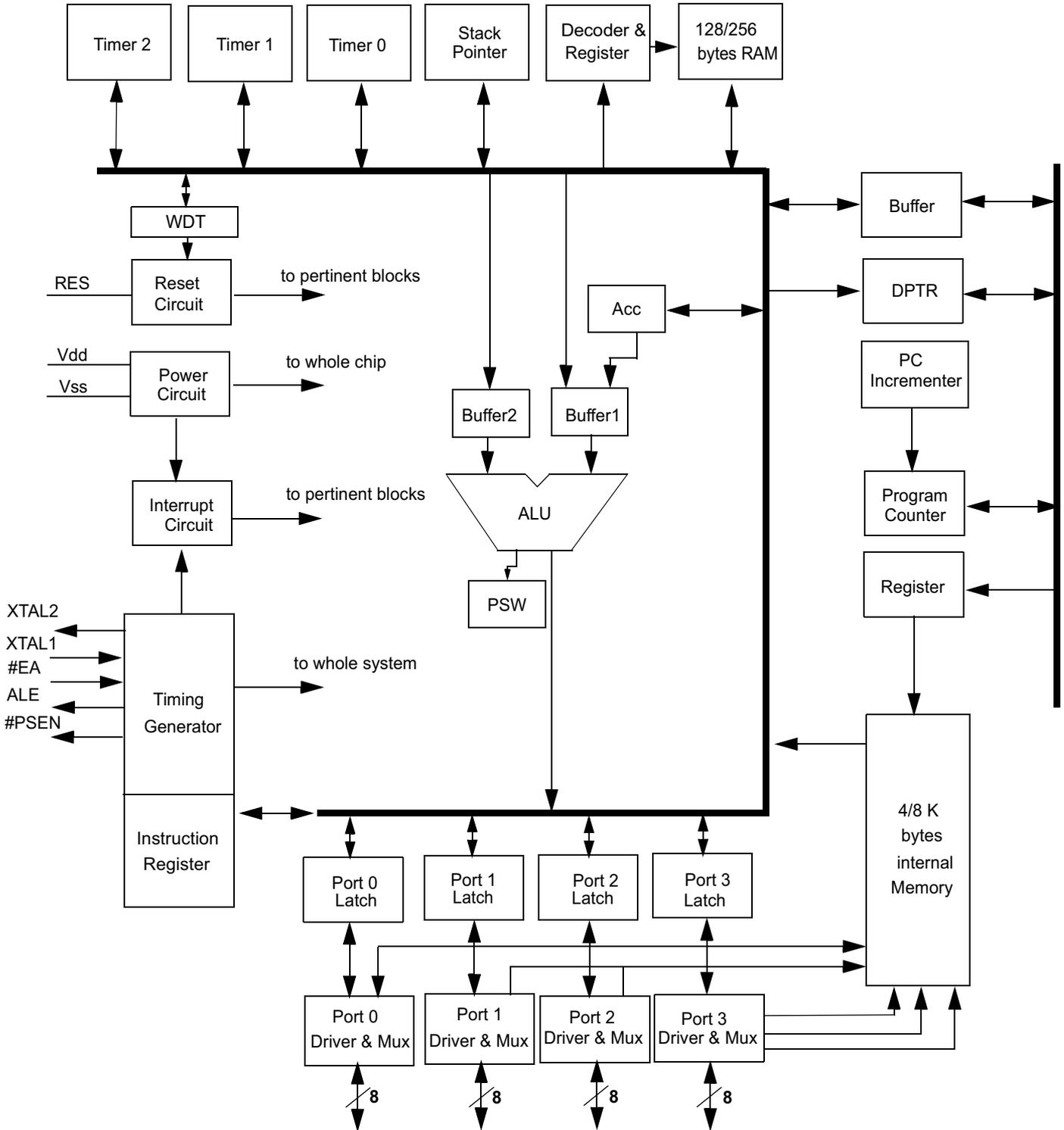
Features

- Working voltage:4.5V through 5.5V

- 12 clocks per machine cycle
- 64K byte external memory space
- 4/8 KB internal program memory
- 128/256 bytes data RAM
- 2/3 16 bit timers/counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instruction
- Page free jumps
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
  Idle mode and power down mode
- Working at 25 MHz clock
- One watch dog timer (WDT)
- Low EMI (inhibit ALE)

Ping Configration :

APU8051/8052
44L PLCC
(Top View)

APU8051/8052
44L QFP
(Top View)

APU8051/8052
40L PDIP
(Top View)

T2/P1.0 1	40 VDD
T2EX/P1.1 2	39 P0.0/AD0
P1.2 3	38 P0.1/AD1
P1.3 4	37 P0.2/AD2
P1.4 5	36 P0.3/AD3
P1.5 6	35 P0.4/AD4
P1.6 7	34 P0.5/AD5
P1.7 8	33 P0.6/AD6
RES 9	32 P0.7/AD7
RXD/P3.0 10	31 #EA
TXD/P3.1 11	30 ALE
#INT/P3.2 12	29 #PSEN
#INT1/P3.3 13	28 P2.7/A15
T0/P3.4 14	27 P2.6/A14
T1/P3.5 15	26 P2.5/A13
#WR/P3.6 16	25 P2.4/A12
#RD/P3.7 17	24 P2.3/A11
XTAL2 18	23 P2.2/A10
XTAL1 19	22 P2.1/A9
VSS 20	21 P2.0/A8

Block Diagram

Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	T2/P1.0		i/o	bit 0 of port 1 & timer 2
2	41	3	T2EX/P1.1		i/o	bit 1 of port 1 & timer control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	RXD/P3.0		i/o	bit 0 of port 3 & Receive data
11	7	13	TXD/P3.1		i/o	bit 1 of port 3 & Transmit data
12	8	14	#INT0/P3.2	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	#INT1/P3.3	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	T0/P3.4		i/o	bit 4 of port 3 & Timer 0
15	11	17	T1/P3.5		i/o	bit 5 of port 3 & Timer 1
16	12	18	#WR/P3.6	L/ -	i/o	bit 6 of port 3 & ext. memory write
17	13	19	#RD/P3.7	L/ -	i/o	bit 7 of port 3 & ext. memory read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc

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SFR Memory MAP

	col0	col1	col2	col3	col4	col5	col6	col7	
$F8									$FF
$F0	B								$F7
$E8									$EF
$E0	ACC								$E7
$D8									$DF
$D0	PSW								$D7
$C8	T2CON		RC2H	RC2L	TL2	TH2			$CF
$C0									$C7
$B8	IP							**SCONF**	$BF
$B0	P3								$B7
$A8	IE								$AF
$A0	P2								$A7
$98	SCON	SBUF						**WDTC**	$9F
$90	P1								$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH	(Reserved)			PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for APU8051/8052

Extension Function Description

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate a reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 80C52. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The **APU8051/8052** WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDT. After WDTE set to 1, The 16-bit counter starts to count with the selected time base source clock which set by PS2 ~ PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when **APU8051/8052** been reset, either hardware rest or WDT reset.

To reset the WDT is done by setting 1 to the bit 5 (CLEAR) of WDT. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

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Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

WDTE	0	CLEAR	0	0	PS2	PS1	PS0
0	0	0	0	0	0	0	0

Reset value

MSB   LSB

WDTE : Watch Dog Timer enable bit

CLEAR : Watch Dog Timer reset bit

PS2 ~ PS0 : clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, $BF)

WDR	R	R	R	R	R	R	ALEI
0	0	0	0	0	0	0	0

Reset value

MSB   LSB

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1

ALEI : ALE output inhibit bit, to reduce EMI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened.

Reduce EMI Function

The **APU8051/8052** allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.
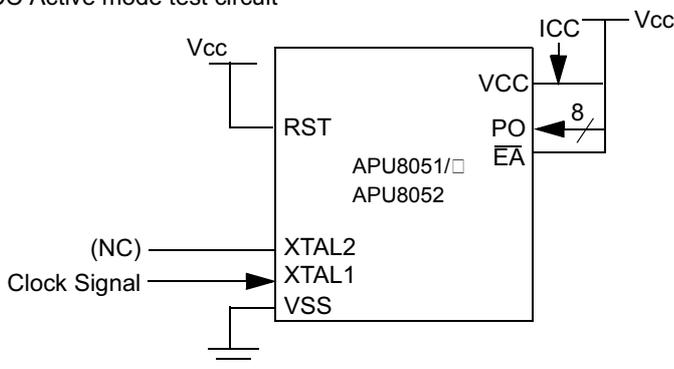
Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Ambient temperature under bias	0	25	70	C	
VCC5	Supply voltage	4.5	5.0	5.5	V	APU8051/8052
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	APU8051/8052
Fosc 25		3.0	25	25	MHz	APU8051/8052
Fosc 40		3.0	40	40	MHz	APU8051/8052

DC Characteristics

(16/25/40MHz, typical operating conditions, valid for APU8051/8052 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		15	mA	Active mode, 40MHz
				10	mA	Active mode, 25MHz
				7	mA	Active mode, 16MHz
				10	mA	Idle mode, 40MHz
				7	mA	Idle mode, 25MHz
				4.5	mA	Idle mode, 16MHz
				10	uA	Power down mode

ICC Active mode test circuit

ICC Idle mode test circuit
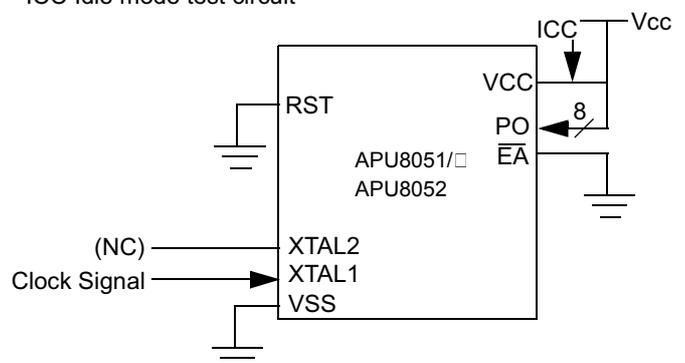
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AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	
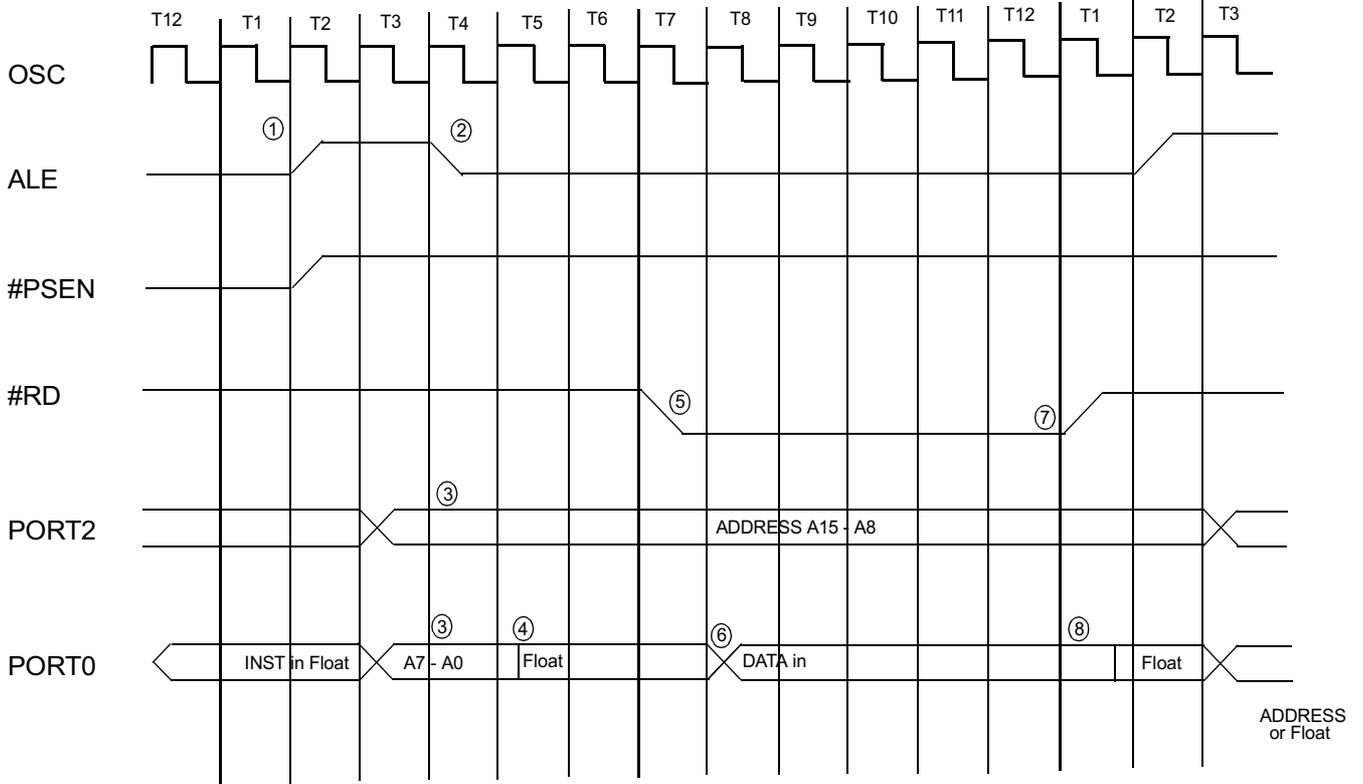
Data Memory Read Cycle Timing
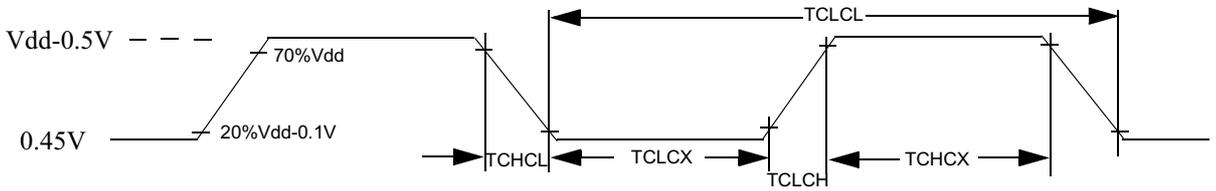

Program Memory Read Cycle Timing
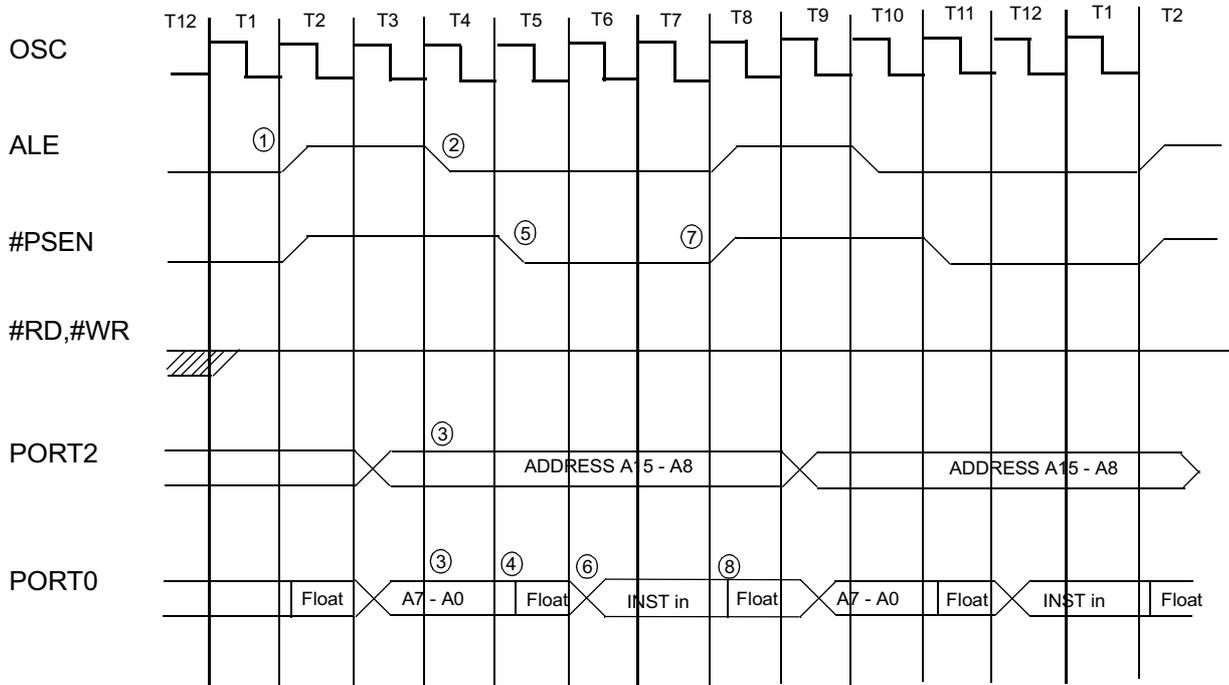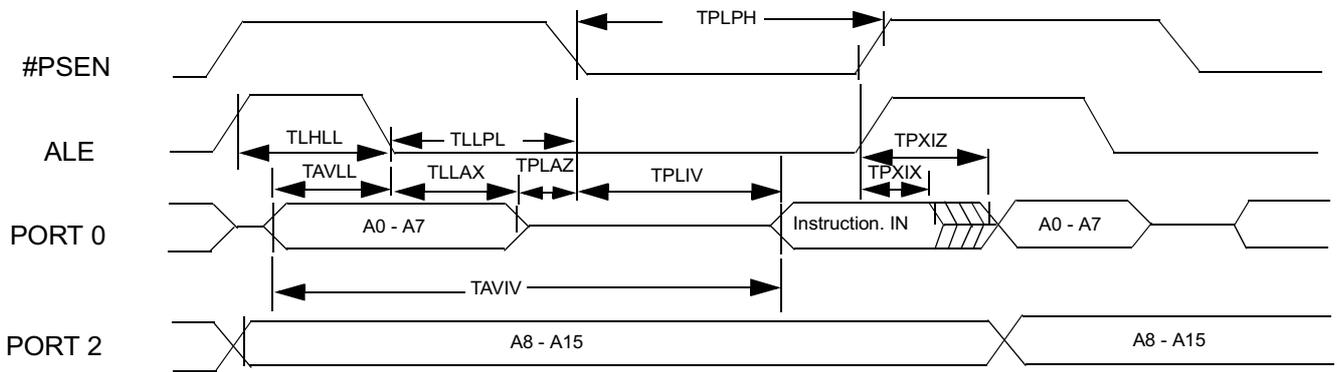
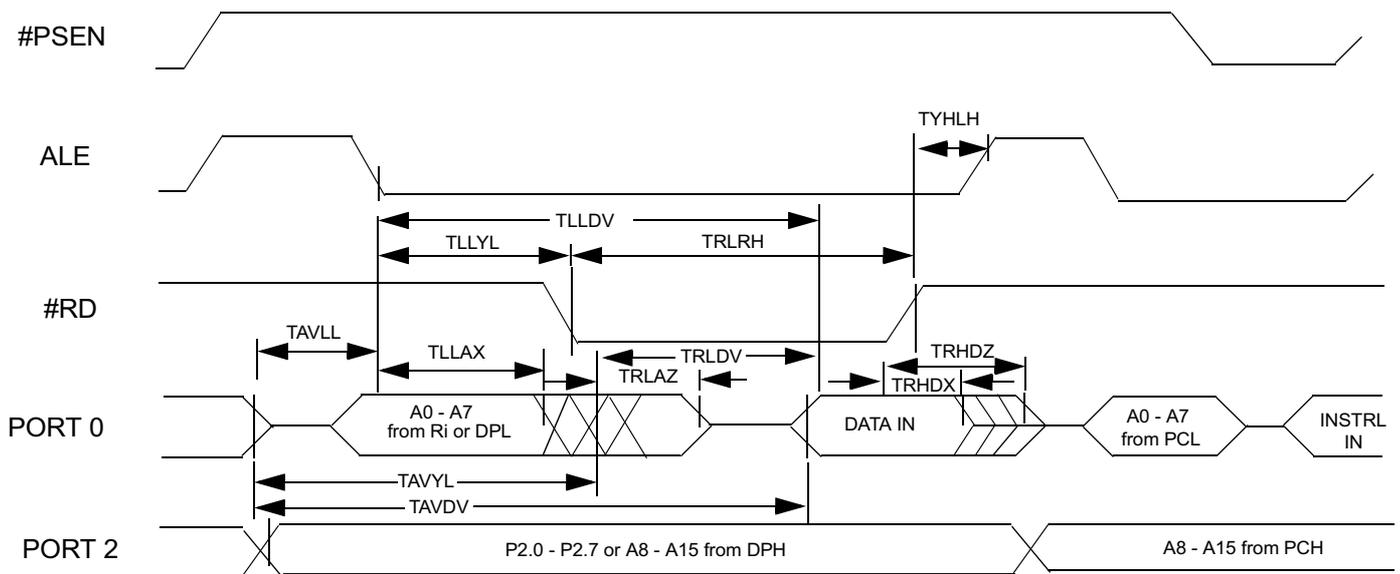## Data Memory Write Cycle Timing
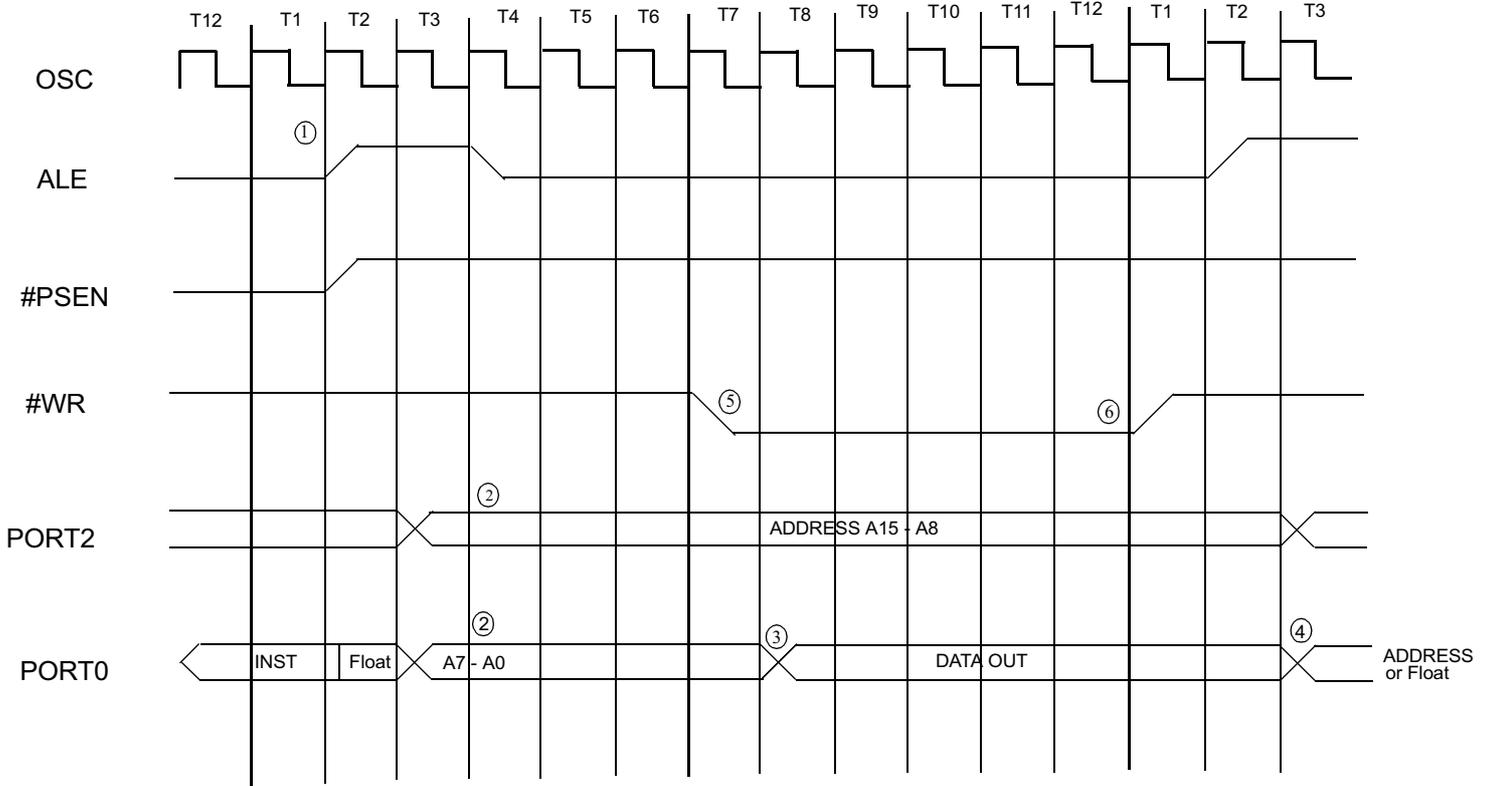
I/O Ports Timing
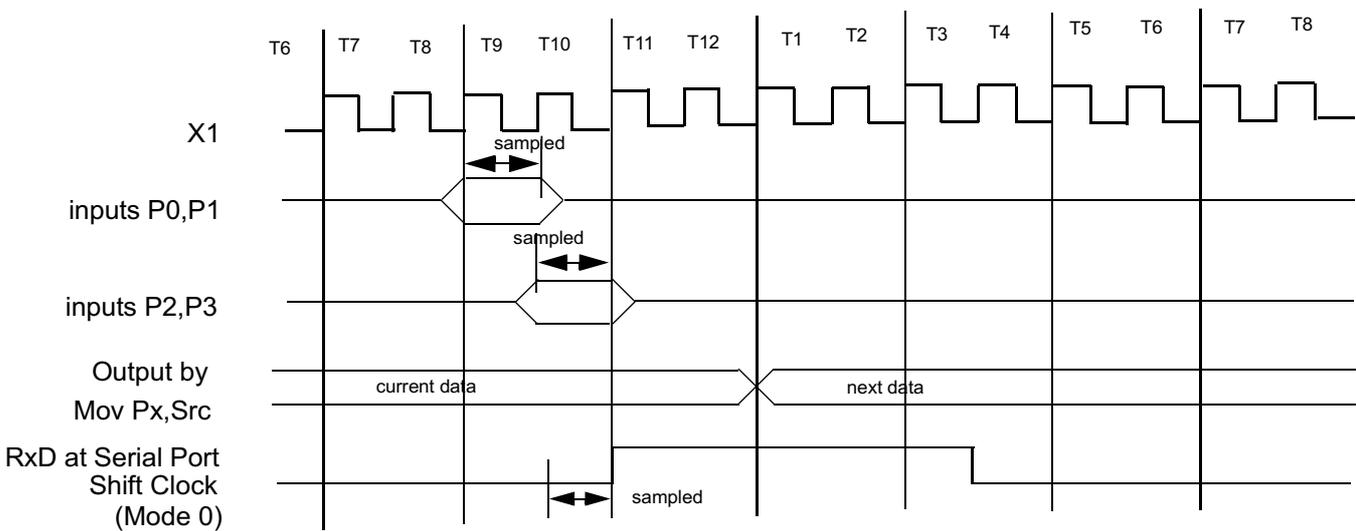
Timing Critical, Requirement of External Clock   (Vss=0.0V is assumed)

Tm.I   External Program Memory Read Cycle
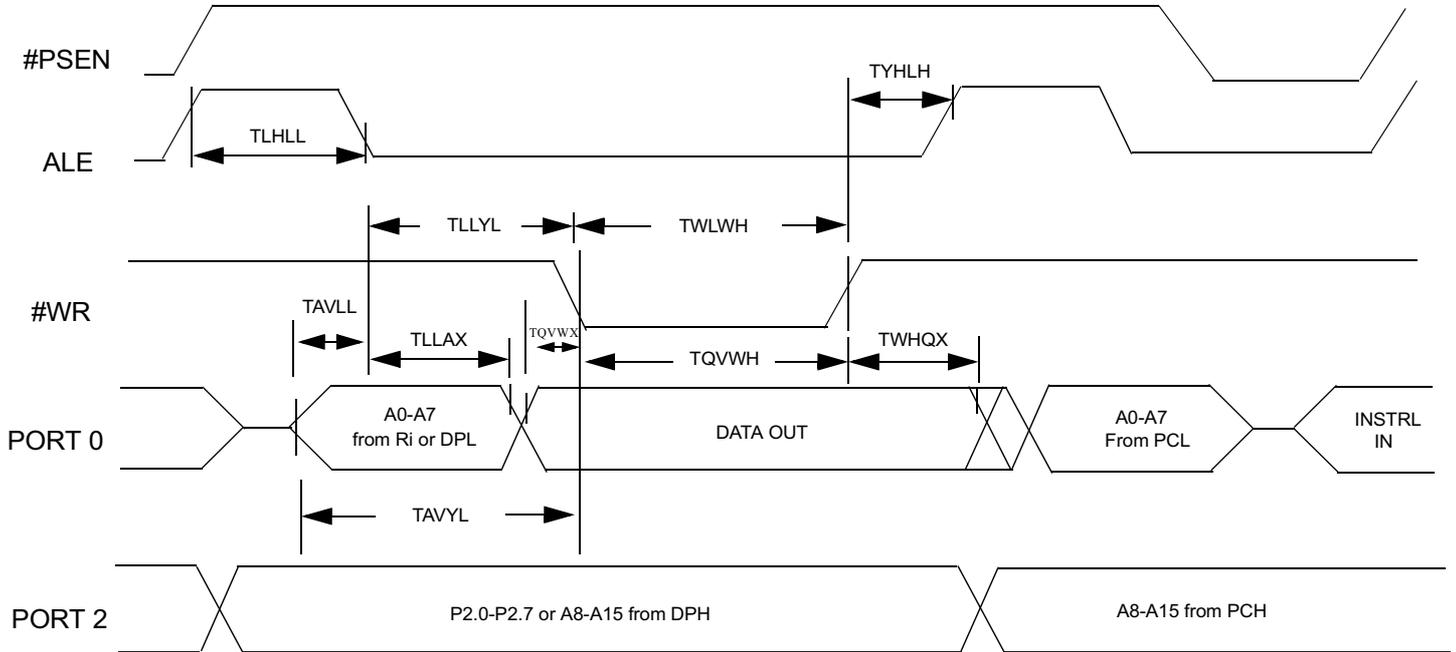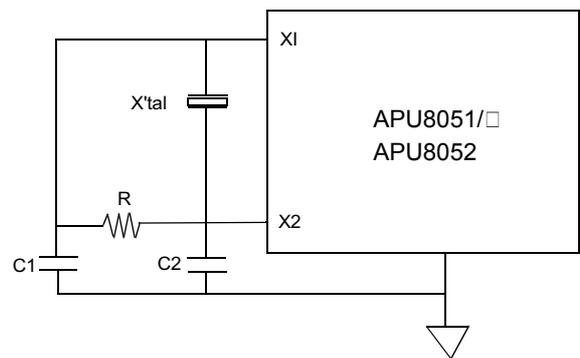

Tm.II   External Data Memory Read Cycle

Tm.III   External Data Memory Write Cycle

Application Reference

Valid for **APU8051/8052**			
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 p	30 p	30 p	30 p
C2	30 p	30 p	30 p	30 p
R	open	open	open	open

X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	10 pF	5 pF
C2	30 pF	15 pF	10 pF	5 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

NOTE: Oscillation circuit may differs with different crystal or ceramic
resonator in higher oscillation frequency which was due to each
crystal or ceramic resonator has its own characteristics.
User should check with the crystal or ceramic resonator manufacturer
for appropriate value of external components.
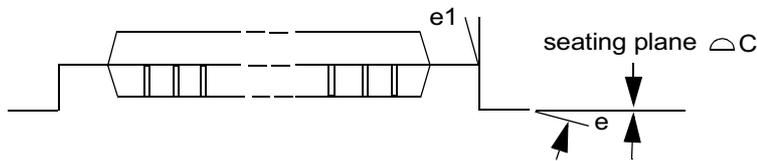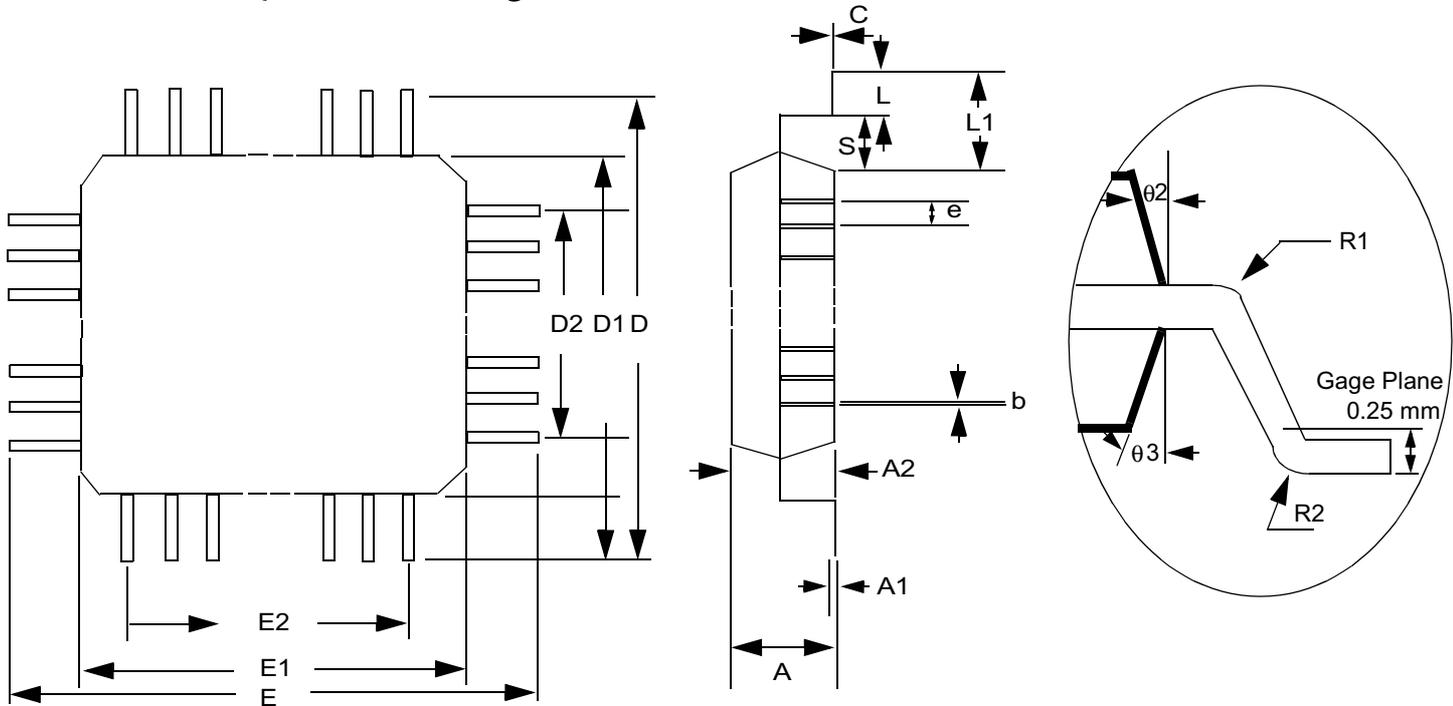
40L 600mil PDIP Information
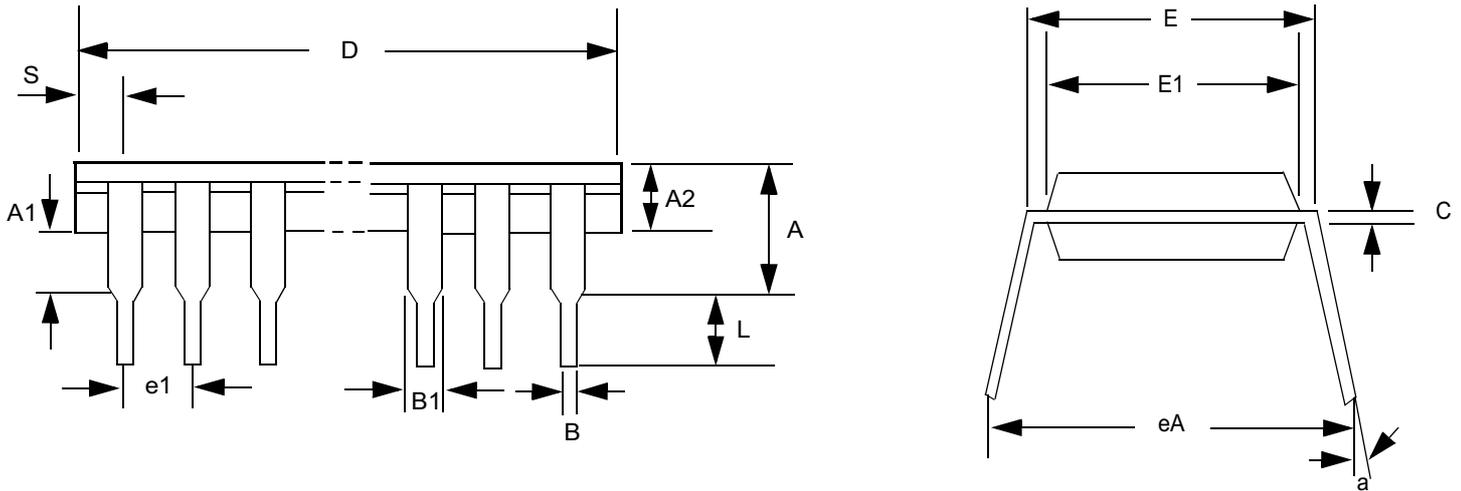
Note:
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0°/ 15˚	0°/ 15˚
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

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44L Plastic Quad Flat Package

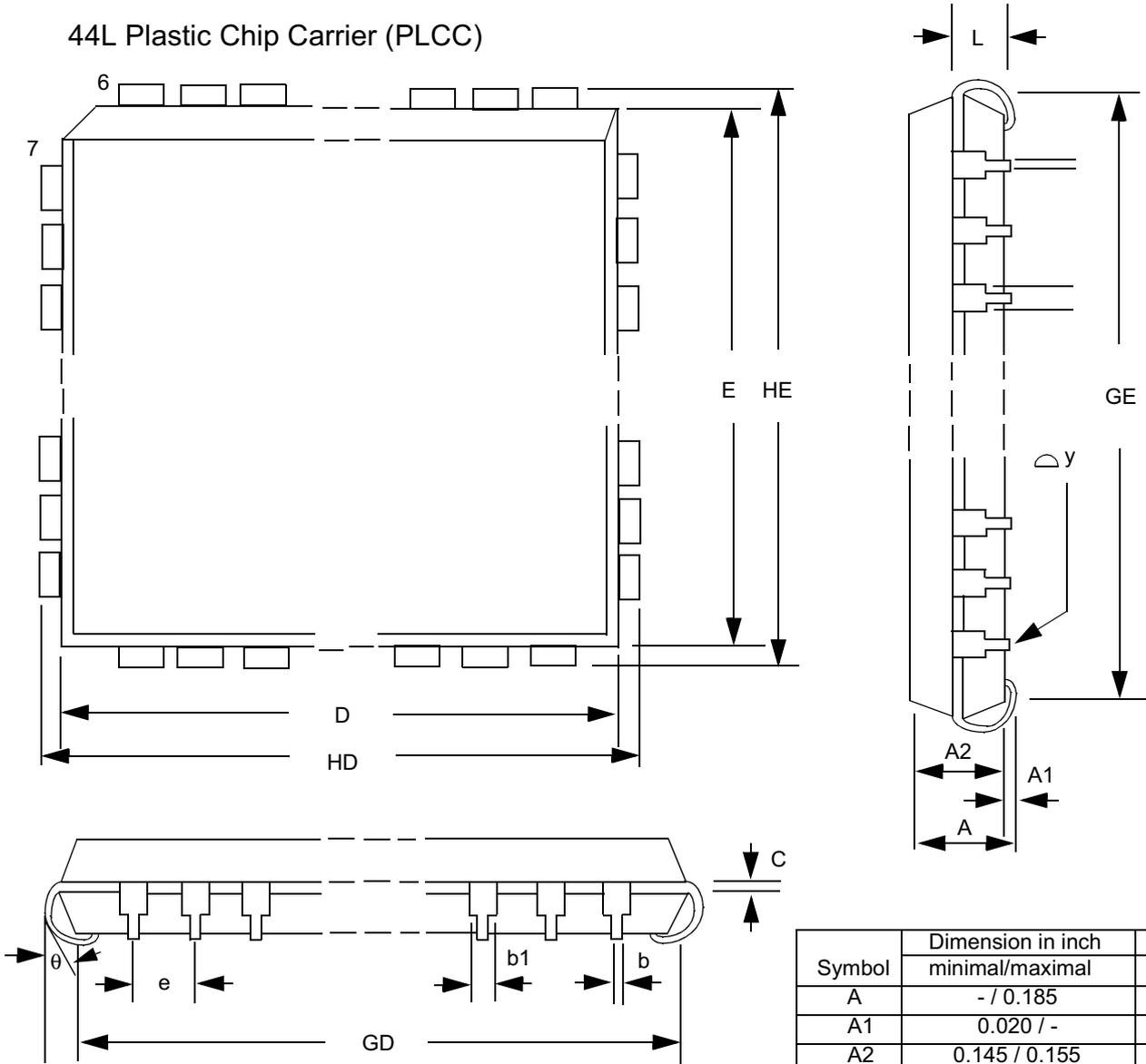| Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌒C	0.004	0.10

Note:

Dimension D1 and E1 do not include mold protrusion.

Allowance protrusion is 0.25mm per side.

Dimension D1 and E1 do include mold mismatch

and are determined datum plane.

Dimension b does not include dambar protrusion.

Allowance dambar protrusion shall be 0.08 mm total

in excess of the b dimension at maximum material

condition. Dambar cannot be located on the lower

radius or the lead foot.

44L Plastic Chip Carrier (PLCC)

Note:

1. Dimension D & E does not include interlead flash.
2. Dimension b1 does not include dambar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌒y	/	/

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