Document Title

8M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Jul. 20th, 2010	Preliminary
0.1	Revise MRS Code for Array Refresh Area	Oct. 12th, 2010	Preliminary

8M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 8M x 16
- Power Supply Voltage : 1.7~1.95V
- Three state output and TTL Compatible
- Separated I/O power(VCCQ) & Core power(VCC)
- Operating Temperature Ranges:
  - Special (-10'C to +60'C)
  - Commercial (0'C to +70'C)
  - Extended (-25'C to +85'C)
  - Industrial (-40'C to +85'C)

- Package Type : 54-FBGA-6.00x8.00 mm²
  - FMP1216ACx-HxxX : Pb-Free & Halogen Free
- Low Power & Page Modes
  - FMP1216AC1 : support the PASR/DPD function
  - FMP1216AC2 : support the Direct DPD function
  - FMP1216AC4 : support the PASR/DPD/PAGE function
  - FMP1216AC5 : support the Direct DPD/PAGE function
- Page read/write operation by 16 words
  - (FMP1216AC4, FMP1216AC5)
- DPD mode by using MRS only
  - (FMP1216AC1, FMP1216AC4)
- Direct DPD mode when /ZZ goes low
  - (FMP1216AC2, FMP1216AC5)

PRODUCT FAMILY

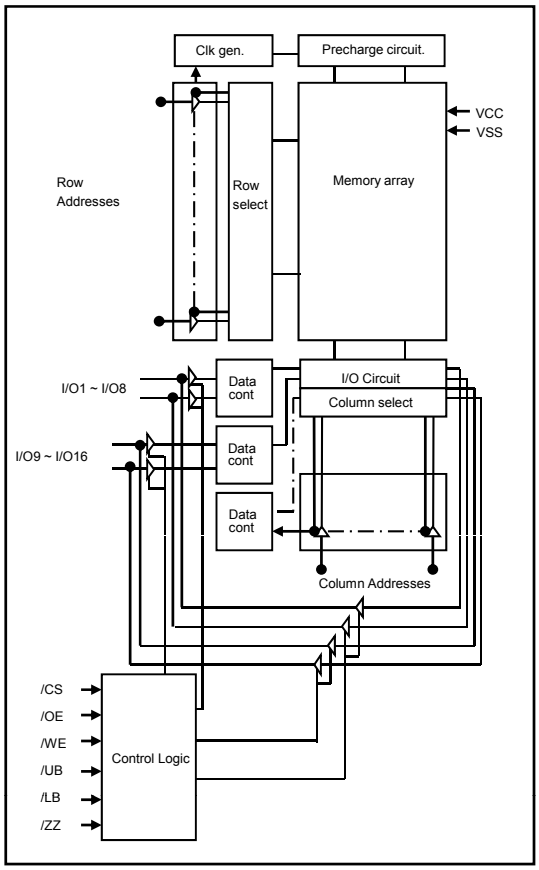
Product Family	Operating Voltage (V)			Speed	Power Dissipation					
					ICC1		ICC2		ISB1 (CMOS Standby Current)	
					f = 1MHz		f = fmax			
	Min.	Typ.	Max.		Typ.	Max.	Typ.	Max.	Typ.	Max.
FMP1216ACx-H70E	1.7	1.8	1.95	70ns	1.5mA	3mA	12mA	25mA	**180uA**	**200uA**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (typ) and T_A = 25C.
2. H=FBGA(Pb-Free & Halogen Free), W=WAFER
3. Operating Temperature Range: S (-10'C~60'C), C(0'C~70'C), E(-25'C~85'C), I (-40'C~85'C)

PIN DESCRIPTION

Name	Function	Name	Function
/ZZ	Low Power Modes	VCC	Core Power
/CS	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A22	Address Inputs	/LB	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Part Name	Function
FMP1216ACx-H70E	70ns, VCC=1.8V, VCCQ=1.8V

1. H=FBGA(Pb-Free & Halogen Free), W=WAFER
2. Operating Temperature Range: S (-10'C~60'C), C(0'C~70'C), E(-25'C~85'C), I (-40'C~85'C)

FUNCTIONAL DESCRIPTION

/CS	/ZZ	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Direct DPD[2]
H	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Low Power Modes[3]
L	H	H	H	X[1]	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	L	H	H	H	High-Z	High-Z	Output Disabled	Active
				L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X[1]	L	H	H	High-Z	High-Z	Write-abort[4]	Active
				L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)
2. In case of FMP1216AC2 & FMP1216AC5 product
3. In case of FMP1216AC1 & FMP1216AC4 product

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 2.45	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-55 to 150	'C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	FMP1216ACx		Unit
		Min	Max	
Supply voltage	V_{CC}	1.7	1.95	V
I/O operating voltage (VCCQ ≤ VCC)	V_{CCQ}	1.7	1.95	V
Ground	V_{SS}	0	0	V
Input high voltage	V_{IH}	0.8VCCQ	VCC+0.2[1]	V
Input low voltage	VIL	-0.2[2]	0.2VCCQ	V

Note :
1. Overshoot : Vcc+1.0V in case of pulse width≤20ns.
2. Undershoot : -1.0V in case of pulse width≤20ns.
3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz , T_A=25'C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

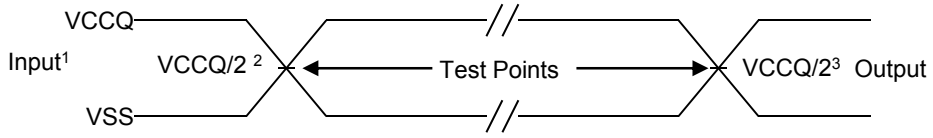
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	-	1	uA
Output leakage current	I_{LO}	/CS=V_{IH}, /ZZ=V_{IH}, /OE=V_{IH} or /WE=VIL, V_{IO}=V_{SS} to V_{CC}	-1	-	1	uA
Average operating current	I_{CC1}	Cycle time=1us, 100%duty, I_{IO}=0mA, /CS≤0.2V, /ZZ=V_{IH}, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, /CS=VIL, /ZZ=V_{IH}, V_{IN}=VIL or V_{IH}	-	-	25	mA
Output low voltage	V_{OL}	I_{OL}=0.5mA			0.2VCCQ	V
Output high voltage	V_{OH}	I_{OH}=-0.5mA	0.8VCCQ			V
Standby Current(TTL)	I_{SB}	/CS=V_{IH}, /ZZ=V_{IH}, Other inputs=V_{IH} or VIL	-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	/CS≥V_{CC}-0.2V, /ZZ≥V_{CC}-0.2V, Other inputs=0~V_{CC}	-	-	200	uA
Low Power Modes	I_{SB0}	/ZZ≤0.2V, Other inputs=0~V_{CC}, No refresh(DPD)	-	-	10	uA
	I_{SB0a}	/ZZ≤0.2V, Other inputs=0~V_{CC}, ¼ refresh area selection	-	-	155	uA
	I_{SB0b}	/ZZ≤0.2V, Other inputs=0~V_{CC}, ½ refresh area selection	-	-	170	uA
	I_{SB0c}	/ZZ≤0.2V, Other inputs=0~V_{CC}, All refresh area selection	-	-	200	uA

Operating Range

Device	Range	Ambient Temperature	VCC	VCCQ
FMP1216ACx-XxxS	Special	-10℃ to +60℃	1.7V to 1.95V	1.7V to VCC
FMP1216ACx-XxxC	Commercial	0℃ to +70℃		
FMP1216ACx-XxxE	Extended	-25℃ to +85℃		
FMP1216ACx-XxxI	Industrial	-40℃ to +85℃		

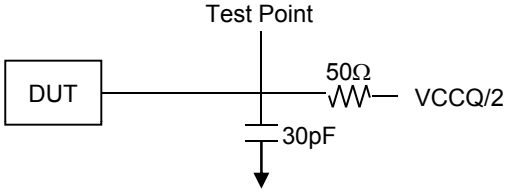
AC Input/Output Reference Waveform



NOTE:

1. AC test inputs are driven at VCCQ for a logic 1 and VSS for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at VCCQ/2.
3. Output timing ends at VCCQ/2.

AC Output Load Circuit



AC CHARACTERISTICS(VCC=1.7V~1.95V)

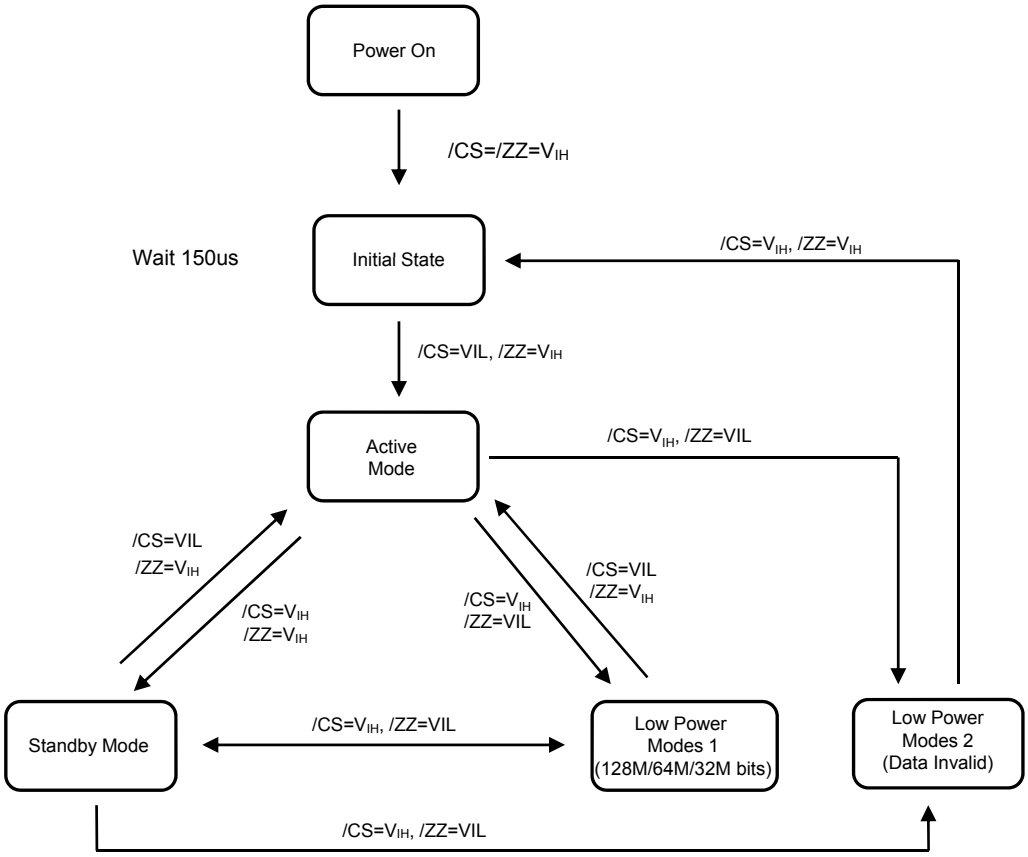
Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	tRC	70	20k	ns
	Address Access Time	tAA	-	70	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	25	ns
	/UB, /LB Access Time	tBA	-	25	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	ns
	Output Hold from Address Change	tOH	5	-	ns
Write	Write Cycle Time	tWC	70	20k	ns
	Chip Select to End of Write	tCW	60	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	/UB, /LB Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	50	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	5	ns
	Data to Write Time Overlap	tDW	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns
	End Write to Output Low-Z	tOW	5	-	ns
Page	Page Mode Cycle Time	tPC	25	-	ns
	Page Mode Address Access Time	tPAA	-	25	ns
	Maximum Cycle Time	tMRC	-	20k	ns
/CS High Pulse Width		tCP	10	-	ns

1. /CS High Pulse Width is defined by /CS.

Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 150us with /CS=/ZZ=VIH

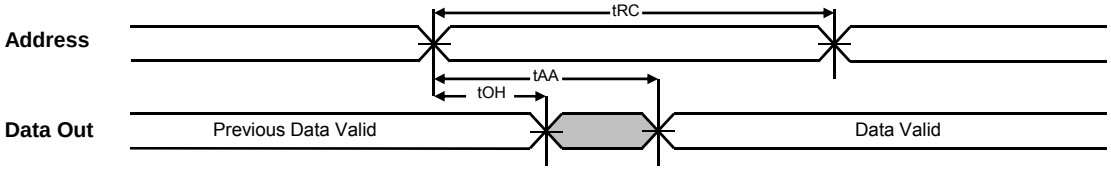
Standby Mode State machines



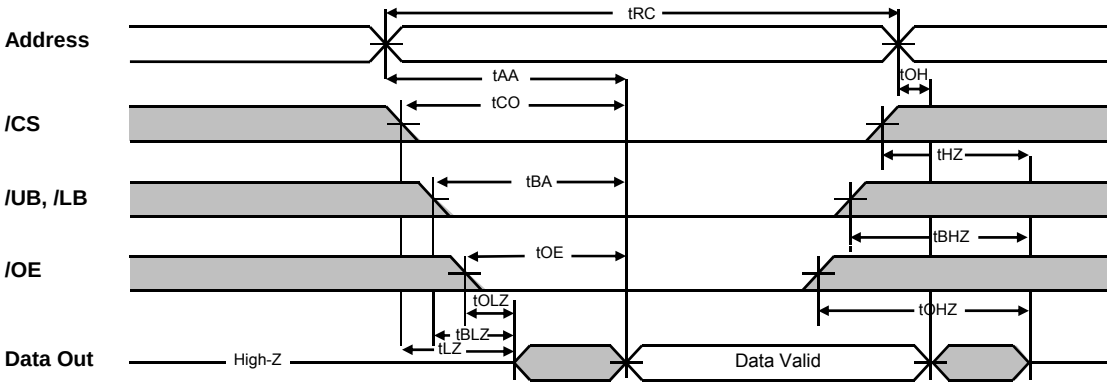
Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	200 (ISB1)	0
Low Power Modes	Invalid	10 (ISB0)	150
	¼ valid	155 (ISB0a)	0
	½ valid	170 (ISB0b)	0
	valid	200 (ISB0c)	0

READ CYCLE (1) (Address controlled,/CS=/OE=VIL, /ZZ=/WE=VIH, /UB or/and /LB=VIL)

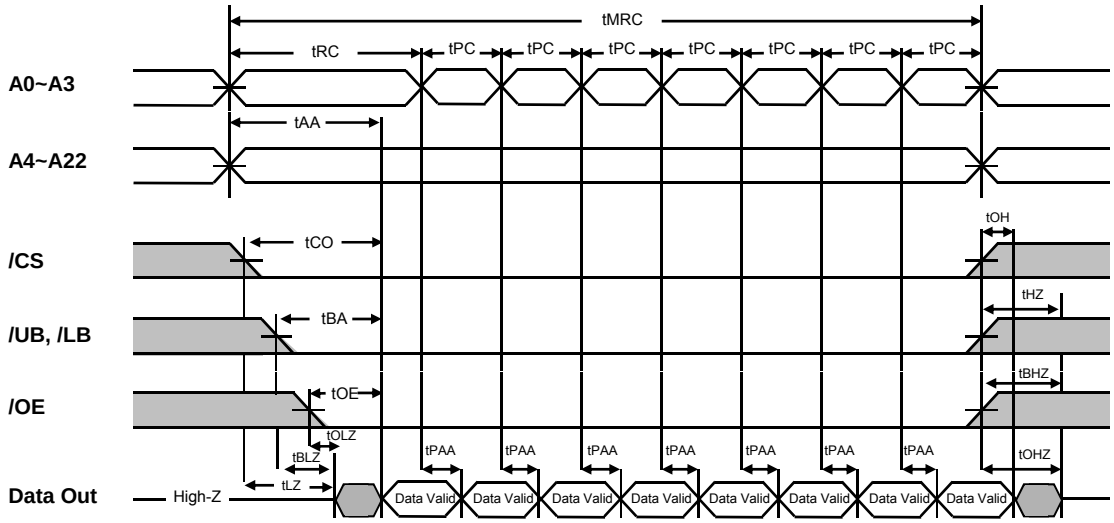


READ CYCLE (2) (/ZZ=/WE=VIH)



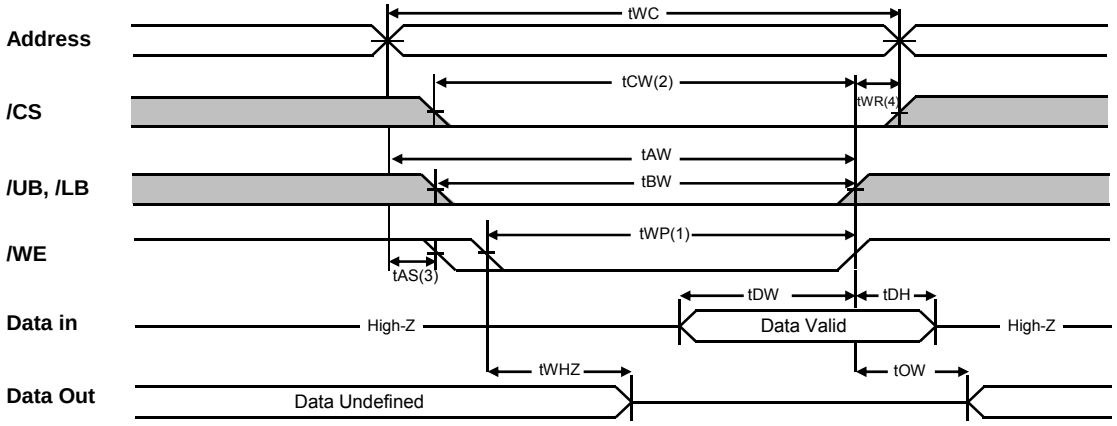
1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

PAGE READ CYCLE (/ZZ=/WE=VIH, 16 words access)

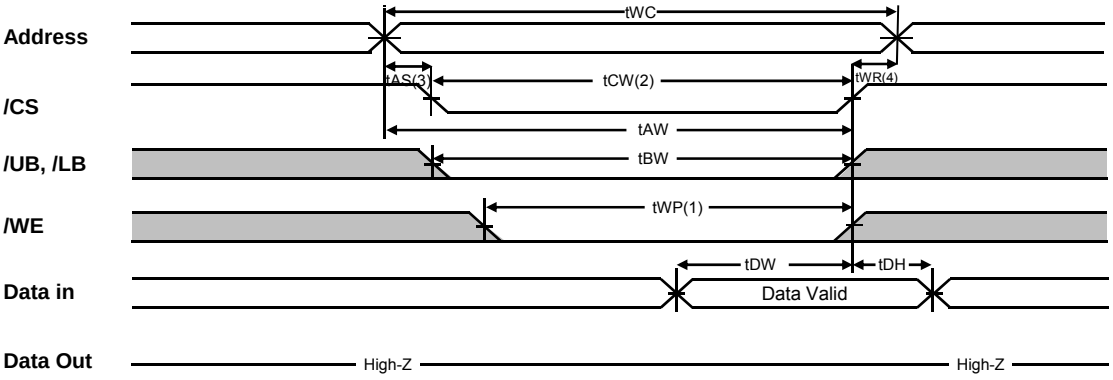


1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.
4. In case page address skew is over 3ns, tPAA will be out of spec.

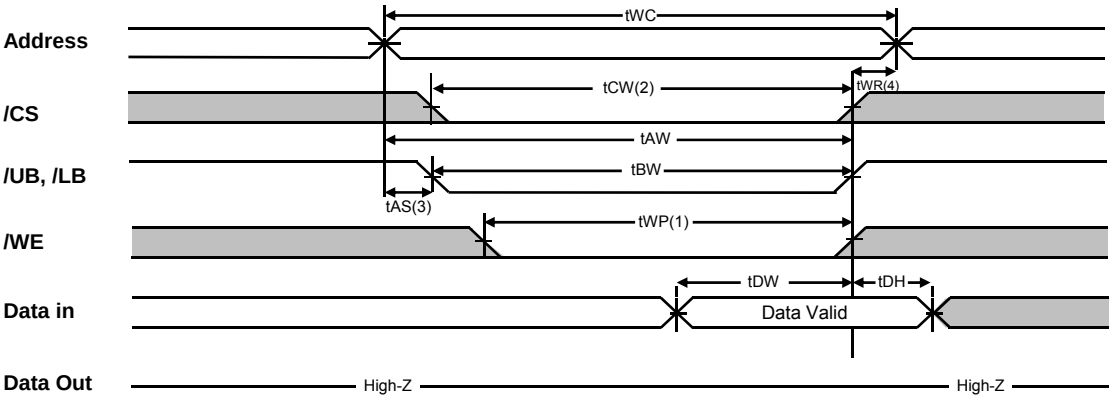
WRITE CYCLE (1) (/WE controlled, /ZZ=VIH)



WRITE CYCLE (2) (/CS controlled, /ZZ=/WE=VIH)



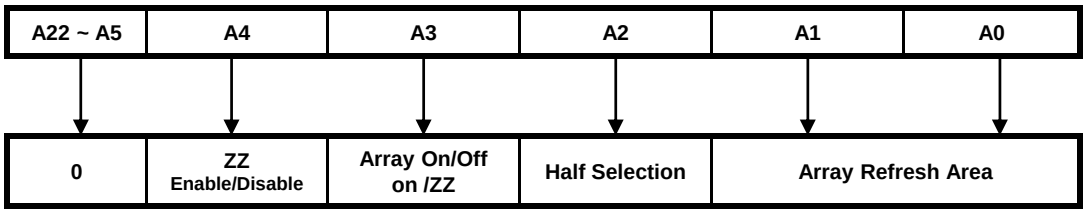
WRITE CYCLE (3) (/UB, /LB controlled, /ZZ=VIH)



1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

LOW POWER MODES

1. Mode Register Set



/ZZ Enable/Disable

A4	Type
0	Deep Power Down Enable
1	DPD Disable (Default)

Note: If the register is written to enable the Deep Power Down, the part will go into Deep Power Down during the following time that /ZZ is driven low and there is no MRS update. When /ZZ is driven high, all of the register settings will return to default state for the part (i.e. full array refresh, Deep Power Down Disabled).

Array On/Off on /ZZ

A3	Type
0	Partial Array Refresh Mode (Default)
1	Reduced Memory Size Mode

Note: The RMS(Reduced Memory Size) mode is enabled after /ZZ goes high and remains enabled after /ZZ goes high. To change to a different mode, the mode register will have to be rewritten.

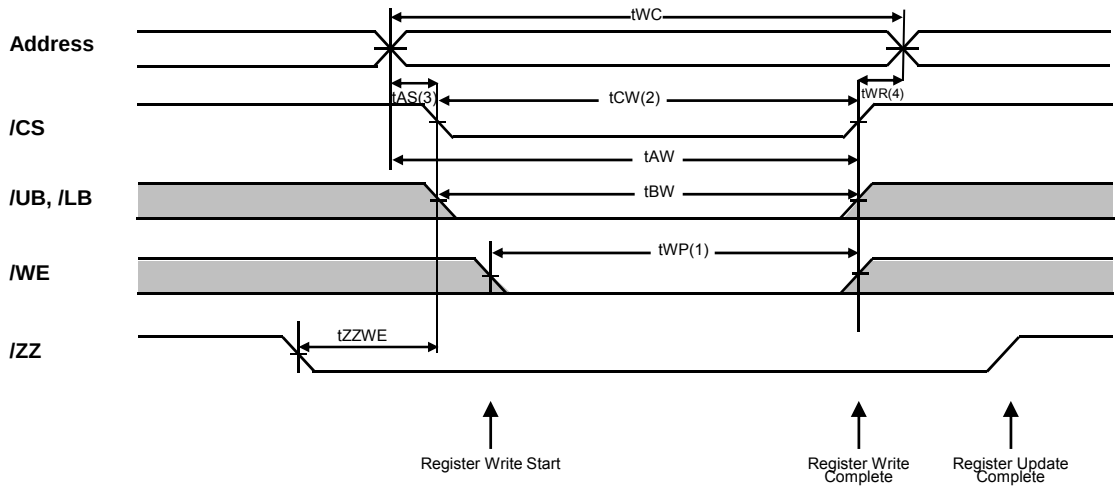
Half Selection (Top / Bottom)

A2	Type
0	Bottom (Default)
1	Top

Array Refresh Area

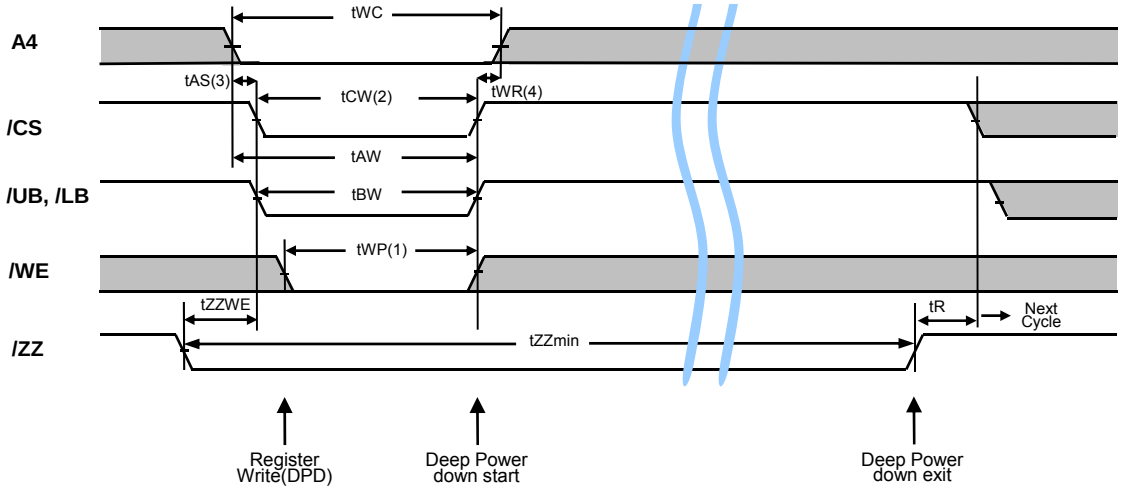
A1	A0	Type
0	0	Full Array (Default)
0	1	RFU
1	0	½ Array
1	1	¼ Array

2. MRS Update



The register update take place on the rising edge of /ZZ. Once the register is updated, the next time /ZZ goes low, without any updates to the register starting within the tZZWE max time of 1us, the part will refresh the array selected. The data bus is a don't care When /ZZ is low during the register updates.

3. Deep Power Down Mode Entry/Exit



Parameter	Description	Min	Max	Units
tZZWE	ZZ low to Write Enable Low	0	1	us
tR(Deep Power Down Mode only)	Operation Recovery Time	150	-	us
tZZmin	Low Power Mode Time	10	-	us

4. Address Information

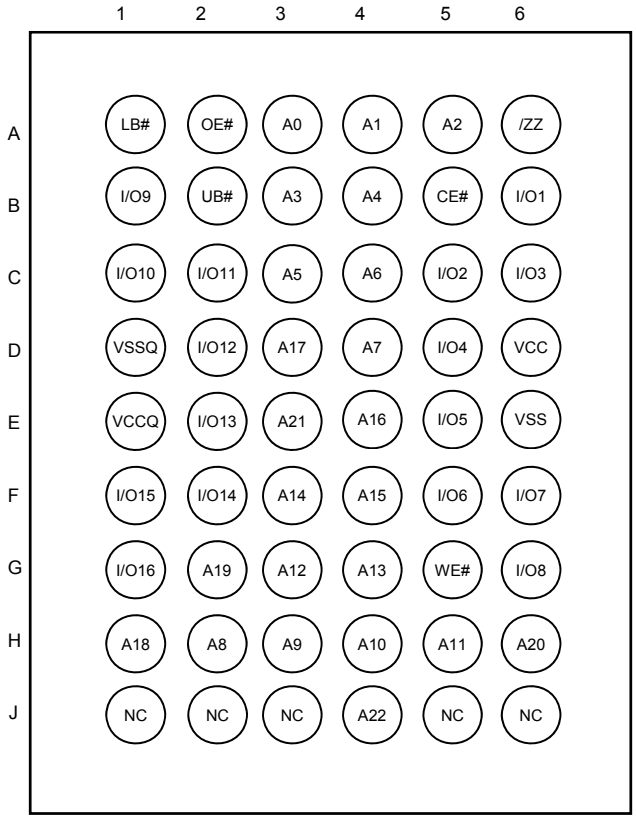
Partial Array Refresh Mode (A3=0, A4=1)

A2	A1,A0	Refresh Section	Address	Size	Density
0	11	1/4	000000h-1FFFFFh	2Mbx16	32Mb
0	10	1/2	000000h-3FFFFFh	4Mbx16	64Mb
X	00	Full	000000h-7FFFFFh	8Mbx16	128Mb
1	11	1/4	600000h-7FFFFFh	2Mbx16	32Mb
1	10	1/2	400000h-7FFFFFh	4Mbx16	64Mb

Reduced Memory Size Mode (A3=1, A4=1)

A2	A1,A0	Refresh Section	Address	Size	Density
0	11	1/4	000000h-1FFFFFh	2Mbx16	32Mb
0	10	1/2	000000h-3FFFFFh	4Mbx16	64Mb
1	11	1/4	600000h-7FFFFFh	2Mbx16	32Mb
1	10	1/2	400000h-7FFFFFh	4Mbx16	64Mb

54Ball FBGA Ball Assignment



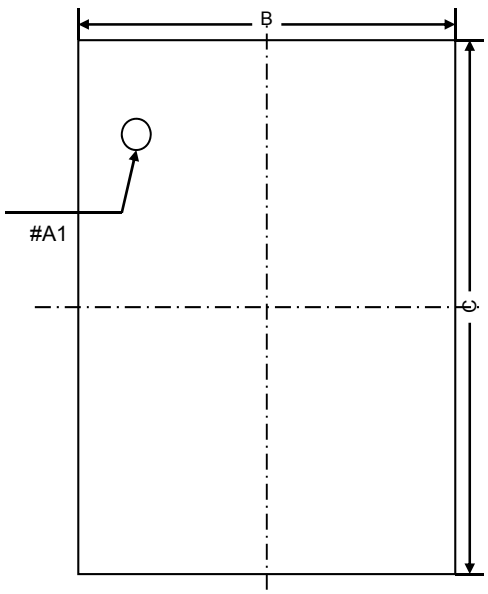
54-FBGA : Top View(Ball Down)

PACKAGE DIMENSION

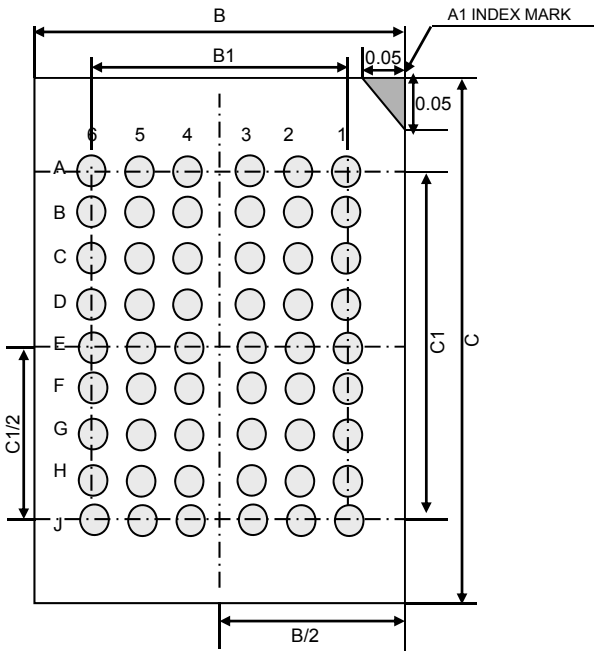
Unit : millimeters

54 BALL FINE PITCH BGA(0.75mm ball pitch)

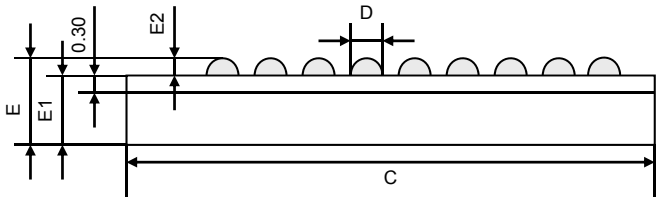
Top View



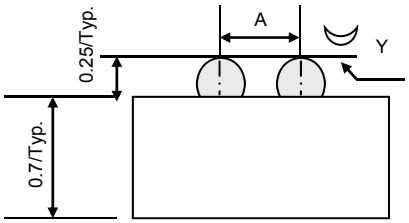
Bottom View



Side View



Detail A



-	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.30	0.35	0.40
E	-	0.8	1.00
E1	-	0.7	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 54(9row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)