AK4536

16-Bit Mono CODEC with ALC & MIC/SPK-AMP

GENERAL DESCRIPTION

The AK4536 is a 16-bit mono CODEC with Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit. Output circuits include a Speaker-Amplifier and Mono Line Output. The AK4536 suits a moving picture of Digital Still Camera and etc. The AK4536 is housed in a space-saving 28-pin QFN package.

FEATURE

1. 16-Bit Delta-Sigma Mono CODEC
2. Recording Function
   - 1ch Mono Input
   - 1st MIC Amplifier: 0dB or 20dB
   - 2nd Amplifier with ALC: -8dB ~ +27.5dB, 0.5dB Step
   - ADC Performance: S/(N+D): 80dB, DR, S/N: 85dB
3. Playback Function
   - Digital Volume: +12dB ~ -115dB, 0.5dB Step, Mute
   - Mono Line Output Performance: S/(N+D): 85dB, S/N: 95dB
   - Mono Speaker-Amp
     - Speaker-Amp Performance: S/(N+D): 50dB, S/N: 90dB (Po = 250mW)
     - BTL Output
     - ALC (Automatic Level Control) Circuit
     - Output Power: 250mW @ 8W, SVDD=3.3V
   - Beep Input
4. Power Management
5. Flexible PLL Mode:
   - Frequencies: 11.2896MHz, 12MHz or 12.288MHz (MCKI pin)
     1fs (FCK pin)
     16fs, 32fs or 64fs (BICK pin)
   - Input Level: CMOS or AC Coupling (MCKI pin)
6. EXT Mode:
   - Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
   - Input Level: CMOS or AC Coupling (MCKI pin)
7. Sampling Rate:
   - PLL Slave Mode: 7.35kHz ~ 26kHz
   - PLL Master Mode: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz or 24kHz
   - EXT Slave Mode: 7.35kHz ~ 26kHz (256fs or 512fs), 7.35kHz ~ 13kHz (1024fs)
8. Serial mP Interface: 3-wire
9. Master / Slave Mode
10. Audio Interface Format: MSB First, 2's compliment
    - ADC: DSP Mode, 16bit MSB justified, I2S
    - DAC: DSP Mode, 16bit MSB justified, 16bit LSB justified, I2S
11. Ta = -10 ~ 70°C
12. Power Supply
    - CODEC, Speaker-Amp: 2.4 ~ 3.6V (typ. 3.3V)
13. Power Supply Current: 19mA (All Power ON)
14. Package: 28pin QFN

■ Block Diagram

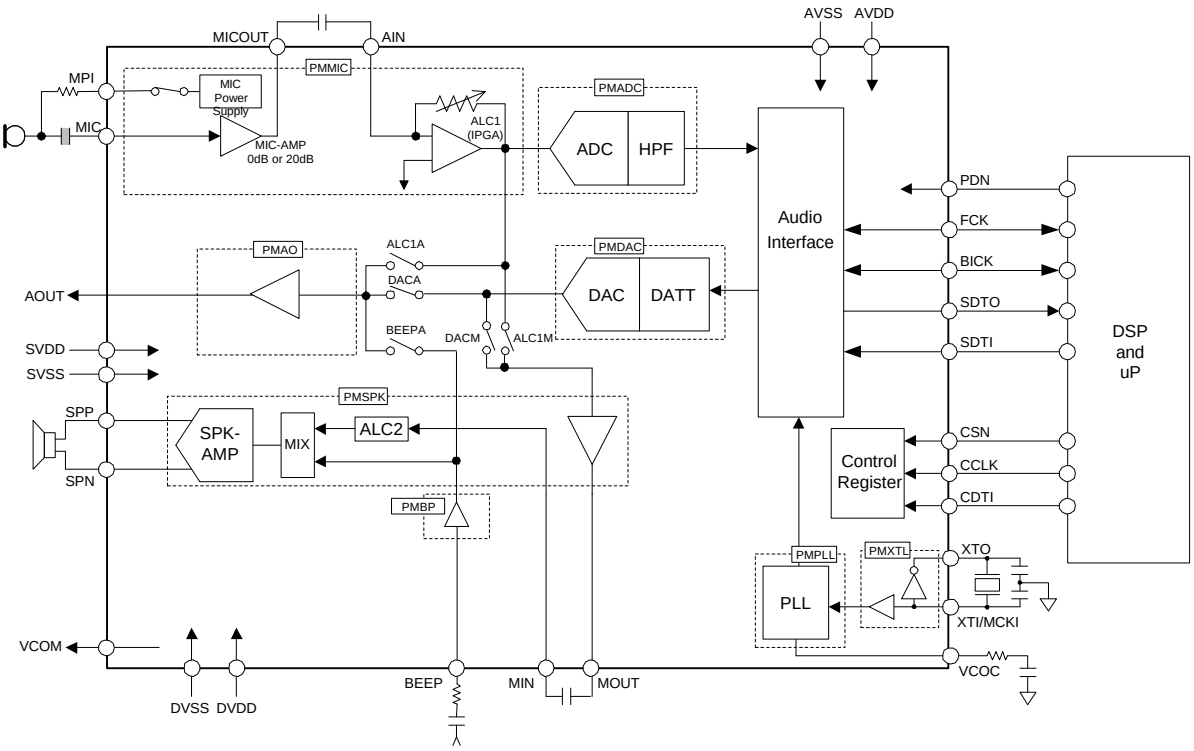
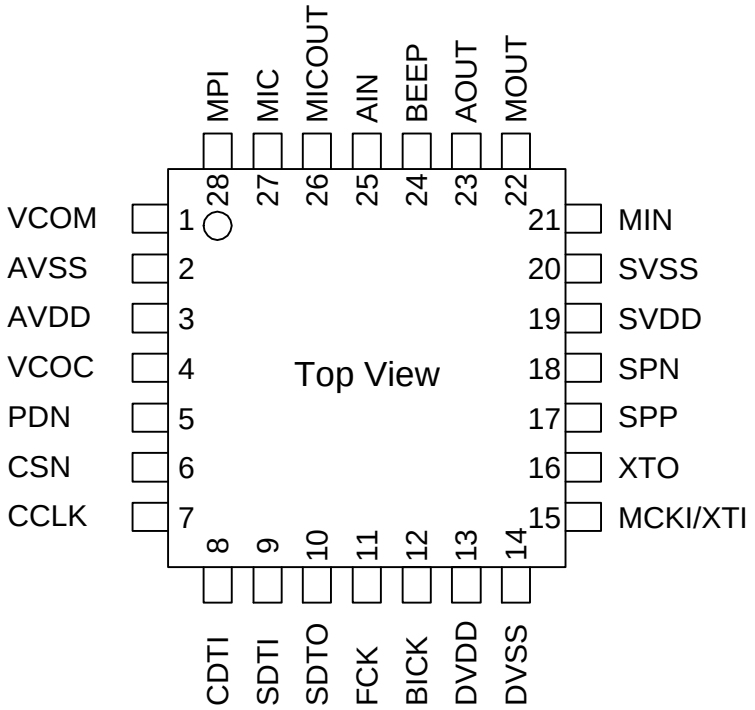


Figure 1. AK4536 Block Diagram

■ Ordering Guide

AK4536VN	–10 ~ +70°C	28pin QFN (0.5mm pitch)
AKD4536	Evaluation board for AK4536	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs.
2	AVSS	-	Analog Ground Pin
3	AVDD	-	Analog Power Supply Pin
4	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and capacitor in series.
5	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control register.
6	CSN	I	Chip Select Pin
7	CCLK	I	Control Data Clock Pin
8	CDTI	I	Control Data Input Pin
9	SDTI	I	Audio Serial Data Input Pin
10	SDTO	O	Audio Serial Data Output Pin
11	FCK	I/O	Frame Clock Pin
12	BICK	I/O	Audio Serial Data Clock Pin
13	DVDD	-	Digital Power Supply Pin
14	DVSS	-	Digital Ground Pin
15	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
16	XTO	O	X'tal Output Pin
17	SPP	O	Speaker Amp Positive Output Pin
18	SPN	O	Speaker Amp Negative Output Pin
19	SVDD	-	Speaker Amp Power Supply Pin
20	SVSS	-	Speaker Amp Ground Pin
21	MIN	I	ALC2 Input Pin
22	MOUT	O	Mono Analog Output Pin
23	AOUT	O	Mono Line Output Pin
24	BEEP	I	Beep Signal Input Pin
25	AIN	I	IPGA (ALC1) Input Pin
26	MICOUT	O	Microphone Analog Output Pin
27	MIC	I	Microphone Input Pin (Mono Input)
28	MPI	O	MIC Power Supply Pin for Microphone

Note: All input pins except analog input pins (MIC, AIN, MIN and BEEP pins) should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	Speaker-Amp	SVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – SVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and SVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.4	3.3	3.6	V
(Note 3)	Digital	DVDD	2.4	3.3	AVDD	V
	Speaker-Amp	SVDD	2.4	3.3	3.6	V

Note 1. All voltages with respect to ground
Note 3. The power up sequence between AVDD, DVDD and SVDD is not critical
It is recommended that DVDD and SVDD are the same voltage as AVDD in order to reduce the current at power down mode.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHRACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=3.3V; AVSS=DVSS=SVSS=0V; fs=8kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; EXT Slave Mode; unless otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier					
Input Resistance		20	30	40	kΩ
Gain	(MGAIN bit = "0")	-	0	-	dB
	(MGAIN bit = "1")	-	20	-	dB
MIC Power Supply: MPI pin					
Output Voltage (Note 4)		2.22	2.47	2.72	V
Output Current		-	-	1.25	mA
Input PGA Characteristics:					
Input Resistance (Note 5)		5	10	15	kΩ
Step Size		0.1	0.5	0.9	dB
Gain Control Range		–8		+27.5	dB
ADC Analog Input Characteristics: MIC Gain=20dB, IPGA=0dB, ALC1=OFF, MIC → IPGA → ADC					
Resolution				16	Bits
Input Voltage (MIC Gain=20dB,Note 6)		0.178	0.198	0.218	Vpp
S/(N+D) (−1dBFS) (Note 7)		70	80		dB
D-Range (−60dBFS)		77	85		dB
S/N		77	85		dB
DAC Characteristics:					
Resolution				16	Bits
Mono Line Output Characteristics: R_L=10kΩ, AOUT pin (DAC → AOUT)					
Output Voltage (Note 8)		1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS) (Note 7)		75	85		dB
D-Range (-60dBFS)		85	95		dB
S/N		85	95		dB
Load Resistance		10			kΩ
Load Capacitance (Note 15)				30	pF
Speaker-Amp Characteristics: R_L=8Ω, BTL, MIN pin → SPP/SPN pin, ALC2=OFF					
Output Voltage (Note 9)	SPKG = "0"	2.47	3.09	3.71	Vpp
	SPKG = "1"	3.20	4.00	4.80	Vpp
S/(N+D)	SPKG = "0", 150mW Output	50	60		dB
	SPKG = "1", 250mW Output	20	50		dB
S/N (Note 10)		80	90		dB
Load Resistance		8			Ω
Load Capacitance				30	pF
BEEP Input: BEEP pin					
Maximum Input Voltage (Note 11)				1.98	Vpp
Feedback Resistance		14	20	26	kΩ
Mono Input: MIN pin					
Maximum Input Voltage (Note 12)				2.18	Vpp
Input Resistance (Note 13)		12	24	36	kΩ
Mono Output: MOUT pin (DAC→ MOUT)					
Output Voltage (Note 14)		1.78	1.98	2.18	Vpp
Load Resistance		10			kΩ
Load Capacitance (Note 15)				30	pF

Parameter			min	typ	max	Units
Power Supplies						
Power Up (PDN = "H")						
	All Circuit Power-up: (Note 16)					
		AVDD+DVDD		10	15	mA
		SVDD: Speaker-Amp Normal Operation (SPPS bit = "1", No Output)		9	18	mA
Power Down (PDN = "L") (Note 17)						
	AVDD+DVDD+SVDD			10	200	μA

Note 4. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ)
Note 5. When IPGA Gain is changed, this typical value changes between 8kΩ and 11kΩ.
Note 6. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ)
Note 7. When a PLL reference clock is FCK pin in PLL Slave Mode, S/(N+D) is 60dB (typ).
Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)
Note 9. Input signal of MIN pin is 1.98Vpp.
Note 10. There are no relations with the setup of SPKG bit, and it is the same value.
Note 11. The maximum input voltage of the BEEP input shows output from AOUT.
Note 12. Maximum Input Voltage is proportional to AVDD voltage. Vin = 0.66 x AVDD (max)
Note 13. When ALC2 Gain is changed, this typical value changes between 22kΩ and 26kΩ.
Note 14. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)
Note 15. When the output pin drives a capacitive load, a resistor should be added in series between the output pin and capacitive load.
Note 16. PLL Master Mode (X'tal = 12.288MHz) and PMMIC = PMADC = PMDAC = PMSPK = PMVCM = PMPLL = PMXTL = PMAO = PMBP = M/S = "1". And output current from MPI pin is 0mA. When the AK4536 is EXT mode (PMPLL = PMXTL = M/S = "0"), "AVDD+DVDD" is typically 8mA.
Note 17. All digital input pins are fixed to DVDD or DVSS.

FILTER CHRACTERISTICS

(Ta = 25°C; AVDD, DVDD, SVDD =2.4 ~ 3.6V; fs=8kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 18)	±0.16dB	PB	0		3.0	kHz
	-0.66dB		-	3.5	-	kHz
	–1.1dB		-	3.6	-	kHz
	–6.9dB		-	4.0	-	kHz
Stopband (Note 18)		SB	4.8			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 19)		GD		17.1		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 18)	–3.0dB	FR	-	1.25	-	Hz
	–0.5dB		-	3.56	-	Hz
	–0.1dB		-	8.14	-	Hz
DAC Digital Filter:						
Passband (Note 18)	±0.12dB	PB	0		3.6	kHz
	–6.2dB		-	4.0	-	kHz
Stopband (Note 18)		SB	4.4			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 19)		GD		16.9		1/fs
Group Delay Distortion		ΔGD		0		μs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 3.4kHz		FR		±1.0		dB

Note 18. The passband and stopband frequencies are proportional to fs (system sampling rate).
For example, ADC is PB=0.45*fs (@-1.1dB). A reference of frequency response is 1kHz.

Note 19. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of a channel from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of a channel from the input register to the output of analog signal.

DC CHRACTERISTICS

(Ta = 25°C; AVDD, DVDD, SVDD=2.4 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling	(Note 20)	VAC	50%DVDD	-	-	Vpp
High-Level Output Voltage	(Iout=−80μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage	(Iout= 80μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

Note 20. When AC coupled capacitor is connected to MCKI pin.

SWITING CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD, SVDD=2.4 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI/XTI pin) (See Figure 3, Figure 4 and Figure 5)					
Crystal Resonator Frequency	fCLK	11.2896		12.288	MHz
External Clock Frequency	fCLK	11.2896		12.288	MHz
Pulse Width Low	tCLKL	0.4/fCLK			ns
Pulse Width High	tCLKH	0.4/fCLK			ns
AC Pulse Width (Note 23)	tACW	0.4/fCLK			ns
FCK Frequency	fFCK	8		24	kHz
Pulse width High	tFCKH		tBCK		ns
BICK Frequency (BCKO1-0 = "00")	tBCK		1/16fFCK		ns
(BCKO1-0 = "01")	tBCK		1/32fFCK		ns
(BCKO1-0 = "10")	tBCK		1/64fFCK		ns
BICK Duty	dBCK		50		%
FCK "↑" to BICK "↑" (Note 21)	tDBF		0.5 x tBCK		ns
FCK "↑" to BICK "↓" (Note 22)	tDBF		0.5 x tBCK		ns
BICK "↑" to SDTO (BCKP = "0")	tBSD			80	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD			80	ns
SDTI Hold Time	tSDH	60			ns
SDTI Setup Time	tSDS	60			ns
PLL Slave Mode (PLL Reference Clock = FCK pin) (See Figure 6, Figure 7, Figure 8 and Figure 9)					
FCK Frequency	fFCK	7.35	8	26	kHz
Pulse Width High	tFCKH	tBCK-60		1/fFCK-tBFCK	ns
BICK Period	tBCK	1/64fFCK		1/16fFCK	ns
BICK Pulse Width Low	tBCKL	240			ns
Pulse Width High	tBCKH	240			ns
FCK "↑" to BICK "↑" (Note 21)	tFCKB	0.4 x tBCK			ns
FCK "↑" to BICK "↓" (Note 22)	tFCKB	0.4 x tBCK			ns
BICK "↑" to FCK "↑" (Note 21)	tBFCK	0.4 x tBCK			ns
BICK "↓" to FCK "↑" (Note 22)	tBFCK	0.4 x tBCK			ns
BICK "↑" to SDTO (BCKP = "0")	tBSD			80	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD			80	ns
SDTI Hold Time	tSDH	60			ns
SDTI Setup Time	tSDS	60			ns

Parameter	Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = BICK pin) (See Figure 6, Figure 7, Figure 8 and Figure 9)					
FCK Frequency	fFCK	7.35		26	kHz
Pulse width High	tFCKH	tBCK-60		1/fFCK-tBFCK	ns
BICK Period (PLL2-0 = "001")	tBCK		1/16fFCK		ns
(PLL2-0 = "010")	tBCK		1/32fFCK		ns
(PLL2-0 = "011")	tBCK		1/64fFCK		ns
BICK Pulse Width Low	tBCKL	0.4 x tBCK			ns
Pulse Width High	tBCKH	0.4 x tBCK			ns
FCK "↑" to BICK "↑" (Note 21)	tFCKB	0.4 x tBCK			ns
FCK "↑" to BICK "↓" (Note 22)	tFCKB	0.4 x tBCK			ns
BICK "↑" to FCK "↑" (Note 21)	tBFCK	0.4 x tBCK			ns
BICK "↓" to FCK "↑" (Note 22)	tBFCK	0.4 x tBCK			ns
BICK "↑" to SDTO (BCKP = "0")	tBSD			80	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD			80	ns
SDTI Hold Time	tSDH	60			ns
SDTI Setup Time	tSDS	60			ns
EXT Slave Mode (See Figure 10 and Figure 11)					
MCKI Frequency: 256fs	fCLK	1.8816	2.048	6.656	MHz
512fs	fCLK	3.7632	4.096	13.312	MHz
1024fs	fCLK	7.5264	8.192	13.312	MHz
Pulse Width Low	tCLKL	0.4/fCLK			ns
Pulse Width High	tCLKH	0.4/fCLK			ns
AC Pulse Width (Note 23)	tACW	0.4/fCLK			ns
FCK Frequency (MCKI = 256fs or 512fs)	fFCK	7.35	8	26	kHz
(MCKI = 1024fs)	fFCK	7.35	8	13	kHz
Duty	duty	45		55	%
BICK Period	tBCK	600			ns
BICK Pulse Width Low	tBCKL	240			ns
Pulse Width High	tBCKH	240			ns
FCK Edge to BICK "↑" " (Note 24)	tFCKB	50			ns
BICK "↑" to FCK Edge (Note 24)	tBFCK	50			ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns

Note 21. MSBS, BCKP bits = "00" or "11"
Note 22. MSBS, BCKP bits = "01" or "10"
Note 23. Pulse width to ground level when MCKI is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3)
Note 24. BICK rising edge must not occur at the same time as FCK edge.

Parameter		Symbol	min	typ	max	Units
Control Interface Timing:						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN "H" Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	150			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 25)	tPD	150			ns
PMADC "↑" to SDTO valid	(Note 26)	tPDV		1059		1/fs

Note 25. The AK4536 can be reset by the PDN pin = "L".
Note 26. This is the count of FCK "↑" from the PMADC bit = "1".

■ Timing Diagram

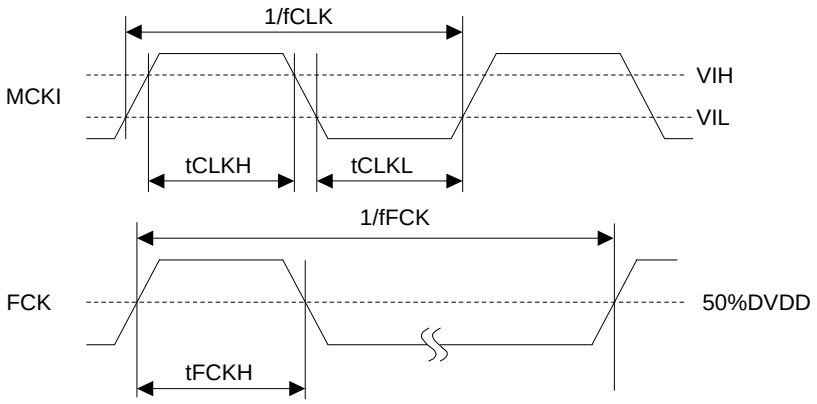


Figure 2. Clock Timing (PLL, Master mode)

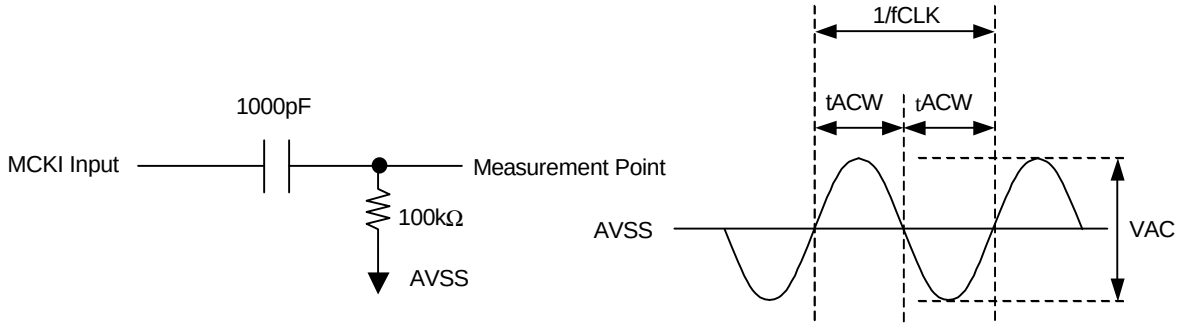


Figure 3. MCKI AC Coupling Timing

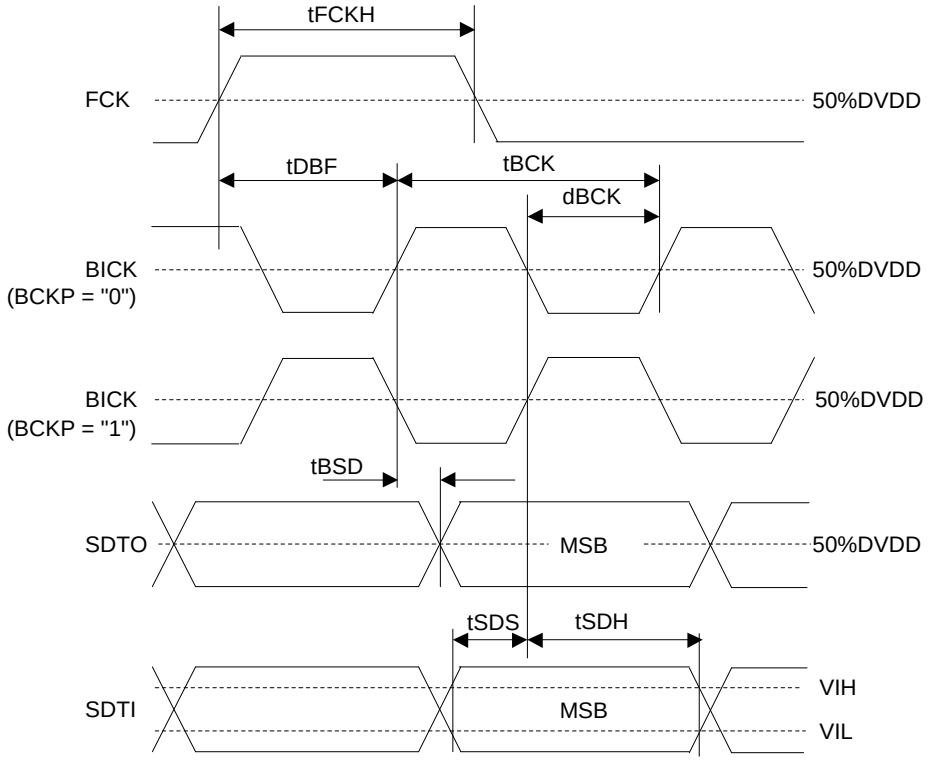


Figure 4. Audio Interface Timing (PLL, Master mode, MSBS = “0”)

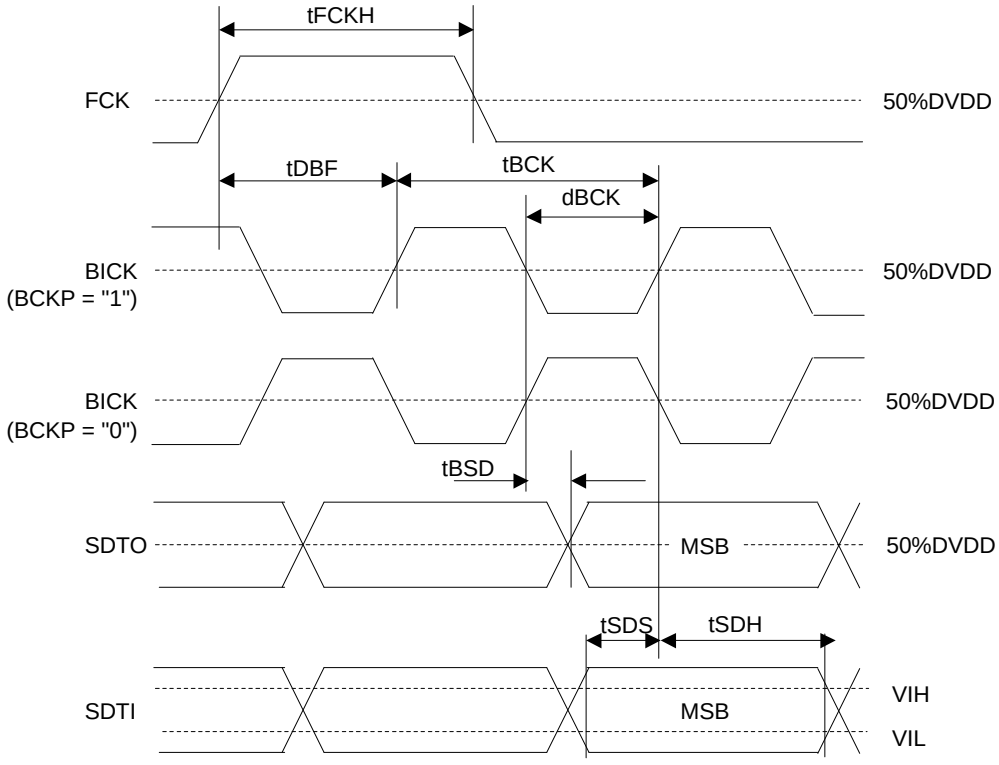


Figure 5. Audio Interface Timing (PLL, Master mode, MSBS = “1”)

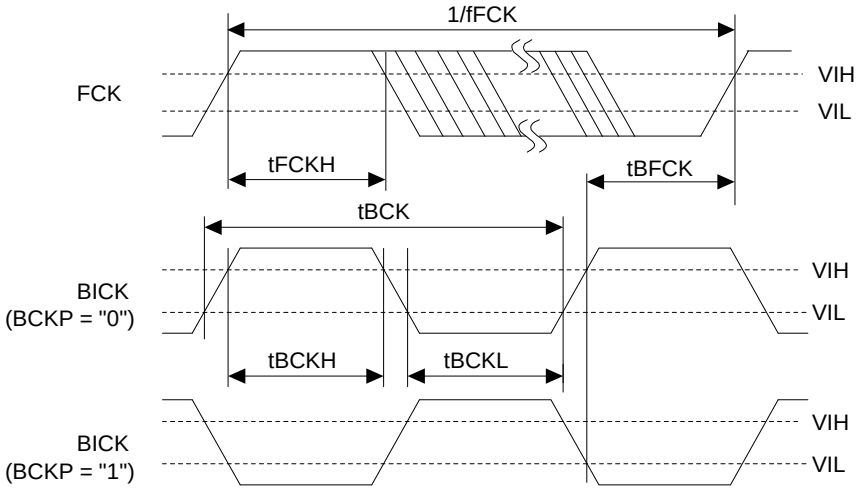


Figure 6. Clock Timing (PLL, Slave mode, MSBS = 0)

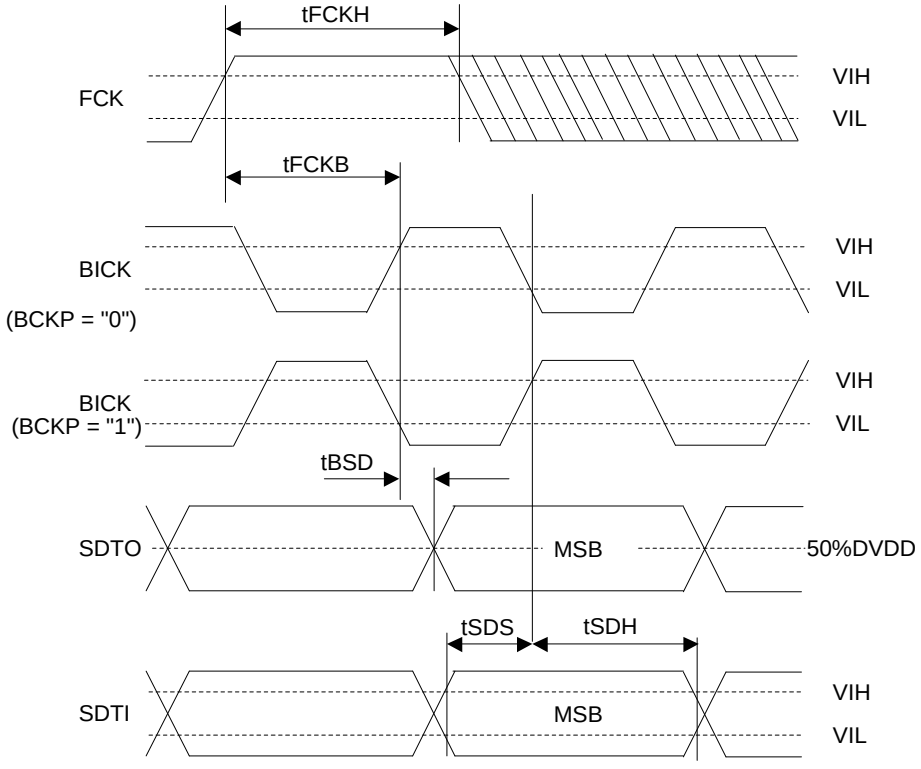


Figure 7. Audio Interface Timing (PLL, Slave mode, MSBS = 0)

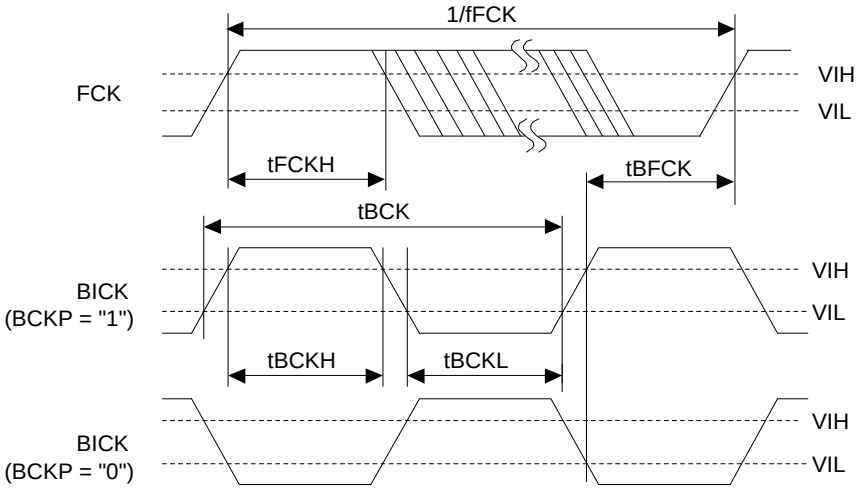


Figure 8. Clock Timing (PLL, Slave mode, MSBS = 1)

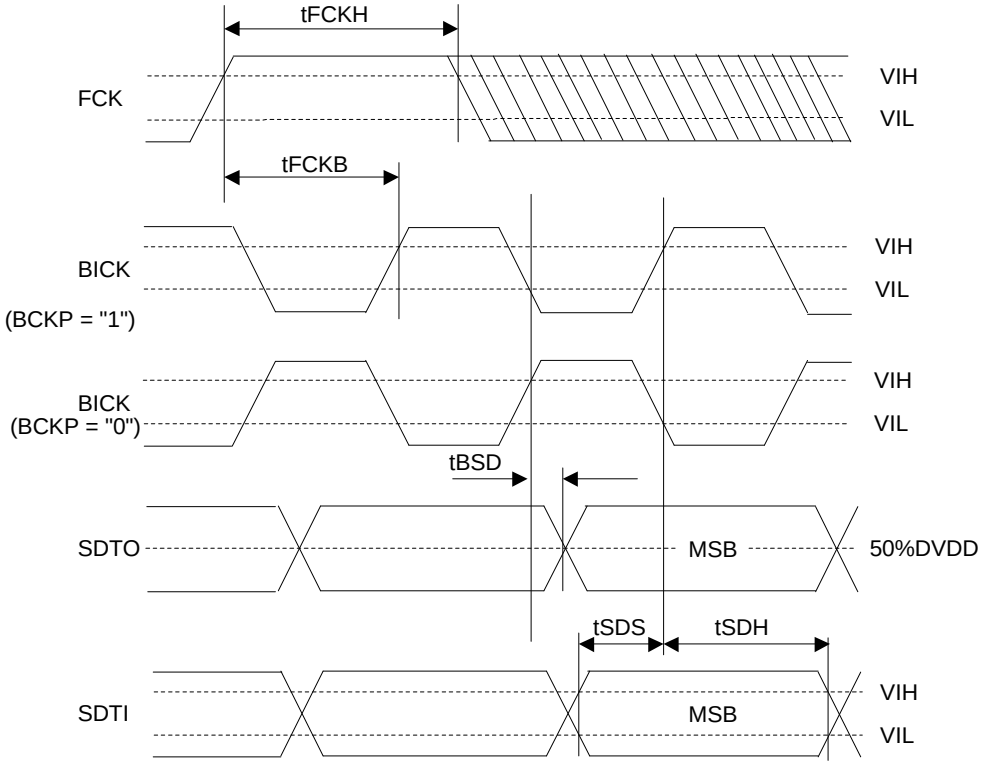


Figure 9. Audio Interface Timing (PLL, Slave mode, MSBS = 1)

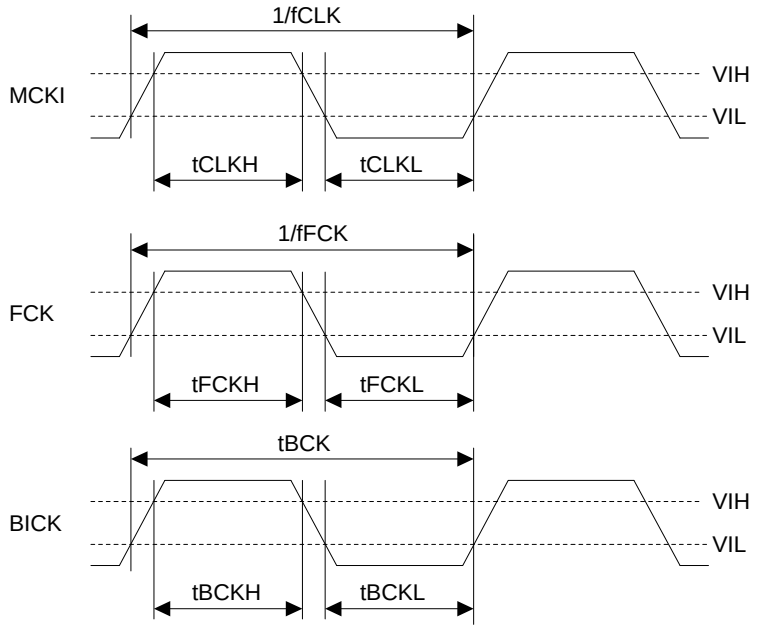


Figure 10. Clock Timing (EXT, Slave mode)

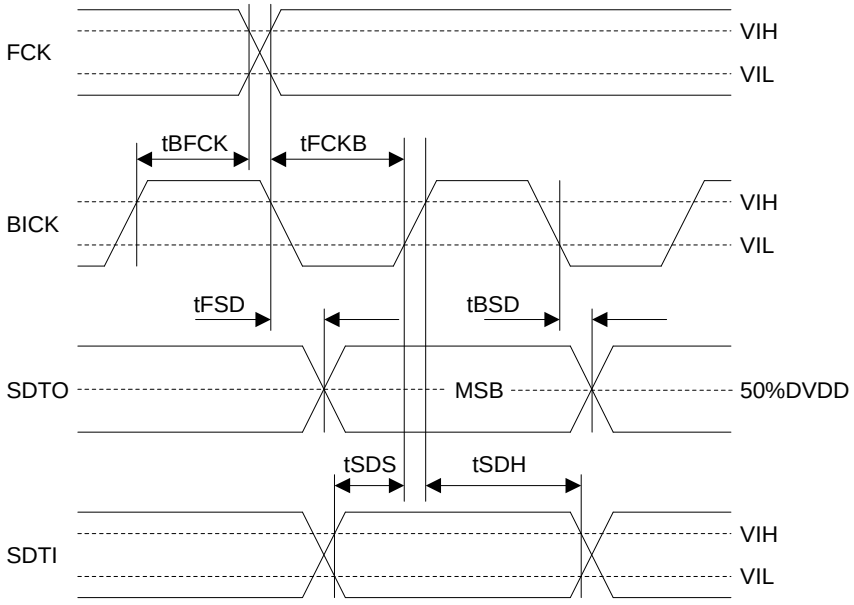


Figure 11. Audio Interface Timing (EXT, Slave mode)

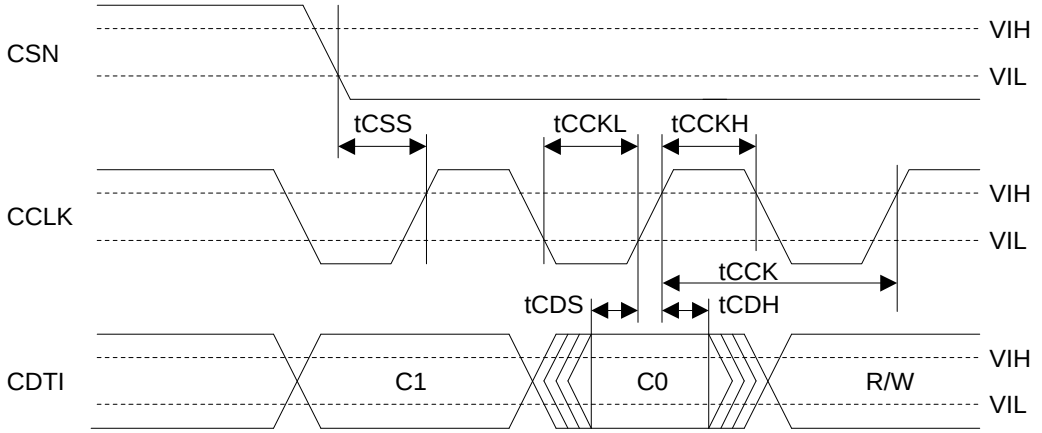


Figure 12. WRITE Command Input Timing

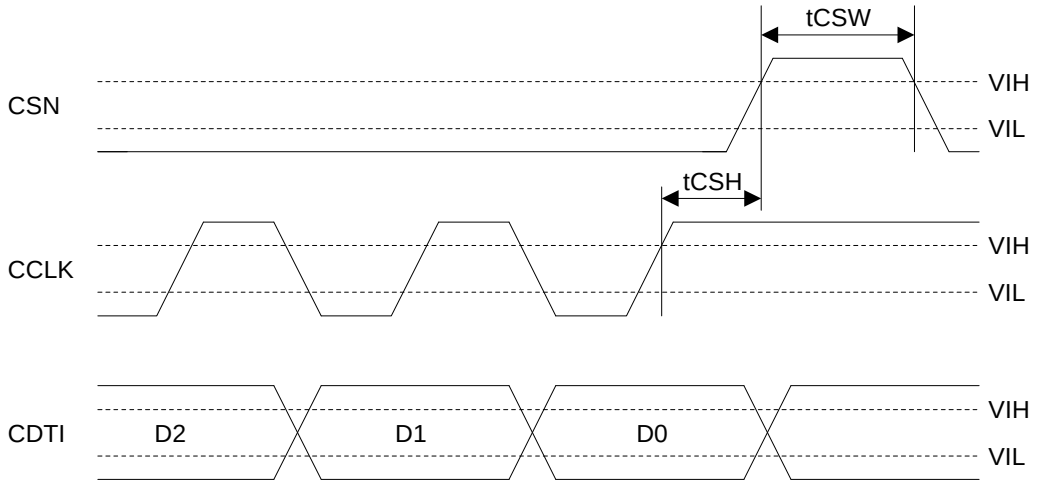


Figure 13. WRITE Data Input Timing

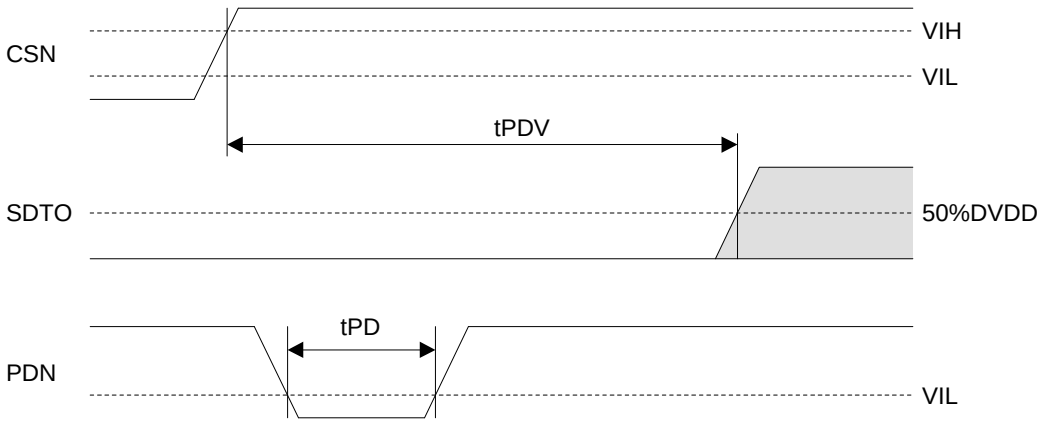


Figure 14. Power Down & Reset Timing

OPERATION OVERVIEW

■ Master Clock Source

The AK4536 requires a master clock (MCKI). This master clock is input to the AK4536 by connecting a X'tal oscillator to XTI and XTO pins or by inputting an external CMOS-level clock to the XTI pin or by inputting an external clock that is greater than 50% of the DVDD level to the XTI pin through a capacitor. When using a X'tal oscillator, there should be capacitors between XTI/XTO pins and DVSS.

Master Clock		Status	PMXTL bit	MCKPD bit
X'tal Oscillator	(Figure 15)	Oscillator ON	1	0
		Oscillator OFF	0	1
External Clock Direct Input	(Figure 16)	Clock is input to MCKI pin.	0	0
		MCKI pin is fixed to "L".	0	0/1
		MCKI pin is fixed to "H".	0	0
		MCKI pin is Hi-Z.	0	1
AC Coupling Input	(Figure 17)	Clock is input to MCKI pin.	1	0
		Clock isn't input to MCKI pin.	0	1

Table 1. Master Clock Status by PMXTL bit and MCKPD bit

(1) X'tal Oscillator

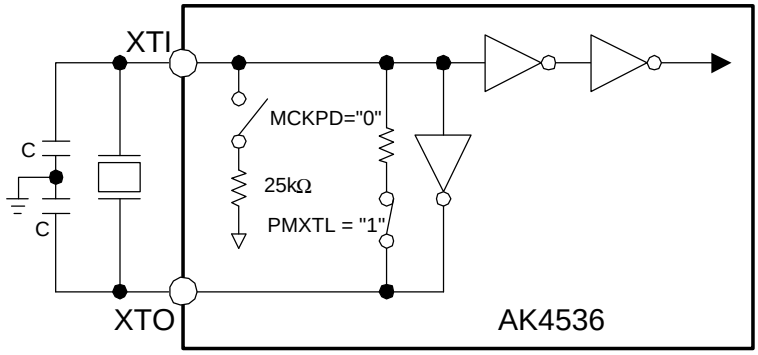


Figure 15. X'tal mode

- Note: The capacitor values depend on the X'tal oscillator used. (typ. 10 ~ 30pF)

(2) External Clock Direct Input

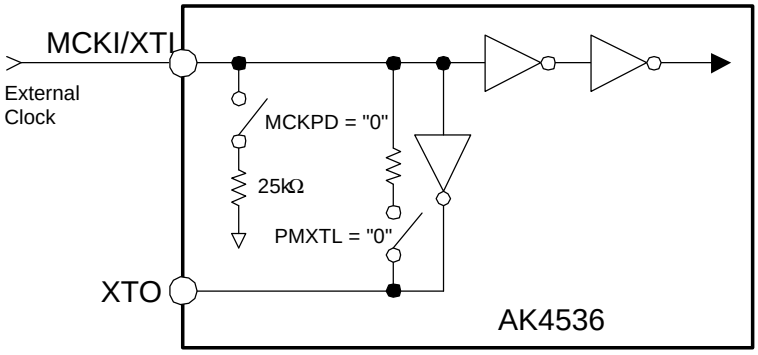


Figure 16. External Clock mode (Input: CMOS Level)
- Note: This clock level must not exceed DVDD level.

(3) AC Coupling Input

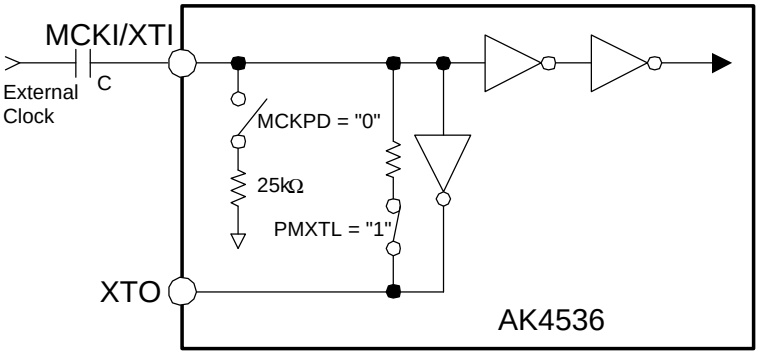


Figure 17. External Clock mode (Input: ≥ 50%DVDD)
- Note: This clock level must not exceed DVDD level.

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL2-0 and FS2-0 bits. The PLL lock time is shown in Table 3, whenever the AK4536 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Select PLL/ EXT Mode

PMPLL bit	Mode	
0	EXT Mode	Default
1	PLL Mode	

Table 2. Select PLL/EXT Mode

2) Setting of PLL Mode

Mode	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
						R[Ω]	C[F]		
0	0	0	0	FCK pin	1fs	10k	470n	160ms	Default
1	0	0	1	BICK pin	16fs	10k	4.7n	2ms	
2	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
4	1	0	0	MCKI/XTI pin	11.2896MHz	10k	4.7n	40ms	
5	1	0	1	MCKI/XTI pin	12.288MHz	10k	4.7n	40ms	
6	1	1	0	MCKI/XTI pin	12MHz	10k	4.7n	40ms	
7	1	1	1	N/A	N/A	-	-	-	

Table 3. Setting of PLL Mode (*fs: Sampling Frequency)

3) Setting of sampling frequency in PLL Mode.

When PLL2 bit is "1" (PLL reference clock input is XTI/MCKI pin), the sampling frequency is selected by FS2-0 bits as defined in Table 4.

Mode	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	8kHz	Default
1	0	0	1	12kHz	
2	0	1	0	16kHz	
3	0	1	1	24kHz	
4	1	0	0	N/A	
5	1	0	1	11.025kHz	
6	1	1	0	N/A	
7	1	1	1	22.05kHz	

Table 4. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL = "1"

When PLL2 bit is "0" (PLL reference clock input is FCK or BICK pin), the sampling frequency is selected by FS1-0 bits. (See Table 5). **FS2 bit is ignored.**

Mode	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	7.35kHz ≤ fs ≤ 10kHz	Default
1	0	1	10kHz < fs ≤ 14kHz	
2	1	0	14kHz < fs ≤ 20kHz	
3	1	1	20kHz < fs ≤ 26kHz	

Table 5. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL = "1"

■ PLL Unlock

1) PLL, Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, irregular frequency clocks are output from FCK and BICK pins after PMPLL bit = "0" → "1". After that PLL is unlocked, BICK and FCK pins output "L" for a moment. (See Table 6) Therefore a first period of FCK and BICK may be irregular clock, but these clocks return to normal after a period of 1/fs.

	Master Mode (M/S bit = "1")		
	After that PMPLL "0" → "1"	PLL Unlock	PLL Lock
BICK pin	Irregular clock output	"L" Output	See Table 9
FCK pin	Irregular clock output	"L" Output	1fs Output

Table 6. Clock Operation at Master & PLL Mode

2) PLL, Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, ADC and DAC are output to abnormal data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACA and DACM bits in Addr=02H.

■ Master Mode/Slave Mode

The M/S bit selects either master or slave modes. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4536 is power-down mode (PDN pin = "L") and exits reset state, the AK4536 is slave mode. After exiting reset state, the AK4536 goes master mode by changing M/S bit = "1".

When the AK4536 is used by master mode, FCK and BICK pins are a floating state until M/S bit becomes "1". FCK and BICK pins of the AK4536 should be pulled-down or pulled-up by about 100kΩ resistor externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	Default
1	Master Mode	

Table 7. Select Master/Salve Mode

■ System Clock

There are the following three methods to interface with external devices. (See Table 8)

Mode	Master Mode (M/S bit = "1")			Slave Mode (M/S bit = "0")		
Pin	MCKI/XTI	BICK	FCK	MCKI/XTI	BICK	FCK
PLL (PMPLL bit = "1")	11.2896MHz/ 12MHz/ 12.288MHz Input	16fs/32fs/64fs Output	fs Output	GND (MCKPD bit = "1")	16fs/32fs/64fs Input	fs Input
EXT (PMPLL bit = "0")	Don't use (Note 27)			256fs/512fs/1024fs Input	≥ 32fs Input	fs Input

Table 8. Clock Operation

Note 27. If this mode is selected, the irregular clocks are output from FCK and BICK pins.

1) PLL, Master Mode (PMPLL bit = "1", M/S bit = "1")

When the AK4536 is connected to X'tal oscillator or an external clock (11.2896MHz, 12MHz or 12.288MHz) is input to MCKI pin, the BICK and FCK clocks are generated by an internal PLL circuit. The BICK is selected among 16fs, 32fs or 64fs, by BCKO1-0 bits. (See Table 9)

Audio interface format corresponds to Mode 0 (DSP Mode) only.

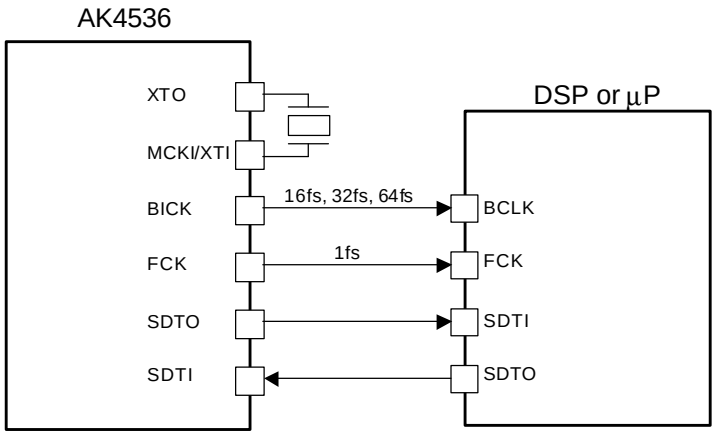


Figure 18. PLL & Master Mode

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency	
0	0	0	16fs	Default
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 9. Output Frequency of BICK at Master Mode

2) PLL, Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is input from BICK or FCK pins. The required clock to the AK4536 is generated by an internal PLL circuit. Input frequency is selected by PLL2-0 bits. Sampling frequency corresponds to 7.35kHz ~ 26kHz by changing FS1-0 bits. (See Table 5)

Audio interface format corresponds to Mode 0 (DSP Mode) only.

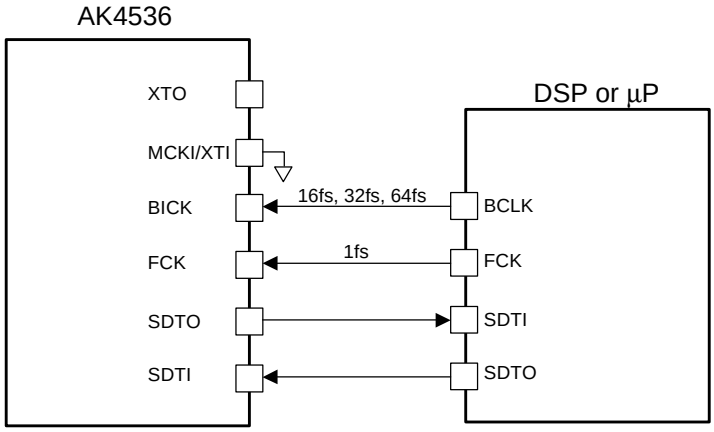


Figure 19. PLL & Slave Mode

The external clocks (BICK and FCK) should always be present whenever the ADC or DAC is in operation (PMADC bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4536 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC bit =PMDAC bit = "0").

3) EXT, Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4536 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), FCK (fs) and BICK (32fs~). The master clock (MCKI) should be synchronized with FCK. The phase between these clocks does not matter. The frequency of MCLK is selected by FS1-0 bits. (See Table 10)

Mode	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	7.35kHz ~ 26kHz	Default
1	0	1	1024fs	7.35kHz ~ 13kHz	
2	1	0	256fs	7.35kHz ~ 26kHz	
3	1	1	512fs	7.35kHz ~ 26kHz	

Table 10. MCKI Frequency at EXT, Slave Mode (PMPLL bit = "0", M/S bit = "0")

*** FS2 bit is ignored.**

Audio interface format corresponds to Mode 1, 2 or 3.

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. When the out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through AOUT amp at fs=8kHz is shown in Table 11.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weight)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 11. Relationship between MCLK and S/N of AOUT

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC is in operation (PMADC bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4536 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC bit = PMDAC bit = "0").

In case of changing sampling frequency while DAC is normal operation, the change of sampling frequency should be done after the input data is input to "0" or muted by DVOL7-0 bits.

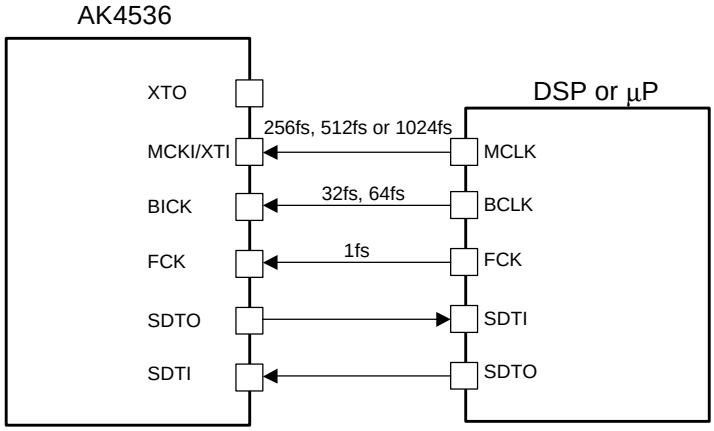


Figure 20. EXT, Slave Mode

■ System Reset

Upon power-up, reset the AK4536 by bringing the PDN pin = “L”. This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADC bit is changed from “0” to “1”. The initialization cycle time is 1059/fs, or 133ms@fs=8kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. The DAC does not require an initialization cycle.

■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits. (See Table 13) In all modes, the serial data is MSB first, 2’s complement format. Audio interface formats can be used in both master and slave modes. FCK and BICK are output from AK4536 in master mode, but must be input to AK4536 in slave mode.

In Mode0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is “0”, SDTO data is output by rising edge of BICK, SDTI data is latched by falling edge of BICK.
When BCKP bit is “1”, SDTO data is output by falling edge of BICK, SDTI data is latched by rising edge of BICK.

MSB data position of SDTO and SDTI can be shifted by MSBS bit. The shifted period is a half of BICK.

MSBS bit	BCKP bit	Data Input/Output Timing
0	0	Figure 21
0	1	Figure 23
1	0	Figure 22
1	1	Figure 24

Table 12. Relationship MSBS and BCKP bits between data I/O timing

In Mode 1-3, the SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge.

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, −1 at 16bit data is converted to −1 at 8-bit data. And when the DAC playbacks this 8-bit data, −1 at 8-bit data will be converted to −256 at 16-bit data and this is a large offset. This offset can be removed by adding the offset of 128 to 16-bit data before converting to 8-bit data.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 16fs	Figure 21 Figure 22 Figure 23 Figure 24	
1	0	1	MSB justified	MSB justified	≥ 32fs	Figure 25	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 26	Default
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 27	

Table 13. Audio Interface Format

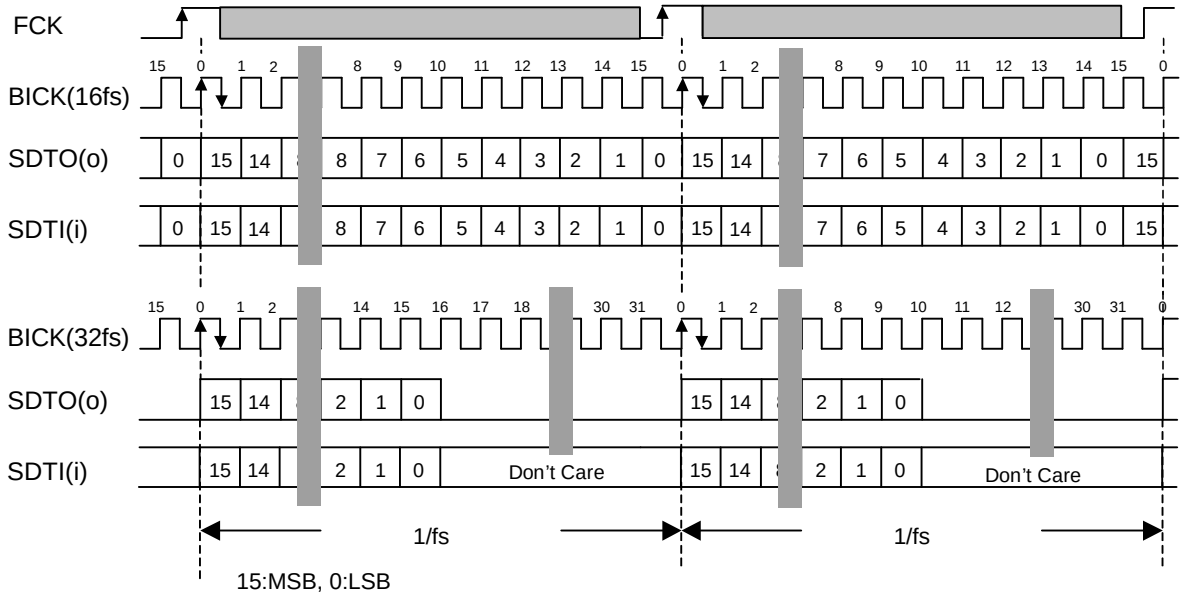


Figure 21. Mode 0 Timing (BCKP = "0", MSBS = "0")

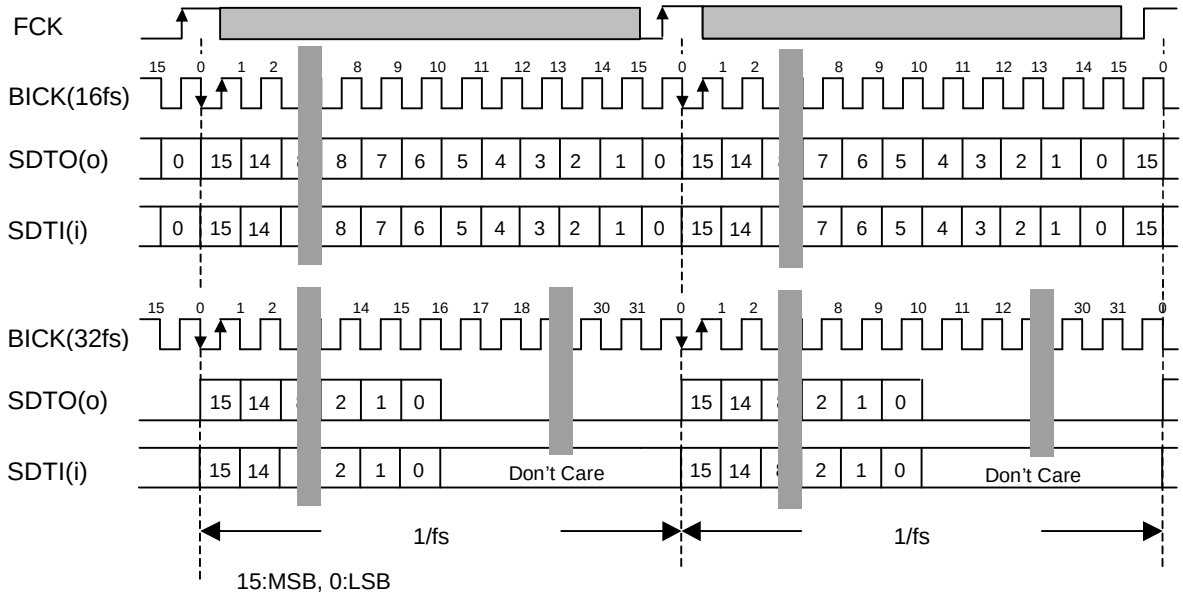


Figure 22. Mode 0 Timing (BCKP = "1", MSBS = "0")

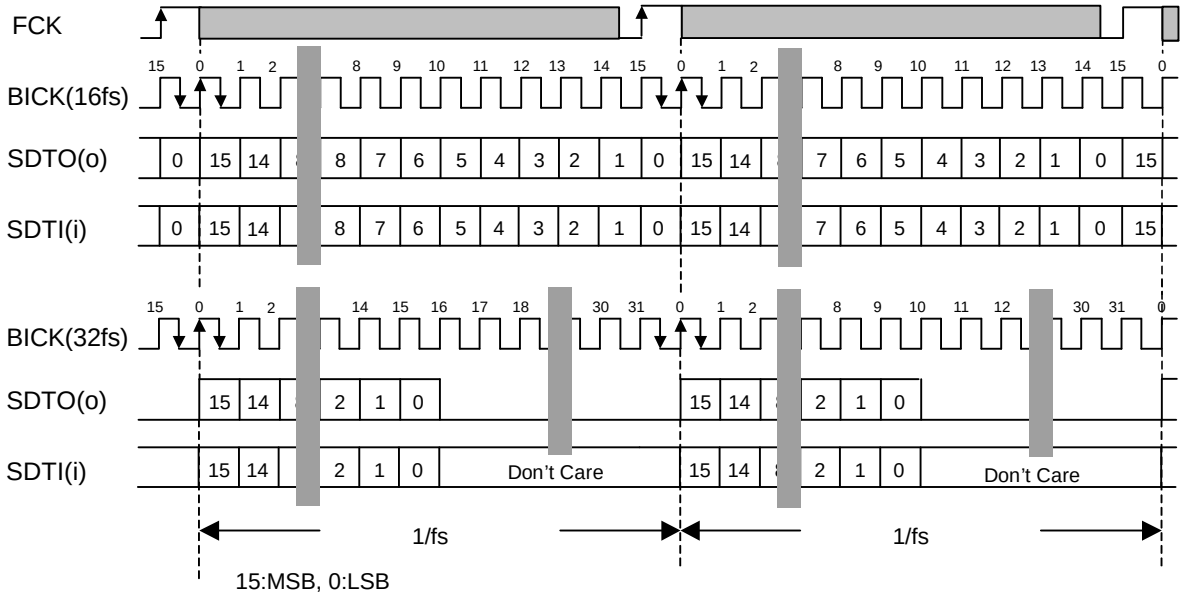


Figure 23. Mode 0 Timing (BCKP = "0", MSBS = "1")

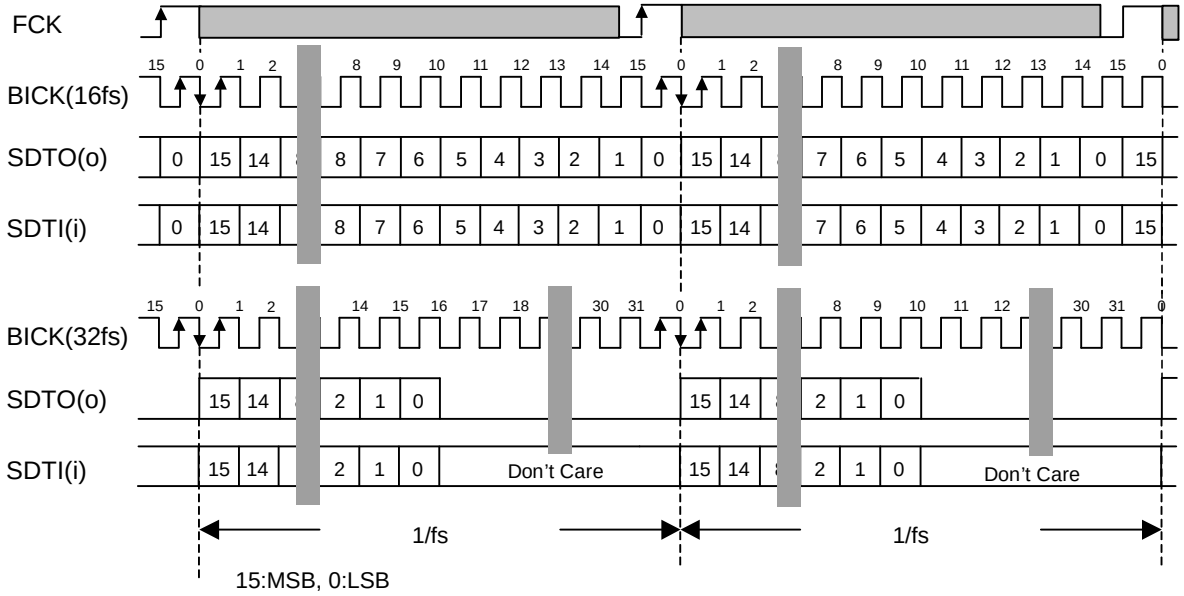


Figure 24. Mode 0 Timing (BCKP = "1", MSBS = "1")

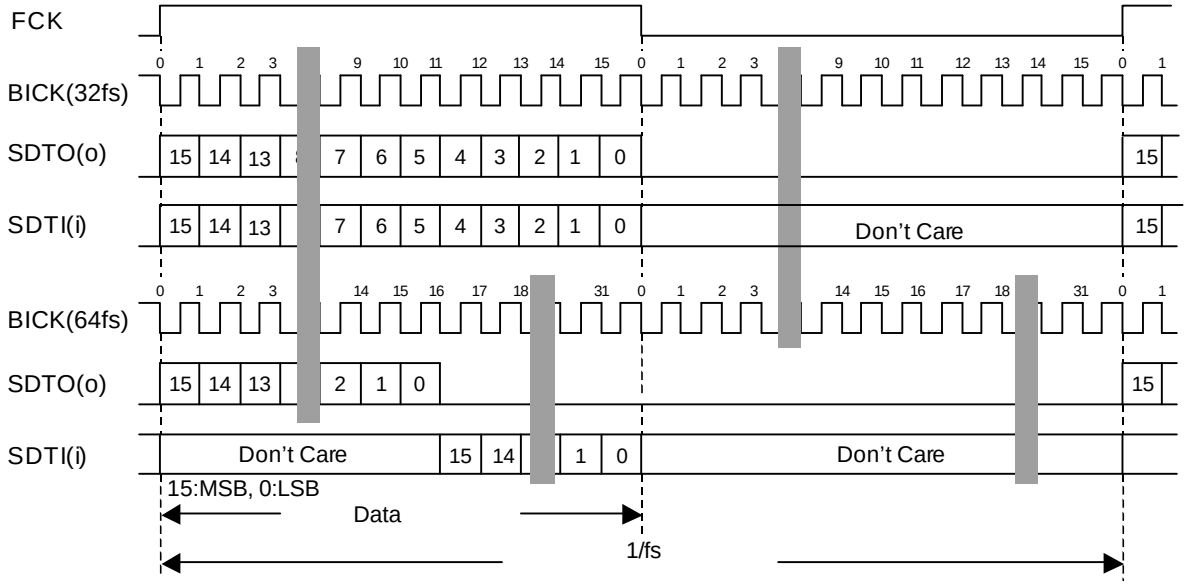


Figure 25. Mode 1 Timing

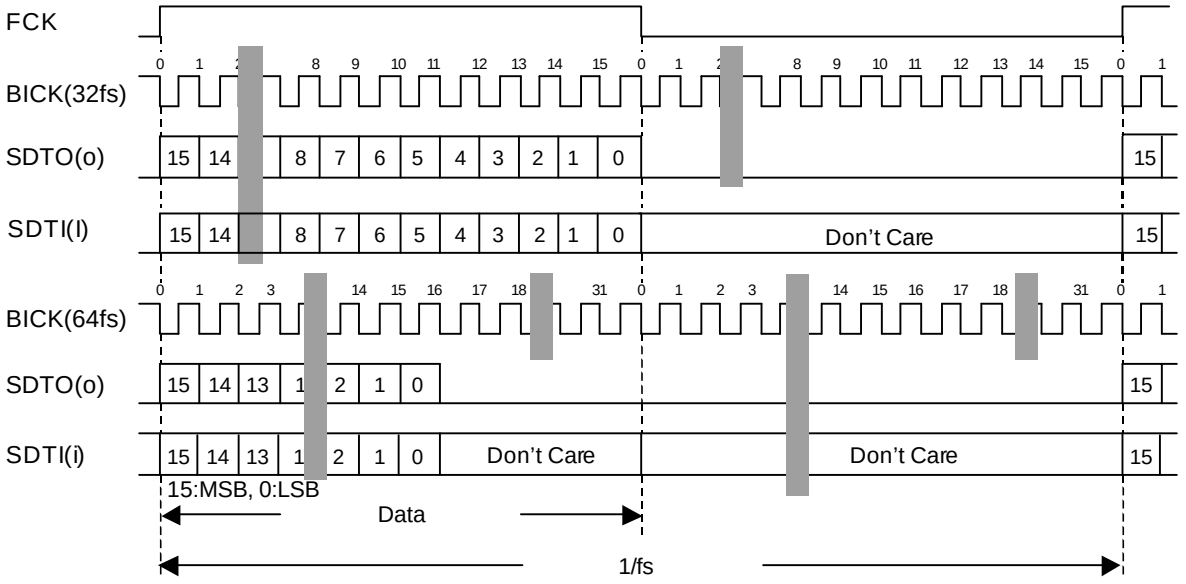


Figure 26. Mode 2 Timing

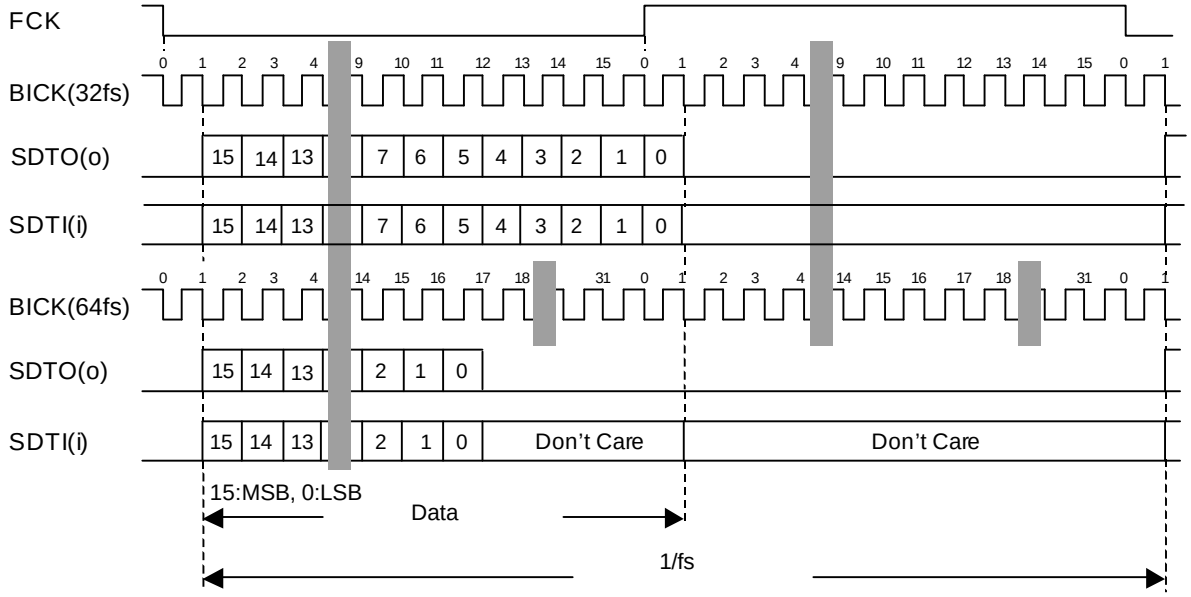


Figure 27. Mode 3 Timing

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.25Hz (@fs=8kHz) and scales with sampling rate (fs).

■ MIC Gain Amplifier

AK4536 has a Gain Amplifier for Microphone input. This gain is 0dB or 20dB, selected by the MGAIN bit. The typical input impedance is 30kΩ.

MGAIN bit	Input Gain	
0	0dB	
1	+20dB	Default

Table 14. Input Gain

■ MIC Power

The MPI pin supplies power for the Microphone. This output voltage is typically 0.75 x AVDD and the maximum output current is 1.25mA.

■ Manual Mode

The AK4536 becomes a manual mode at ALC1 bit = “0”. This mode is used in the case shown below.

1. After exiting reset state, set up the registers for the ALC1 operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC1 operation (Limiter period, Recovery period and etc) are changed. For example; When the change of the sampling frequency.
3. When IPGA is used as a manual volume.

■ MIC-ALC Operation

The ALC (Automatic Level Control) of MIC input is done by ALC1 block when ALC1 bit is “1”.

[1] ALC1 Limiter Operation

When the ALC1 limiter is enabled, and IPGA output exceeds the ALC1 limiter detection level (LMTH), the IPGA value is attenuated by the amount defined in the ALC1 limiter ATT step (LMAT1-0 bits) automatically.

When the ZELM bit = “1”, the timeout period is set by the LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. If the ALC1 bit does not change into “0” after completing the attenuation, the attenuation operation repeats while the input signal level equals or exceeds LMTH.

When the ZELM bit = “0”, the timeout period is set by the ZTM1-0 bits. This enables the zero-crossing attenuation function so that the IPGA value is attenuated at the zero-detect points of the waveform.

[2] ALC1 Recovery Operation

The ALC1 recovery refers to the amount of time that the AK4536 will allow a signal to exceed a predetermined limiting value prior to enabling the limiting function. The ALC1 recovery operation uses the WTM1-0 bits to define the wait period used after completing an ALC1 limiter operation. If the input signal does not exceed the “ALC1 Recovery Waiting Counter Reset Level”, the ALC1 recovery operation starts. The IPGA value increases automatically during this operation up to the reference level (REF6-0 bits). The ALC1 recovery operation is done at a period set by the WTM1-0 bits. Zero crossing is detected during WTM1-0 period, the ALC1 recovery operation waits WTM1-0 period and the next recovery operation starts.

During the ALC1 recovery operation, when input signal level exceeds the ALC1 limiter detection level (LMTH), the ALC1 recovery operation changes immediately into an ALC1 limiter operation.
In the case of “(Recovery waiting counter reset level) ≤ IPGA Output Level < Limiter detection level” during the ALC1 recovery operation, the wait timer for the ALC1 recovery operation is reset. Therefore, in the case of “(Recovery waiting counter reset level) > IPGA Output Level”, the wait timer for the ALC1 recovery operation starts.

The ALC1 operation corresponds to the impulse noise. When the impulse noise is input, the ALC1 recovery operation becomes faster than a normal recovery operation.

[3] Example of ALC1 Operation

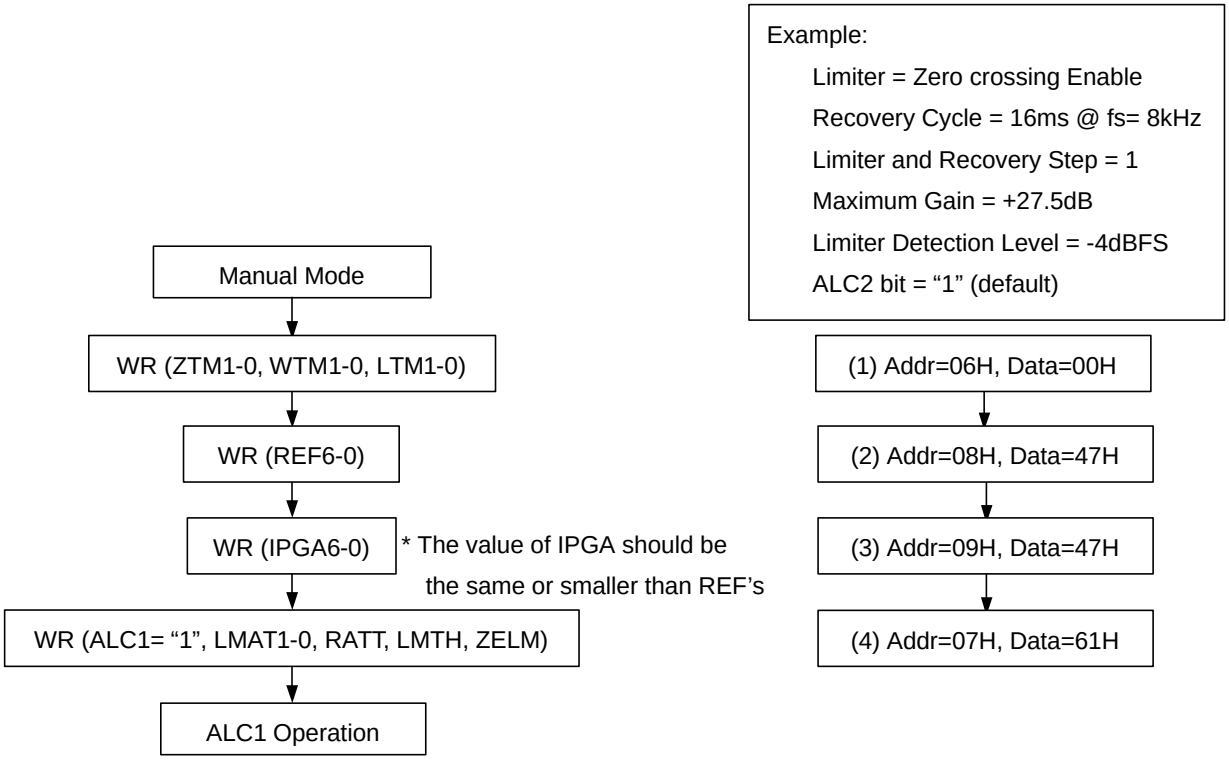
Table 15 shows the examples of the ALC1 setting.

Register Name	Comment	fs=8kHz		fs=16kHz	
		Data	Operation	Data	Operation
LMTH	Limiter detection Level	1	-4dBFS	1	-4dBFS
LTM1-0	Limiter operation period at ZELM = 1	00	Don't use	00	Don't use
ZELM	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	16ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	16ms	01	16ms
REF6-0	Maximum gain at recovery operation	47H	+27.5dB	47H	+27.5dB
IPGA6-0	Gain of IPGA	47H	+27.5dB	47H	+27.5dB
LMAT1-0	Limiter ATT Step	00	1 step	00	1 step
RATT	Recovery GAIN Step	0	1 step	0	1 step
ALC1	ALC1 Enable bit	1	Enable	1	Enable

Table 15. Examples of the ALC1 Setting

The following registers should not be changed during the ALC1 operation. These bits should be changed, after the ALC1 operation is finished by ALC1 bit = "0" or PMMIN bit = "0".

- **LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELM bits**



Note : WR : Write

Figure 28. Registers set-up sequence at the ALC1 operation

■ Digital Output Volume

The AK4536 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVOL7-0 bits. The volume is included in front of a DAC block, a input data of DAC is changed from +12 to –115dB with MUTE. This volume has a soft transition function. It takes 1061/fs (=133ms @ fs = 8kHz) from 00H to FFH.

DVOL7-0	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
•	•	
18H	0dB	Default
•	•	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 16. Digital Output Volume Code Table

■ BEEP Input

When the PMBP bit is set to “1”, the beep input is powered-up. And when the BEEPS bit is set to “1”, the input signal from the BEEP pin is output to Speaker-Amp. When the BEEPA bit is set to “1”, the input signal from the BEEP pin is output to the mono line output amplifier. The external resister Ri adjusts the signal level of BEEP input. The internal feedback resistance is 20k ± 30%Ω.

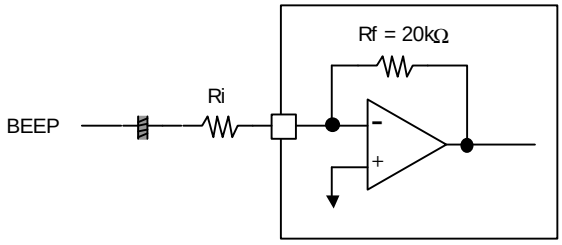


Figure 7. Block Diagram of BEEP pin

■ Speaker Output

The output signal from DAC is input to the Speaker-amp via the ALC2 circuit. This Speaker-amp is a mono output controlled by BTL and a gain of the Speaker-Amp is set by SPKG bit. When SPKG bit is "0", output power is a maximum of 150mW@8Ω and SVDD = 3.3V. When SPKG bit is "1", output power is a maximum of 250mW@8Ω and SVDD = 3.3V.

Speaker blocks (MOUT, ALC2 and Speaker-amp) can be powered-up/down by controlling the PMSPK bit. When the PMSPK bit is "0", the MOUT, SPP and SPN pins are placed in a Hi-Z state.

When the PMSPK bit is "1" and SPPS bit is "0", the Speaker-amp enters power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. And then the Speaker output gradually changes to the SVDD/2 voltage and this mode can reduce pop noise at power-up. When the AK4536 is powered-down, pop noise can be also reduced by first entering power-save-mode.

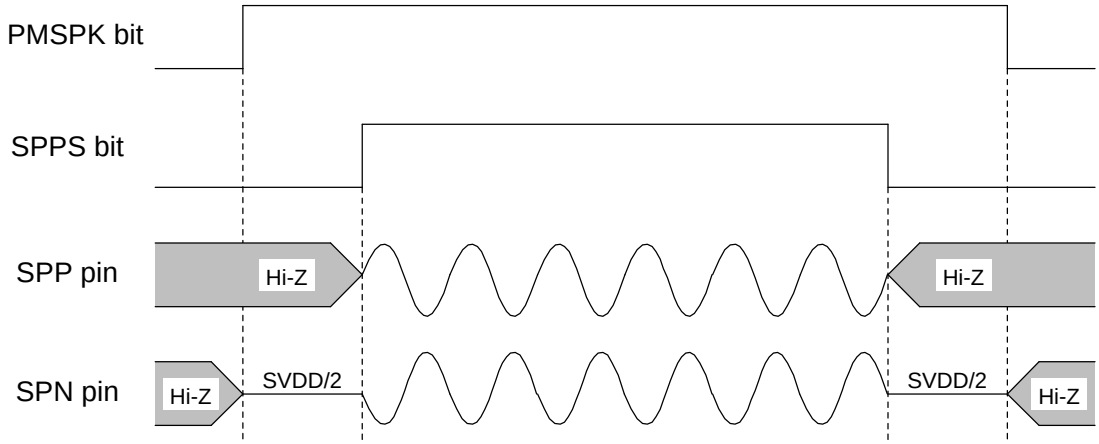


Figure 29. Power-up/Power-down Timing for Speaker-Amp

■ MONO LINE OUTPUT (AOUT pin)

A signal of DAC is output from AOUT pin. When the DACA bi is "0", this output is OFF and the AOUT pin is forced to VCOM voltage. The load resistance is 10kΩ(min). When PMAO bit is "0", the mono line output enters power-down and the output is placed in a Hi-Z state.

■ SPK-ALC Operation

The ALC (Automatic Level Control) operation of speaker output is done by ALC2 block when ALC2 bit is "1". Input resistance of the ALC2 is 24kΩ (typ) and centered around VCOM voltage. The ALC2 level diagram is shown in Figure 30.

The limiter detection level is proportional to SVDD voltage. The output level is limited by the ALC2 circuit when the input signal exceeds –5.2dBV (=FS-2.1dB@AVDD=SVDD=3.3V). When a continuous signal of –5.2dBV or greater is input to the ALC2 circuit, the change period of the ALC2 limiter operation is 250μs (=2/fs@fs=8kHz) and the attenuation level is 0.5dB/step.

The ALC2 recovery operation uses zero crossings and gains of 1dB/step. The ALC2 recovery operation is done until the input level of the Speaker-amp goes to –7.2dBV(=FS-4.1dB@AVDD=SVDD=3.3V). **Maximum gain of the ALC2 recovery operation is +18dB.**

When the input signal is between –5.2dBV and –7.2dBV, the ALC2 limiter or recovery operations are not done.

When the PMSPK bit changes from "0" to "1", the initilization cycle (512/fs = 64ms @fs=8kHz at ROTM bit = "0") starts. The ALC2 is disabled during the initilization cycle and the ALC2 starts after completing the initilization cycle. The ROTM bit is set during the PMSPK bit = "0".

When the ALC2 is disable, a gain of the ALC2 block is fixed to –2dB. Therefore, a gain of internal speaker block is +4dB (Full-differential output) at SPKG bit = "0", and it is +6.24dB (Full-differential output) at SPKG bit = "1".

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		–5.2dBV	–7.2dBV
Period	fs=8kHz	2/fs = 250μs	512/fs=64ms
	fs=16kHz	2/fs = 125μs	512/fs=32ms
Zero-crossing Detection		No	Yes (Timeout = Period Time)
ATT/GAIN		0.5dB step	1dB step

Table 17. Limiter /Recovery of ALC2 (ROTM bit = "0")

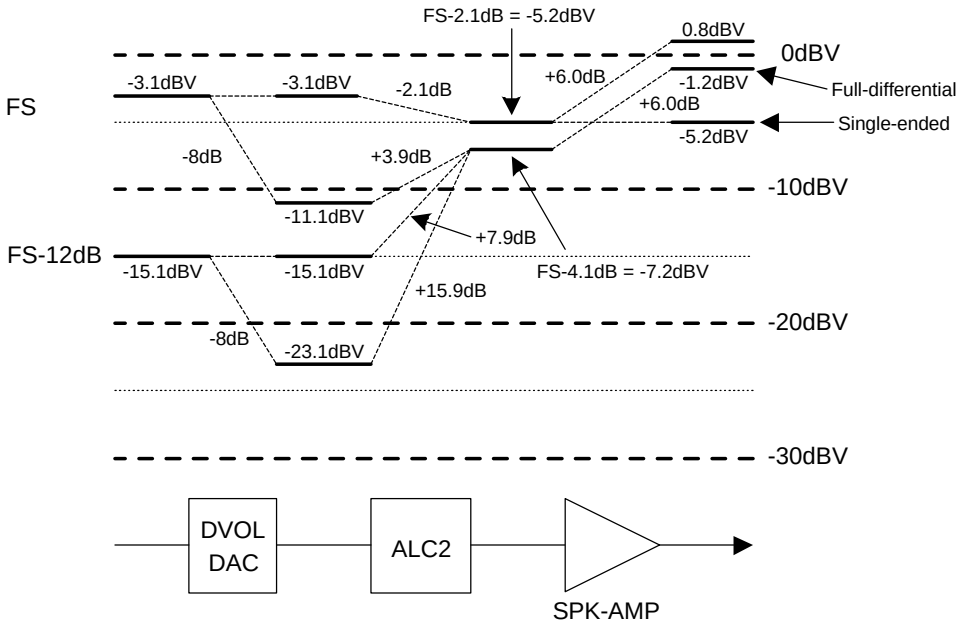
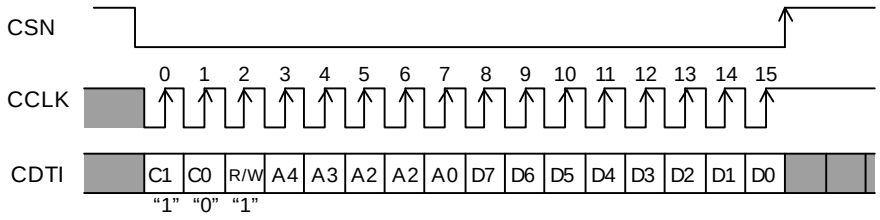


Figure 30. Speaker-Amp Output Level Diagram (SVDD=3.3V, DVOL=–8.0dB, SPKG bit = "0")
* FS = Full Scale

■ Serial Control Interface

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address (Fixed to "10"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = "L".



C1-C2: Chip Address (C1 = "1", C0 = "0"); Fixed to "10"
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0: Register Address
D7-D0: Control data

Figure 31. Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMAO	PMDAC	PMMIC	PMADC
01H	Power Management 2	0	0	0	0	M/S	MCKPD	PMXTL	PMPLL
02H	Signal Select 1	SPPS	BEEPS	ALC2S	DACA	DACM	MPWR	MICAD	MGAIN
03H	Signal Select 2	0	0	0	0	SPKG	BEEPA	ALC1M	ALC1A
04H	Mode Control 1	0	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
05H	Mode Control 2	0	0	0	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	0	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
07H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
08H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
0AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0

The PDN = “L” resets the registers to their default values.

Note: Unused bits must contain a “0” value.
Note: Only write to address 00H to 0AH.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMAO	PMDAC	PMMIC	PMADC
Default		0	0	0	0	0	0	0	0

PMADC: ADC Block Power Control
0: Power down (Default)
1: Power up
When the PMADC bit changes from "0" to "1", the initialization cycle (1059/fs=133ms@8kHz) starts. After initializing, digital data of the ADC is output.

PMMIC: MIC In Block (MIC-Amp and ALC1) Power Control
0: Power down (Default)
1: Power up

PMDAC: DAC Block Power Control
0: Power down (Default)
1: Power up

PMAO: Mono Line Out Power Control
0: Power down (Default)
1: Power up

PMSPK: Speaker Block Power Control
0: Power down (Default)
1: Power up

PMBP: BEEP In Power Control
0: Power down (Default)
1: Power up

PMVCM: VCOM Block Power Control
0: Power down (Default)
1: Power up

Each block can be powered-down respectively by writing "0" in each bit. When the PDN pin is "L", all blocks are powered-down.

When PMPLL and PMXTL bits and all bits in 00H address are "0", all blocks are powered-down. The register values remain unchanged.

When any of the blocks are powered-up, the PMVCM bit must be set to "1". When PMPLL and PMXTL bits and all bits in 00H address are "0", PMVCM bit can write to "0".

When BEEP signal is output from Speaker-Amp (Signal path: BEEP pin → SPP/SPN pins) or Mono Lineout-Amp (Signal path: BEEP pin → AOUT pin) only, the clocks may not be present. When ADC, DAC, ALC1 or ALC2 is in operation, the clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	M/S	MCKPD	PMXTL	PMPLL
Default		0	0	0	0	0	1	0	0

PMPLL: PLL Block Power Control Select
0: PLL is Power down and External is selected. (Default)
1: PLL is Power up and PLL Mode is selected.

PMXTL: X'tal Oscillation Block Power Control
0: Power down (Default)
1: Power up

MCKPD: MCKI pin pull down control
0: Master Clock input enable
1: Pull down by 25kΩ (Default)

M/S: Select Master / Slave Mode
0: Slave Mode (Default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPS	BEEPS	ALC2S	DACA	DACM	MPWR	MICAD	MGAIN
Default		0	0	0	0	0	0	0	1

MGAIN: 1st MIC-amp Gain control

0: 0dB

1: +20dB (Default)

MICAD: Switch Control from MIC In to ADC.

0: OFF (Default)

1: ON

When MICAD bit is "1", the ALC1 output signal is input to ADC.

MPWR: Power Supply Control for Microphone

0: OFF (Default)

1: ON

When PMMIC bit is "1", MPWR bit is enabled.

DACM: Switch Control from DAC to mono amp.

0: OFF (Default)

1: ON

When PMSPK bit is "1", DACM bit is enabled. When PMSPK bit is "0", MOUT pin is Hi-Z state.

DACA: Switch Control from DAC to mono line amp

0: OFF (Default)

1: ON

When PMAO bit is "1", DACA bit is enabled. When PMAO bit is "0", the AOUT pin goes Hi-Z state.

ALC2S: ALC2 output to Speaker-Amp Enable

0: OFF (Default)

1: ON

When ALC2S bit is "1", the ALC2 output signal is input to Speaker-Amp.

BEEPS: BEEP pin to Speaker-Amp Enable

0: OFF (Default)

1: ON

When BEEPS bit is "1", the beep signal is input to Speaker-Amp.

SPPS: Speaker-amp Power-Save-Mode

0: Power Save Mode (Default)

1: Normal Operation

When SPPS bit is "1", the Speaker-amp is in power-save-mode and the SPP pin becomes Hi-z and SPN pin is set to SVDD/2 voltage. When the PMSPK bit = "1", this bit is valid. After the PDN pin changes from "L" to "H", the PMSPK bit is "0", which powers down Speaker-amp.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	0	0	0	0	SPKG	BEEPA	ALC1M	ALC1A
Default		0	0	0	0	0	0	0	0

ALC1A: Switch Control from ALC1 output signal to mono line output amp.
0: OFF (Default)
1: ON
When PMAO bit is “1”, ALC1A bit is enabled. When PMAO bit is “0”, the AOUT pin goes Hi-Z state.

ALC1M: Switch Control from ALC1 output signal to mono amp.
0: OFF (Default)
1: ON
When PMSPK bit is “1”, ALC1M is enabled. When PMSPK bit is “0”, the MOUT pin goes Hi-Z state.

BEEPA: Switch Control from beep signal to mono line output amp.
0: OFF (Default)
1: ON
When PMAO bit is “1”, BEEPA is enabled. When PMAO bit is “0”, the AOUT pin goes Hi-Z state.

SPKG: Select Speaker-Amp Output Gain
0: 0dB (Default)
1: +2.24dB

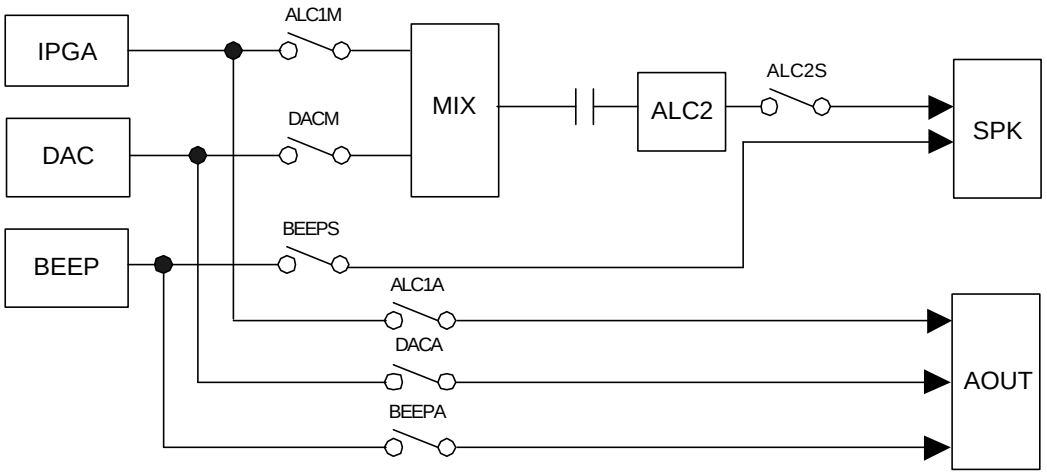


Figure 32. Speaker and Mono Lineout-Amps switch control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	0	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (See Table 18)

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 16fs	Figure 21 Figure 22 Figure 23 Figure 24	
1	0	1	MSB justified	LSB justified	≥ 32fs	Figure 25	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 26	Default
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 27	

Table 18. Audio Interface Format

BCKO1-0: Select BICK frequency (See Table 19)

Mode	BCKO1 bit	BCKO0 bit	BICK Frequency	
0	0	0	16fs	Default
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 19. Output Frequency of BICK at Master Mode

PLL2-0: Select input frequency at PLL mode (See Table 20)

Mode	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input	Input Frequency	
0	0	0	0	FCK pin	1fs	Default
1	0	0	1	BICK pin	16fs	
2	0	1	0	BICK pin	32fs	
3	0	1	1	BICK pin	64fs	
4	1	0	0	MCKI/XTI pin	11.2896MHz	
5	1	0	1	MCKI/XTI pin	12.288MHz	
6	1	1	0	MCKI/XTI pin	12MHz	
7	1	1	1	N/A	N/A	

Table 20. Setting of PLL Mode (*fs: Sampling Frequency)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	0	0	0	MSBS	BCKP	FS2	FS1	FS0
Default		0	0	0	0	0	0	0	0

FS2-0: Setting of Sampling Frequency (See Table 21 and Table 22) and MCKI Frequency (See Table 23)
These bits are selected to sampling frequency at PLL mode and MCKI frequency at EXT mode.

Mode	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	8kHz	Default
1	0	0	1	12kHz	
2	0	1	0	16kHz	
3	0	1	1	24kHz	
4	1	0	0	N/A	
5	1	0	1	11.025kHz	
6	1	1	0	N/A	
7	1	1	1	22.05kHz	

Table 21. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL = "1"

Mode	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	7.35kHz ≤ fs ≤ 10kHz	Default
1	0	1	10kHz < fs ≤ 14kHz	
2	1	0	14kHz < fs ≤ 20kHz	
3	1	1	20kHz < fs ≤ 26kHz	

Table 22. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL = "1"
*** FS2 bit is ignored.**

Mode	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	7.35kHz ~ 26kHz	Default
1	0	1	1024fs	7.35kHz ~ 13kHz	
2	1	0	256fs	7.35kHz ~ 26kHz	
3	1	1	512fs	7.35kHz ~ 26kHz	

Table 23. MCKI Frequency at EXT, Slave Mode (PMPLL bit = "0", M/S bit = "0")
*** FS2 bit is ignored.**

BCKP, MSBS: "00" (Default) (See Table 26)

MSBS bit	BCKP bit	Data Input/Output Timing	
0	0	Figure 21	Default
0	1	Figure 23	
1	0	Figure 22	
1	1	Figure 24	

Table 24. Relation between MSBS, BCKP bits and data I/O timing

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	0	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
Default		0	0	0	0	0	0	0	0

LTM1-0: ALC1 limiter operation period at zero crossing disable (ZELM bit = "1") (see Table 25)

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by the LTM1-0 bits. Default is "00" (0.5/fs).

LTM1 bit	LTM0 bit		ALC1 Limiter Operation Period		
			8kHz	16kHz	
0	0	0.5/fs	63μs	31μs	Default
0	1	1/fs	125μs	63μs	
1	0	2/fs	250μs	125μs	
1	1	4/fs	500μs	250μs	

Table 25. ALC1 Limiter Operation Period at zero crossing disable (ZELM bit="1")

WTM1-0: ALC1 Recovery Waiting Period (see Table 26)

A period of recovery operation when any limiter operation does not occur during the ALC1 operation. Default is "00" (128/fs).

WTM1 bit	WTM0 bit		ALC1 Recovery Operation Waiting Period		
			8kHz	16kHz	
0	0	128/fs	16ms	8ms	Default
0	1	256/fs	32ms	16ms	
1	0	512/fs	64ms	32ms	
1	1	1024/fs	128ms	64ms	

Table 26. ALC1 Recovery Operation Waiting Period

ZTM1-0: ALC1 Zero crossing timeout Period (see Table 27)

When the IPGA perform zero crossing or timeout, the IPGA value is changed by the μP WRITE operation, ALC1 recovery operation or ALC1 limiter operation (ZELM bit = "0"). Default is "00" (128/fs).

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period		
			8kHz	16kHz	
0	0	128/fs	16ms	8ms	Default
0	1	256/fs	32ms	16ms	
1	0	512/fs	64ms	32ms	
1	1	1024/fs	128ms	64ms	

Table 27. Zero Crossing Timeout Period

ROTM: Period time for ALC2 Recovery operation, ALC2 Zero Crossing Timeout and ALC2 initializing cycle.

0: 512/fs (Default)

1: 1024/fs

The ROTM bit is set during the PMSPK bit = "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
Default		0	1	0	0	0	0	0	0

LMTH: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level (see Table 28)

The ALC1 limiter detection level and the ALC1 recovery counter reset level may be offset by about ±2dB. Default is "0".

LMTH bit	ALC1 Limiter Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	ADC Input ≥ −6.0dBFS	−6.0dBFS > ADC Input ≥ −8.0dBFS	Default
1	ADC Input ≥ −4.0dBFS	−4.0dBFS > ADC Input ≥ −6.0dBFS	

Table 28. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC1 Recovery GAIN Step (see Table 29)

During the ALC1 recovery operation, the number of steps changed from the current IPGA value is set. For example, when the current IPGA value is 30H and RATT bit = "1" is set, the IPGA changes to 32H by the ALC1 recovery operation and the output signal level is gained up by 1dB (=0.5dB x 2). When the IPGA value exceeds the reference level (REF6-0 bits), the IPGA value does not increase.

RATT bit	GAIN STEP	
0	1	Default
1	2	

Table 29. ALC1 Recovery Gain Step Setting

LMAT1-0: ALC1 Limiter ATT Step (see Table 30)

During the ALC1 limiter operation, when IPGA output signal exceeds the ALC1 limiter detection level set by LMTH, the number of steps attenuated from the current IPGA value is set. For example, when the current IPGA value is 47H and the LMAT1-0 bits = "11", the IPGA transition to 43H when the ALC1 limiter operation starts, resulting in the input signal level being attenuated by 2dB (=0.5dB x 4). When the attenuation value exceeds IPGA = "00" (−8dB), it clips to "00".

LMAT1 bit	LMAT0 bit	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 30. ALC1 Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC1 Limiter operation

0: Enable (Default)

1: Disable

When the ZELM bit = "0", the IPGA of each L/R channel perform a zero crossing or timeout independently and the IPGA value is changed by the ALC1 operation. The zero crossing timeout is the same as the ALC1 recovery operation. When the ZELM bit = "1", the IPGA value is changed immediately.

ALC1: ALC1 Enable Flag
0: ALC1 Disable (Default)
1: ALC1 Enable

When ALC1 bit is “1”, the ALC1 operation is enabled.

ALC2: ALC2 Enable Flag
0: ALC2 Disable
1: ALC2 Enable (Default)

After completing the initializing cycle (512/fs = 64ms @fs=8kHz at ROTM bit = “0”), the ALC2 operation is enabled. When the PMSPK bit changes from “0” to “1” or PDN pin changes from “L” to “H”, the initilization cycle starts.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		0	0	1	1	0	1	1	0

REF6-0: Reference value at ALC1 Recovery Operation (see Table 31)

During the ALC1 recovery operation, if the IPGA value exceeds the setting reference value by gain operation, then the IPGA does not become larger than the reference value. For example, when REF7-0 = "30H", RATT = 2step, IPGA = 2FH, even if the input signal does not exceed the "ALC1 Recovery Waiting Counter Reset Level", the IPGA does not change to 2FH + 2step = 31H, and keeps 30H. Default is "36H".

DATA (HEX)	GAIN (dB)	STEP	
47	+27.5		
46	+27.0		
45	+26.5		
•	•		
36	+19.0		Default
•	•		
10	+0.0		
•	•	0.5dB	
06	–5.0		
05	–5.5		
04	–6.0		
03	–6.5		
02	–7.0		
01	–7.5		
00	–8.0		

Table 31. Setting Reference Value at ALC1 Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
Default		0	0	0	1	0	0	0	0

IPGA6-0: Input Analog PGA (see Table 32)

Default: "10H" (0dB)

During the ALC1 operation, the writing value in IPGA6-0 bits is ignored.

In a manual mode, IPGA can be set to any values in Table 32.The ZTM1-0 bits set zero crossing timeout period when IPGA value is changed. When the control register is written from the μP, the zero crossing counter is reset and its counter starts. When the signal zero crossing or zero crossing timeout, the written value from the μP becomes valid.

DATA (HEX)	GAIN (dB)	STEP	
47	+27.5	0.5dB	
46	+27.0		
45	+26.5		
•	•		
36	+19.0		
•	•		
10	+0.0		Default
•	•		
06	–5.0		
05	–5.5		
04	–6.0		
03	–6.5		
02	–7.0		
01	–7.5		
00	–8.0		

Table 32. Input Gain Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
Default		0	0	0	1	1	0	0	0

DVOL7-0: Output Digital Volume (see Table 33)

The AK4536 has a digital output volume (256 levels, 0.5dB step, Mute). The gain can be set by the DVOL7-0 bits. The volume is included in front of a DAC block, a input data of DAC is changed from +12 to –115dB with MUTE. This volume has a soft transition function. It takes 1061/fs (=133ms @ fs = 8kHz) from 00H to FFH.

DVOL7-0	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
•	•	
18H	0dB	Default
•	•	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 33. Digital Volume Code Table

SYSTEM DESIGN

Figure 33 shows the system connection diagram. An evaluation board [AKD4536] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

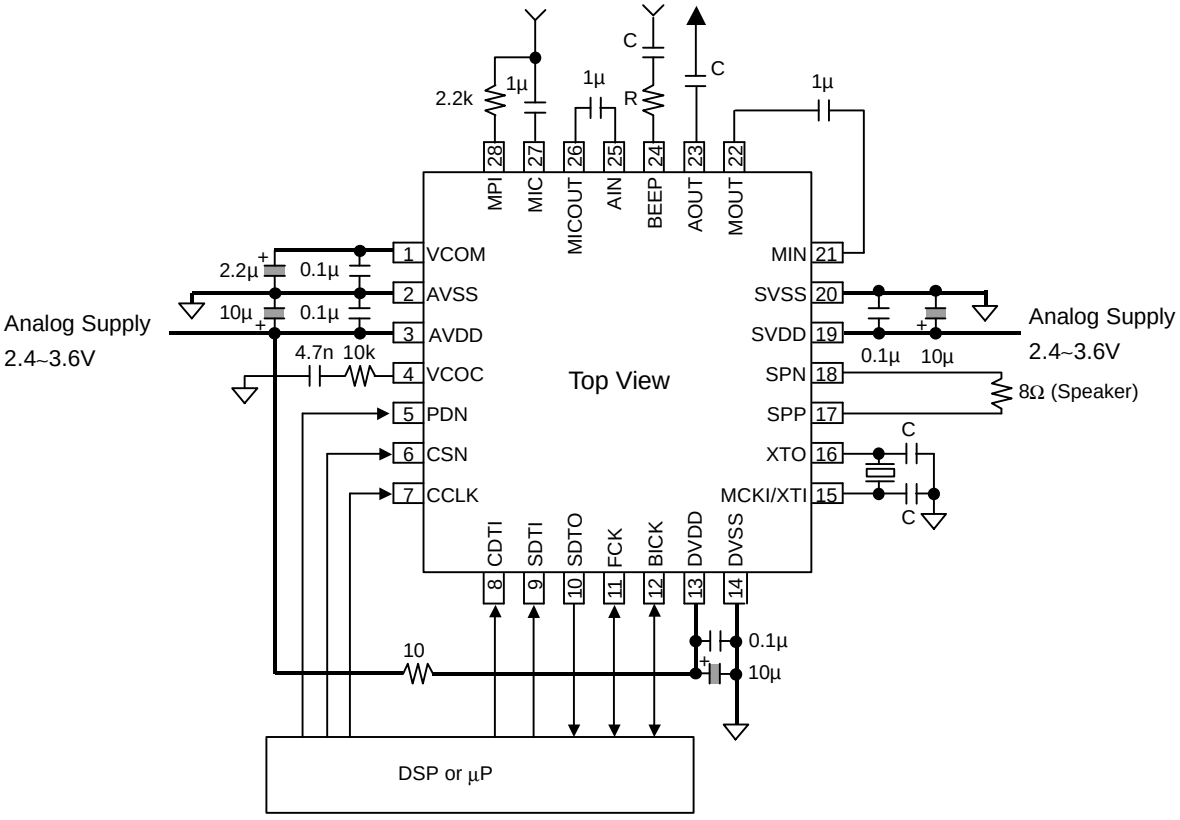


Figure 33. Typical Connection Diagram

Notes:
- AVSS, DVSS and SVSS of the AK4536 should be distributed separately from the ground of external controllers.
- All digital input pins except pull-down pin should not be left floating.
- Value of R and C in Figure 33 should depend on system.
- When the AK4536 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4536 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 34.

Mode	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	Rp and Cp of VCOC pin	
						Rp[Ω]	Cp[F]
0	0	0	0	FCK pin	1fs	10k	470n
1	0	0	1	BICK pin	16fs	10k	4.7n
2	0	1	0	BICK pin	32fs	10k	4.7n
3	0	1	1	BICK pin	64fs	10k	4.7n
4	1	0	0	MCKI/XTI pin	11.2896MHz	10k	4.7n
5	1	0	1	MCKI/XTI pin	12.288MHz	10k	4.7n
6	1	1	0	MCKI/XTI pin	12MHz	10k	4.7n
7	1	1	1	N/A	N/A	-	-

Table 34. Setting of PLL Mode (*fs: Sampling Frequency)

1. Grounding and Power Supply Decoupling

The AK4534 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and SVDD are usually supplied from the system's analog supply. If AVDD, DVDD and SVDD are supplied separately, the correct power up sequence should be observed. AVSS, DVSS and SVSS of the AK4536 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4536 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4536.

3. Analog Inputs

The Mic and Beep inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp for the Mic input and 0.6 x AVDD Vpp for the Beep input, centered around the internal common voltage (approx. 0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = (1/2\pi RC)$. The AK4536 can accept input voltages from AVSS to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Mono output from the MOUT pin and Mono Line Output from the AOUT pin are centered at 0.45 x AVDD (typ). The Speaker-Amp output is centered at SVDD/2.

CONTROL SEQUENCE

■ Clock Set up

When ADC, DAC, ALC1 and ALC2 are used, the clocks must be supplied.

1. When X'tal is used in PLL & Master mode.

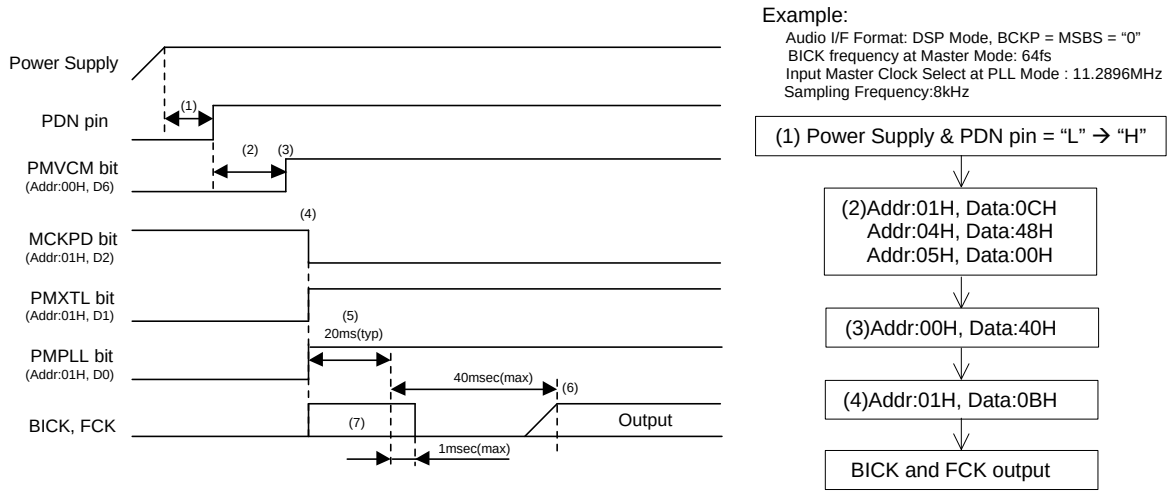


Figure 34. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4536.

(2) DIF1-0, PLL2-0, FS2-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.

(3) Power UpVCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Release the pulled-down of the XTI pin: MCKPD bit = "1" → "0"
Power Up X'tal: PMXTL bit = "0" → "1"
Power Up the PLL: PMPLL bit = "0" → "1"

(5) It takes X'tal oscillator 20ms(typ) to be stable after PMXTL bit="1". This time depends on X'tal. PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1".

(6) The AK4536 starts to output the FCK and BICK clocks after the PLL becomes stable. The normal operation of the block which a clock is necessary for becomes possible.

(7) The irregular frequencies are output from FCK and BICK pins in this section.

2. When an external master clock is used in PLL & Master mode.

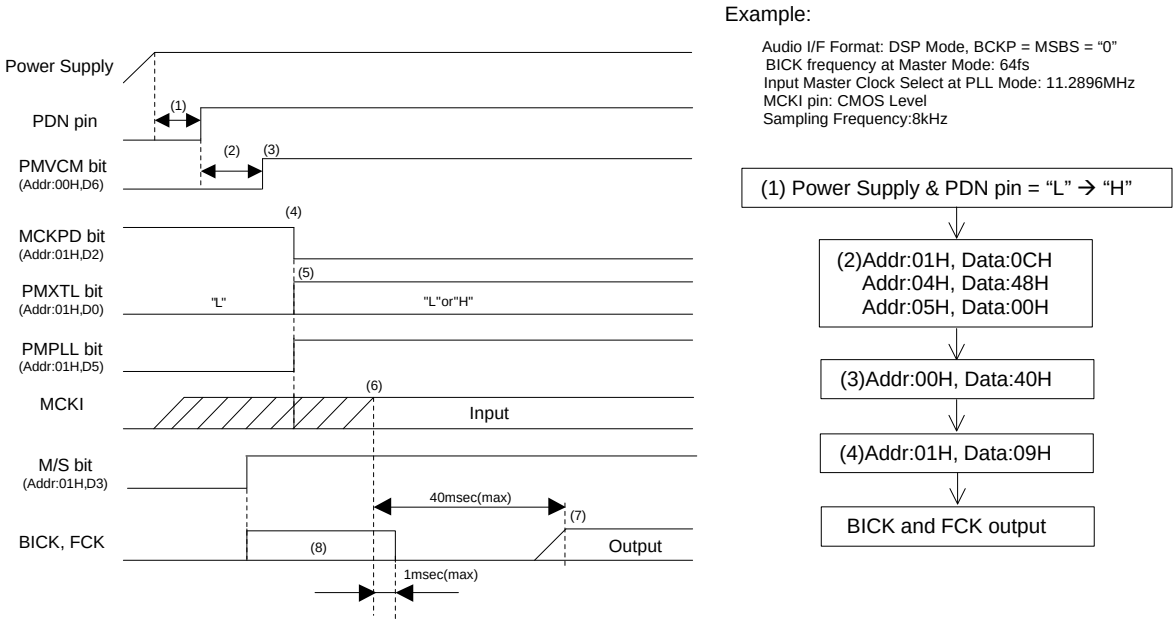


Figure 35. Clock Set Up Sequence (2)

<Example>

(1) After Power Up, PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4536.

(2) DIF1-0, PLL2-0, FS2-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Release the pulled-down of the XTI pin: MCKPD bit = "1" → "0"
Power Down X'al: PMXTL bit = "0"

(5) When MCKI pin is input by AC coupling: PMXTL bit = "1"
When MCKI pin is input by CMOS Level: PMXTL bit = "0"

(6) When PMPLL bit changes from "0" to "1", the PLL starts after the clocks is supplied to MCKI pin. The PLL lock time is 40ms(max).

(7) The AK4536 starts to output the FCK and BICK clocks after the PLL becomes stable. The normal operation of the block which a clock is necessary for becomes possible.

(8) The irregular frequencies are output from FCK and BICK pins in this section.

3. When the external clocks (FCK and BICK pins) is used in PLL & Slave mode.

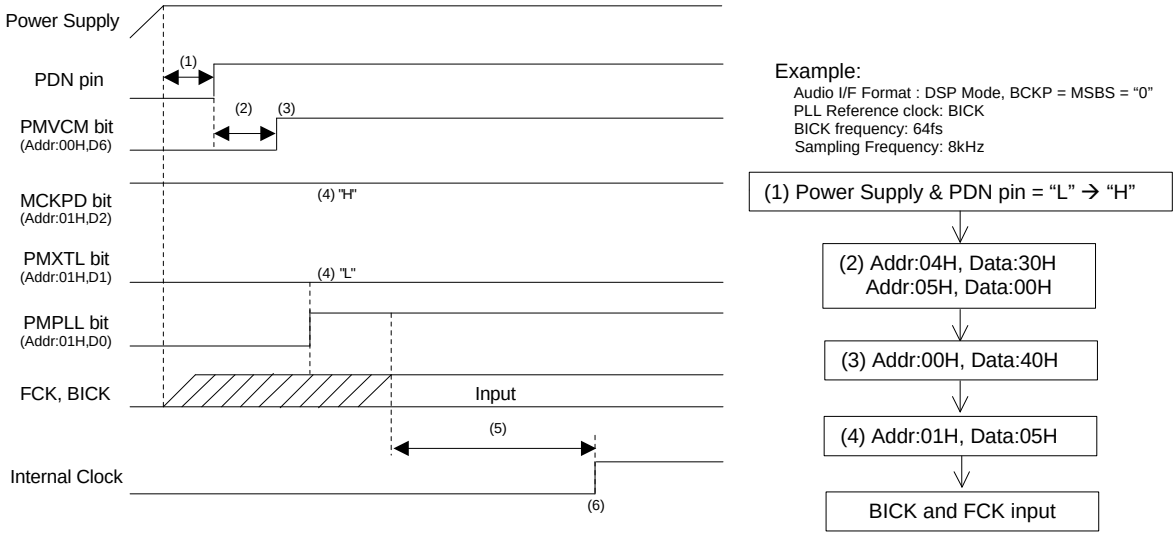


Figure 36. Clock Set Up Sequence (3)

<Example>

(1) After Power Up, PDN pin "L" → "H"
"L" time(1) of 150ns or more is needed to reset the AK4536.

(2) DIF1-0, FS2-0, PLL2-0, MSBS and BCKP bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Pull down the XTI pin: MCKPD bit = "1"
Power Down X'tal: PMXTL bit = "0"

(5) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (FCK or BICK pin) is supplied. PLL lock time is 160ms(max) when FCK is a PLL reference clock. And PLL lock time is 2ms(max) when BICK is a PLL reference clock.

(6) The AK4536 starts to output the FCK and BICK clocks after the PLL becomes stable. The normal operation of the block which a clock is necessary for becomes possible.

4. EXT mode (Slave mode)

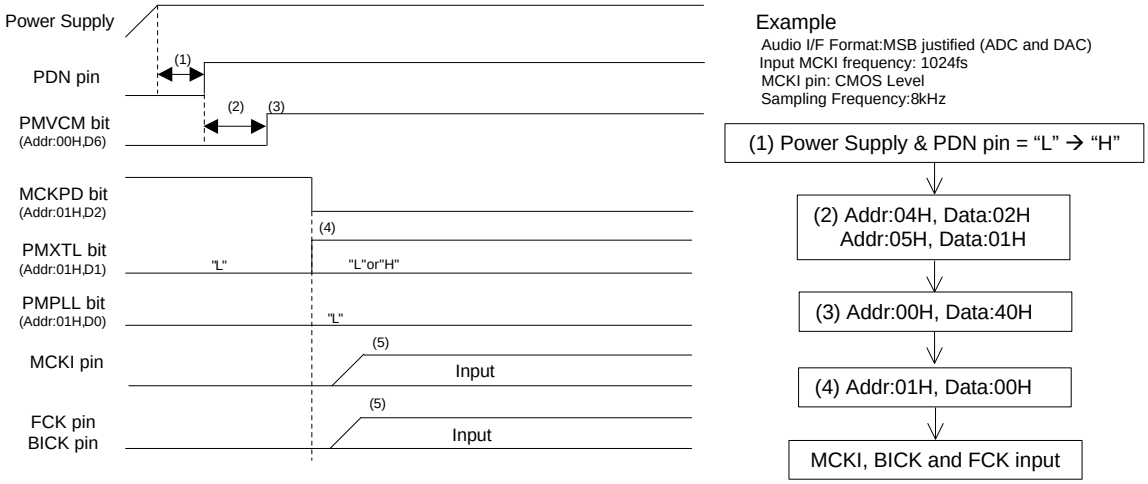


Figure 37. Clock Set Up Sequence (4)

<Example>

(1) After Power Up, PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4536.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Release the pulled-down of the XTI pin: MCKPD bit = "1" → "0"
Power down PLL: PMPLL bit = "0"
When MCKI pin is input by AC coupling: PMXTL bit = "1"
When MCKI pin is input by CMOS Level: PMXTL bit = "0"

(5) After the MCKI, FCK and BICK are supplied, the normal operation of the block which a clock is necessary for becomes possible

■ MIC Input Recording

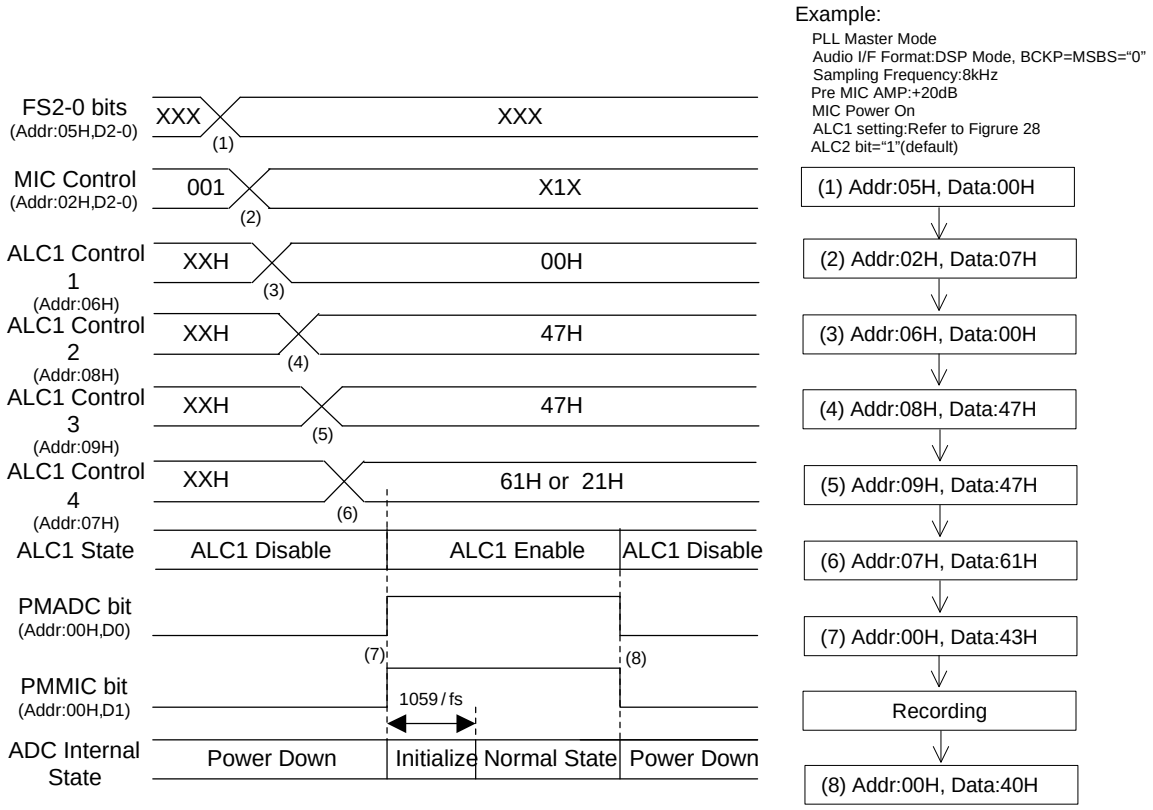


Figure 38. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=8kHz. If the parameter of the ALC1 is changed, please refer to "Figure 28. Register set-up sequence at the ALC1 operation."

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS2-0 bits). When the AK4536 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up MIC input (Addr: 02H)
(3) Set up Timer Select for ALC1 (Addr: 06H)
(4) Set up REF value for ALC1 (Addr: 08H)
(5) Set up IPGA value for ALC1 (Addr: 09H)
(6) Set up LMTH, RATT, LMAT1-0, ALC1 bits (Addr: 07H)
(7) Power Up MIC and ADC: PMMIC bit = PMADC bit = "0" → "1"
The initialization cycle time of ADC is 1059/fs=133ms@fs=8kHz.
After the ALC1 bit is set to "1" and MIC block is powered-up, the ALC1 operation starts.
(8) Power Down MIC and ADC: PMMIC bit = PMADC bit = "1" → "0"
When the registers for the ALC1 operation are not changed, ALC1 bit may be keeping "1". The ALC1 operation is disabled because the MIC block is powered-down. If the registers for the ALC1 operation are also changed when the sampling frequency is changed, it should be done after the AK4536 goes to the manual mode (ALC1 bit = "0") or MIC block is powered-down (PMMIC bit = "0").

■ Speaker-amp Output

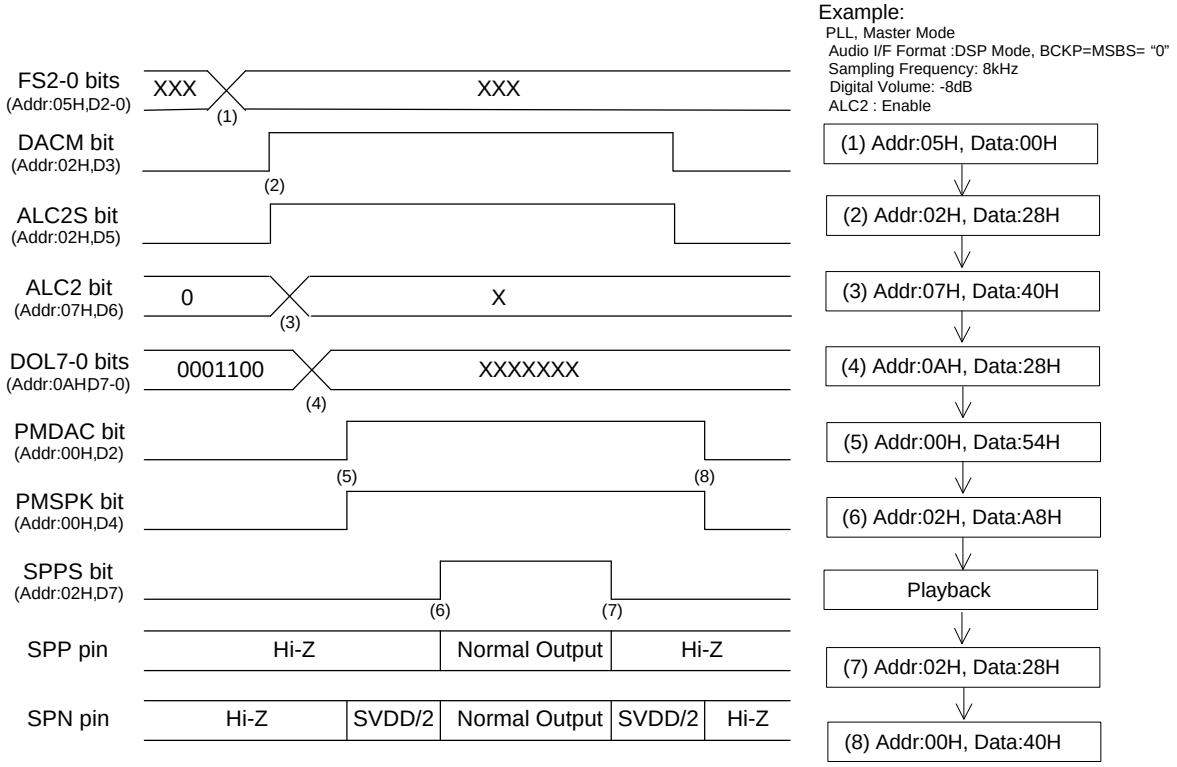


Figure 39. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS2-0 bit). When the AK4536 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → SPK-Amp"
DACM = ALC2S bit: "0" → "1"

(3) Set up the ALC2 Enable/Disable (ALC2 bit)

(4) Set up the digital volume (Addr = 0AH)

(5) Power Up of DAC and Speaker-Amp: PMDAC bit = PMSPK bit = "0" → "1"

(6) Exit the power-save-mode of Speaker-Amp: SPPS bit = "0" → "1"
The initializing time of Speaker amp is 512/fs =64ms (@ fs=8kHz, ROTM bit = "0")

(7) Enter the power-save-mode of Speaker-Amp: SPPS bit = "1" → "0"

(8) Power Down DAC and Speaker-Amp: PMDAC bit = PMSPK bit = "1" → "0"

■ Stop of Clock

Master clock can be stopped when ADC, DAC, ALC1 and ALC2 don't operate.

1. When X'tal is used in PLL & Master mode.

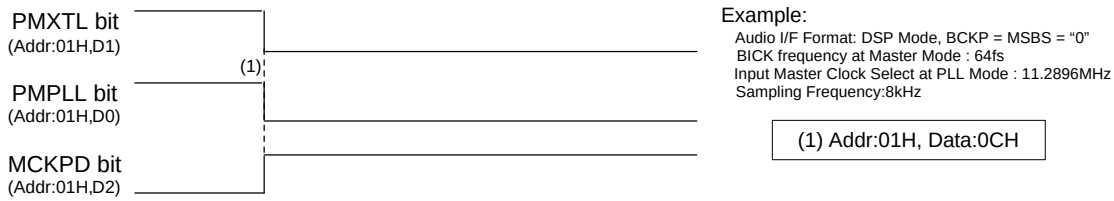


Figure 40. Stop of Clock Sequence (1)

<Example>
(1) Power down X'tal and PLL: PMXTL bit = PMPLL bit = "1" → "0"
Pull down the XTI pin: MCKPD bit = "0" → "1"

2. When an external clock is used in PLL & Master mode

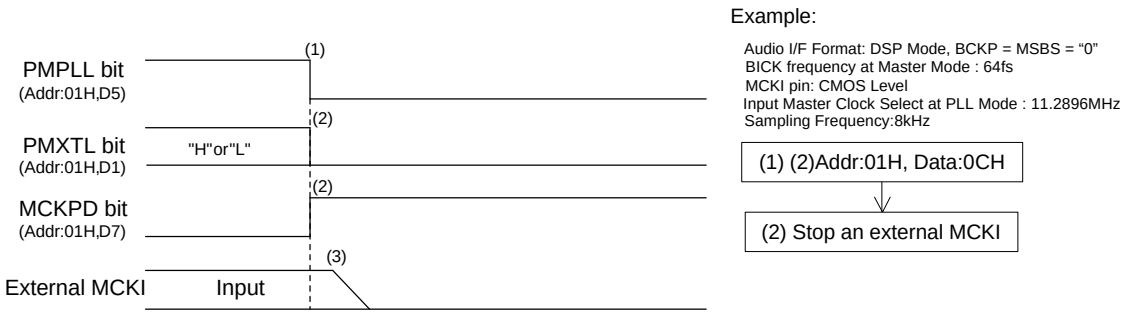


Figure 41. Stop of Clock Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Pull down the MCKI pin: MCKPD bit = "0" → "1"
Power down X'tal: PMXTL bit = "1" → "0"
When the external master clock becomes Hi-Z or the external master clock is input by AC couple, MCKI pin should be pulled down. When the external master clock is input by AC couple, X'tal should be powered-down.
(3) Stop an external master clock

3. PLL & Slave mode

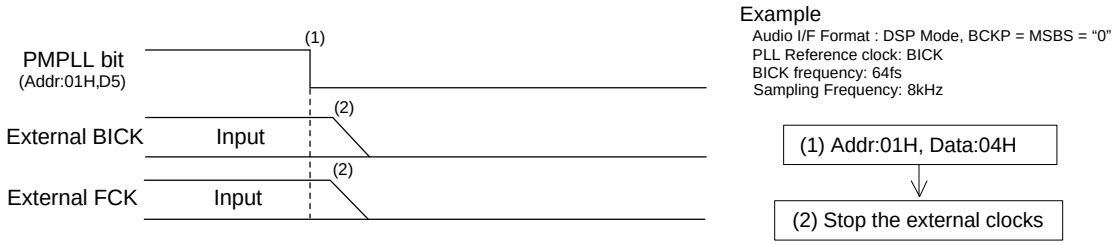


Figure 42. Stop of Clock Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and FCK clocks.

4. EXT mode

Figure 43. Stop of Clock Sequence (4)

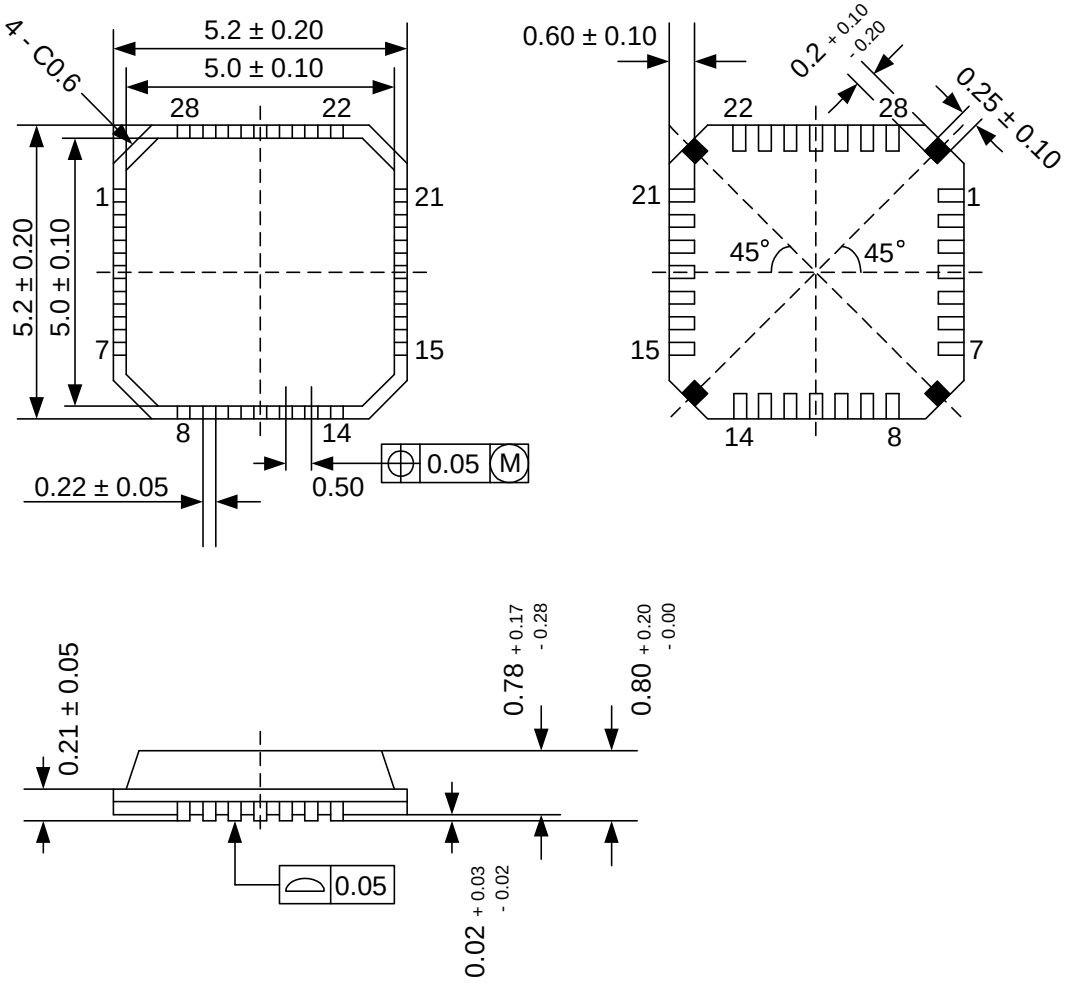
<Example>
(1) Pull down the MCKI pin: MCKPD bit = "0" → "1"
Power down X'tal: PMXTL bit = "1" → "0"
When the external master clock becomes Hi-Z or the external master clock is input by AC couple, MCKI pin should be pulled down. When the external master clock is input by AC couple, X'tal should be powered-down.
(2) Stop the external MCKI, BICK and FCK clocks

■ Power down

Power down VCOM (PMVCM= "1" → "0") after all blocks except VCOM are powered down and a master clock stops. The AK4536 is also powered-down by PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE

● 28pin QFN (Unit: mm)

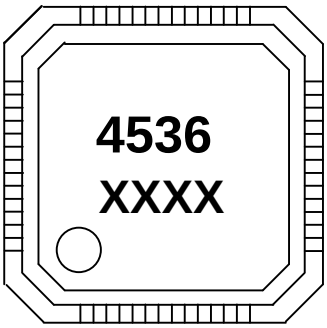


Note) The part of black at four corners on reverse side must not be soldered and must be open.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb free)

MARKING



XXXX : Date code identifier (4 digits)

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  a. A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.