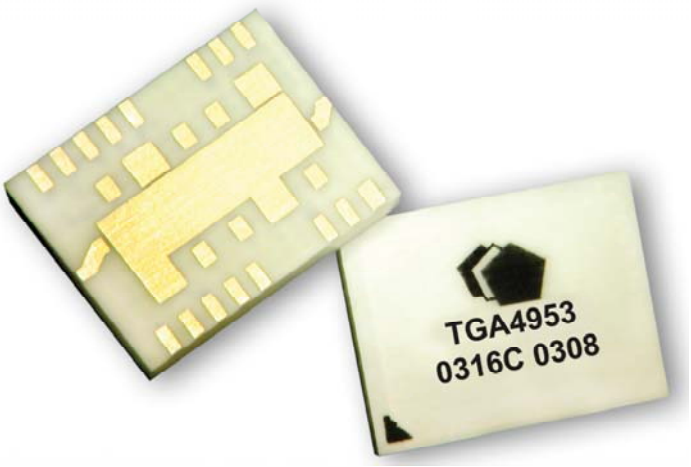
9.9-11.2Gb/s Optical Modulator Driver TGA4953-EPU

OC-192 Metro and Long Haul Applications
Surface Mount Package



Key Features and Performance

- Metro MSA Compatible
- Wide Drive Range (3V to 10V)
- Single-ended Input / Output
- Low Power Dissipation (1W at Vo=6V)
- Very Low Rail Ripple
- 25 ps Edge Rates (20/80)
- Small Form Factor
  - 11.4 x 8.9 x 2 mm
  - 0.450 x 0.350 x 0.080 inches
- Evaluation Board Available.

Description

The TriQuint TGA4953-EPU is part of a series of surface mount modulator drivers suitable for a variety of driver applications and is compatible with Metro MSA standards.

The 4953 consists of two high performance wideband amplifiers combined with off chip circuitry assembled in a surface mount package. A single 4953 placed between the MUX and Optical Modulator provides OEMs with a board level modulator driver surface mount solution.

The 4953 provides Metro and Long Haul designers with system critical features such as: low power dissipation (1.1 W at Vo=6 V), very low rail ripple, high voltage drive capability at 5V bias (6 V amplitude adjustable to 3 V), low output jitter (10 ps typical), and low input drive sensitivity (250 mV at Vo=6 V).

The 4953 requires external DC blocks, a low frequency choke, and control circuitry.

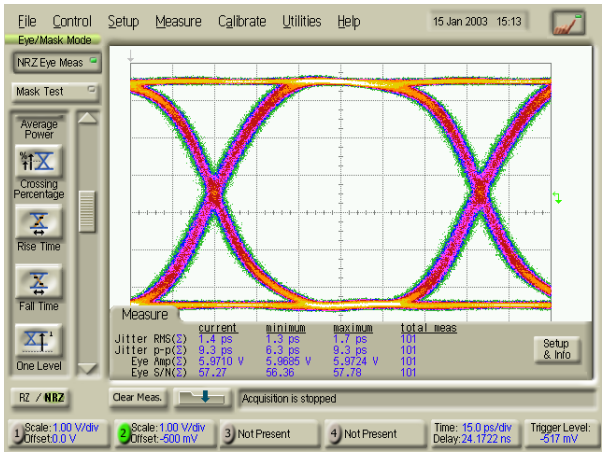
The TGA4953-EPU is available on an evaluation board.

Primary Applications

- Mach-Zehnder Modulator Driver for Metro and Long Haul.

Measured Performance

TGA4953 Evaluation Board (Metro MSA Conditions)
10.7 Gb/s, Vplus=5 V, Id=210 mA, (Pdc=1.1 Watt)
Vout=6 Vpp, CPC=50%, Vin = 500 mVpp
Scale: 2 V/div, 15 ps/div



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MAXIMUM RATINGS

SYMBOL	PARAMETER 6/	VALUE	NOTES
Vd1, Vd2T	POSITIVE SUPPLY VOLTAGE Drain Voltage	8 V	
Id1 Id2T	POSITIVE SUPPLY CURRENT Drain Current Drain Current	100 mA 300mA	1/
P_d	POWER DISSIPATION	4 W	2/
Vg1, Vg2 Ig1, Ig2	NEGATIVE GATE Voltage Gate Current	0 V to –3 V 5 mA	
Vctrl1, Vctrl2 Ictrl1, Ictrl2	CONTROL GATE Voltage Gate Current	Vd/2 to –3 V 5 mA	3/
P_{IN} V_{IN}	RF INPUT Sinusoidal Continuous Wave Power 10.7Gb/s PRBS Input Voltage Peak to Peak	23 dBm 4 Vpp	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	4/ 5/
T_{STG}	STORAGE TEMPERATURE	-40 to 125 ^{0}C	

Notes:

1/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.
2/ When operated at this bias condition with a base plate temperature of 80^{0}C, the median life is reduced.
3/ Assure Vctl1 never exceeds Vd1 and assure Vctrl2 never exceeds Vd2 during bias up and down sequences.
4/ These ratings apply to each individual FET.
5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
6/ These ratings represent the maximum operable values for the device.

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THERMAL INFORMATION

Parameter	Test Condition	P_{diss} (W)	T_{Base} (°C)	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	MTTF (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd2T=4.7V, Id2T=150mA +/-5%	.71	80	98	26	>1E6

Notes:

1. Based on a detailed thermal model of the output stage where channel temperature is highest. Assumes worst case power dissipation condition (where no RF is applied at the input (no power is dissipated in the load).
2. Thermal transfer is conducted thru the bottom of the TGA4953EPU package into the motherboard. Design the motherboard to assure adequate thermal transfer to the base plate.

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RF SPECIFICATIONS
(T_A = 25°C Nominal)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			8		GHz
	SATURATED POWER BW			12		GHz
1/, 2/	SMALL-SIGNAL GAIN MAGNITUDE	2 and 4 GHz 6 GHz 10 GHz 14 GHz 18 GHz	30 28 26 19 12			dB
	GAIN FLATNESS	500KHz thru 5GHz			+/-1	dB
	SMALL SIGNAL AGC RANGE	Midband		30		dB
	NOISE FIGURE	3 GHz		2.5		dB
3/, 4/	EYE AMPLITUDE	VD2T=8.0V VD2T=6.5V VD2T=5.5V VD2T=4.5V VD2T=4.0V	10 8.0 7.0 6.0 5.5			Vpp
5/	ADDITIVE JITTER (rms)			.5		ps
6/, 7/	SATURATED OUTPUT POWER	2, 4, 6, 8, and 10 GHz	25			dBm
1/, 2/	INPUT RETURN LOSS MAGNITUDE	2, 4, 6, 10, 14, and 18GHz	10	15		dB
1/, 2/	OUTPUT RETURN LOSS MAGNITUDE	2, 4, 6, 10, 14, and 18GHz	10	15		dB
	RISE TIME (20/80)			25	30	ps

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RF SPECIFICATION
(Continued)

Notes:

1/ Verified at package level RF test.

2/ Package RF Test Bias: Vd=5 V, adjust Vg1 to achieve Id=65 mA then adjust Vg2 to achieve Id=200mA, Vctrl=+0.2 V

3/ Verified by design, SMT assembled onto a demonstration board detailed on sheet 6.

4/ Vin=250mV, Data Rate = 10.7Gb/s, VD1=VD2T or greater, VCTRL2 and VG2 are adjusted for maximum output.

5/ Computed using RSS Method where Jrms_additive = SQRT($Jrms\_out^2$ - $Jrms\_in^2$)

6/ Verified at die level on-wafer probe.

7/ Power Bias Die Probe: Vtee=8 V, adjust Vg to achieve Id=175 mA+/-5%, Vctrl=1.5 V
Note: At the die level, drain bias is applied thru the RF output port using a bias tee, voltage is at the DC input to the bias tee.

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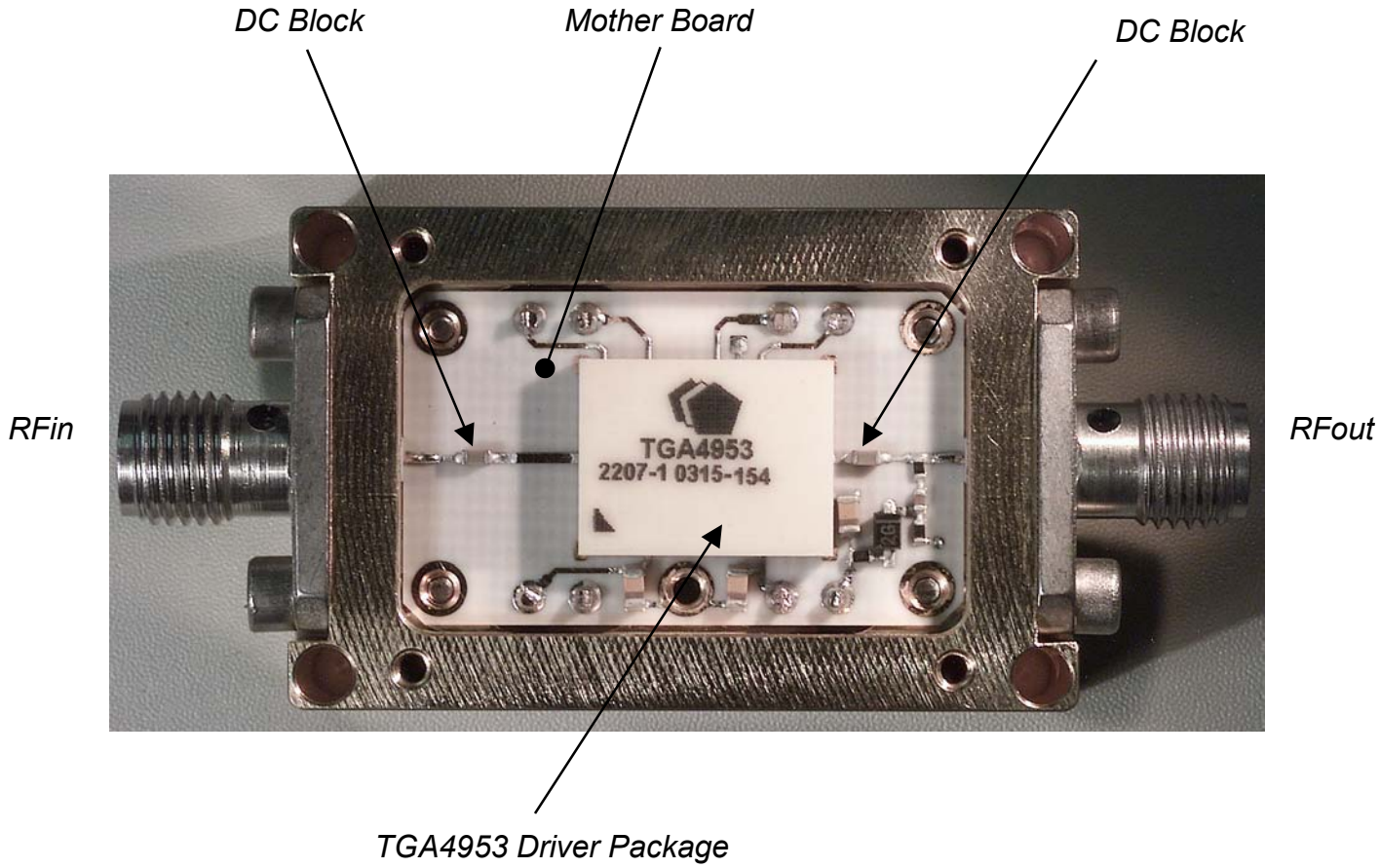
Demonstration Board



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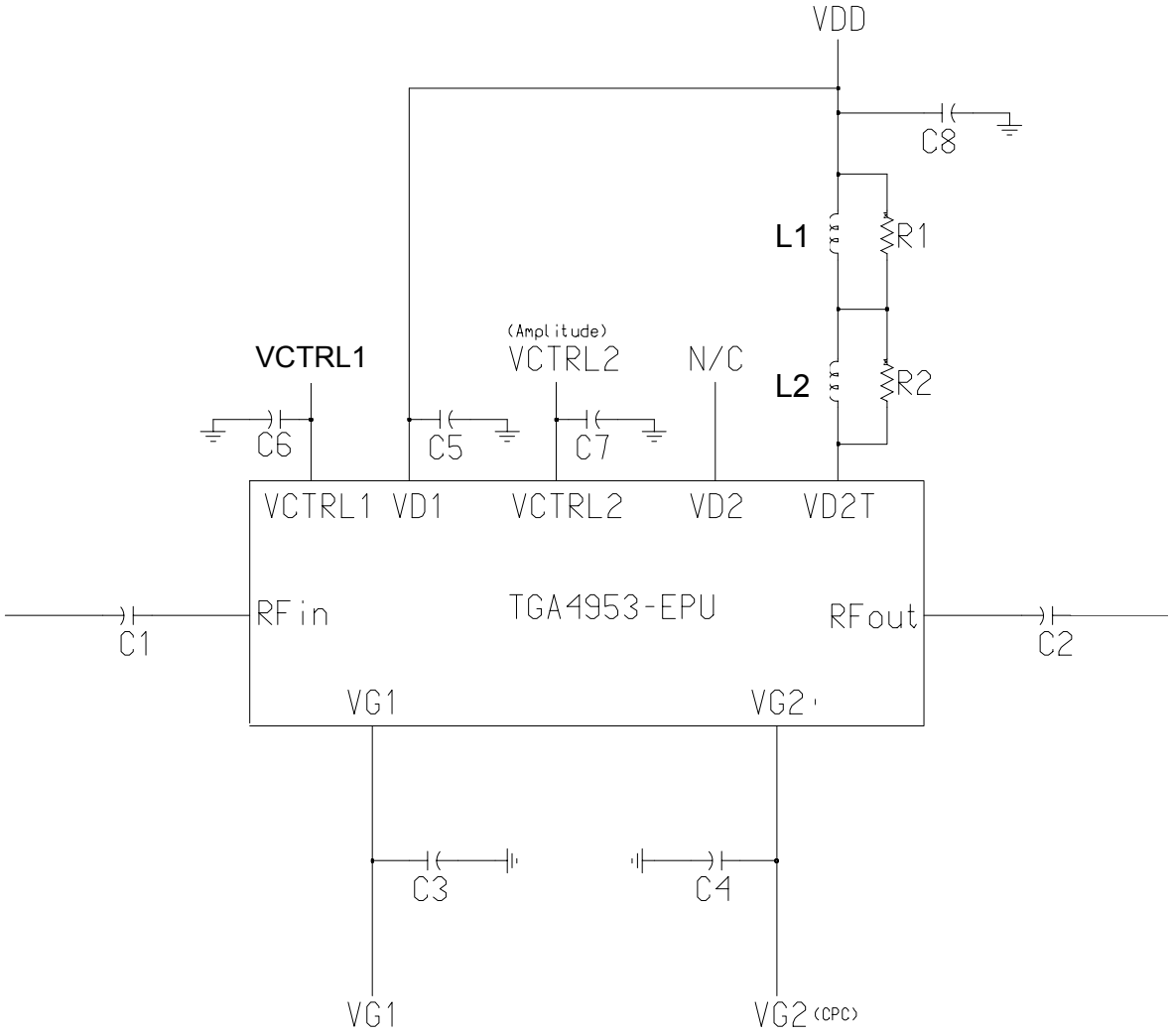
Demonstration Board Application Circuit



Note:

1. C3 and C4 extend low frequency performance thru 30 KHz. For applications requiring low frequency performance thru 100 KHz, C3 and C4 may be omitted.

2. C5 is a power supply decoupling capacitor and may be omitted.

3. C6 and C7 are power supply decoupling capacitors and may be omitted when driven directly with an op-amp. Impedance looking into VCTRL1 and VCTRL2 is 10Kohms real.

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Demonstration Board Application Circuit
(Continued)

Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2	DC Block, Broadband	Presidio	BB0502X7R104M16VNT9820
C3, C4, C5	10uF Capacitor MLC Ceramic	AVX	0802YC106KAT
C6, C7	0.01 uFCapacitor MLC Ceramic	AVX	0603YC103KAT
C8	10 uF Capacitor Tantalum	AVX	TAJA106K016R
L1	220 uH Inductor	Belfuse	S581-4000-14
L2	330 nH Inductor	Panasonic	ELJ-FAR33MF2
R1, R2	274 Ω Resistor	Panasonic	ERJ-2RKF2740X

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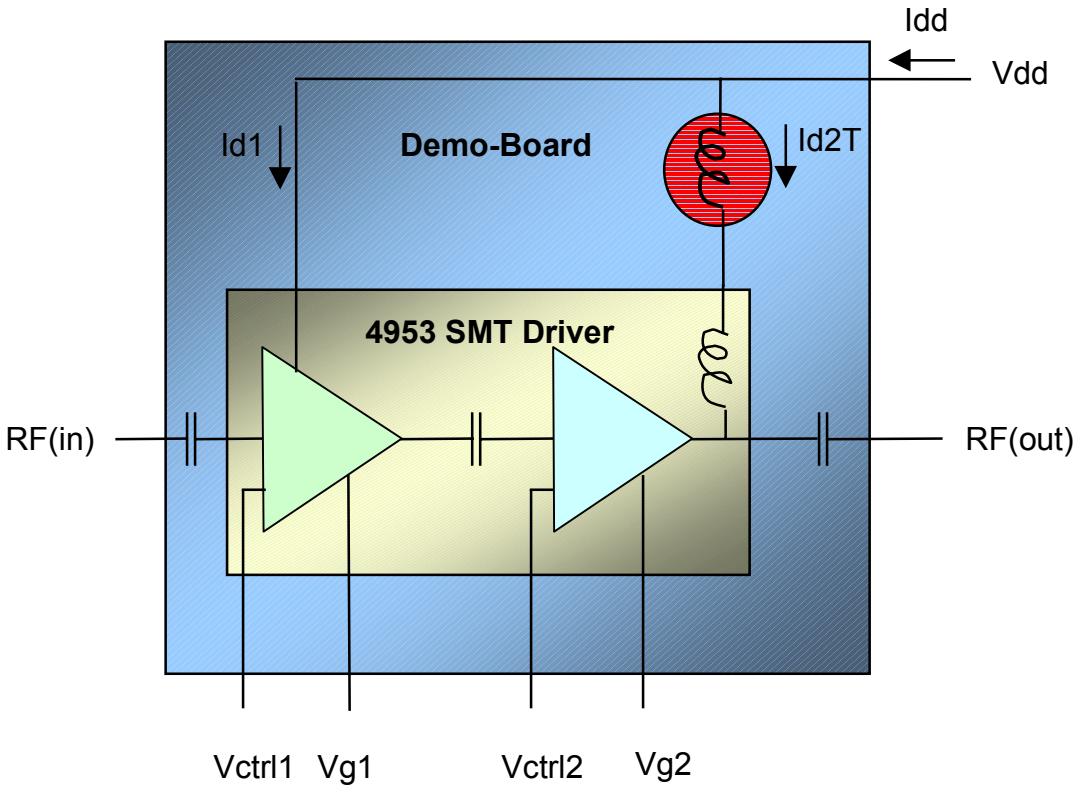
TGA4953 Typical Performance Data Measured on a Demonstration Board



Demonstration Board Block Diagram

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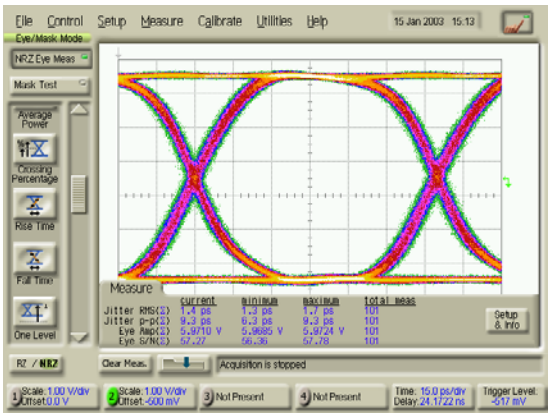
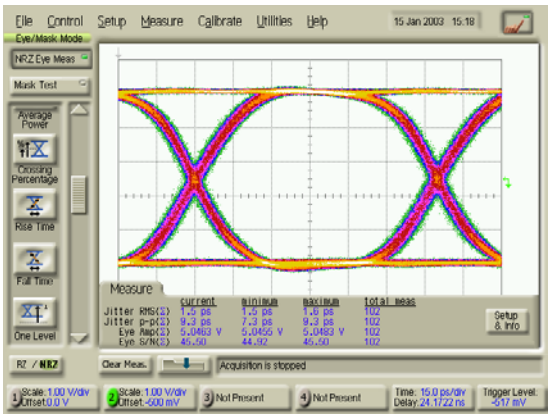
Typical Measured Performance on Demonstration Board
10.7Gb/s 2^31-1, Vdd=5V
CPC=50%

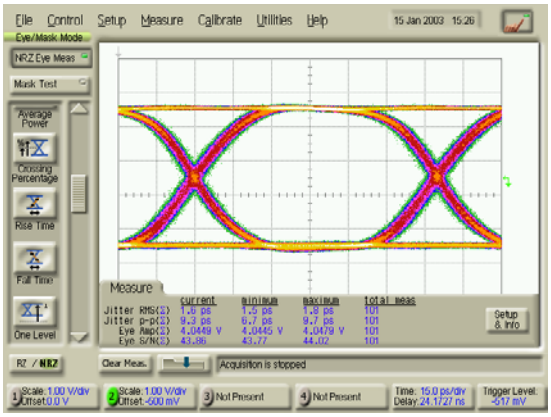
Vo=6V



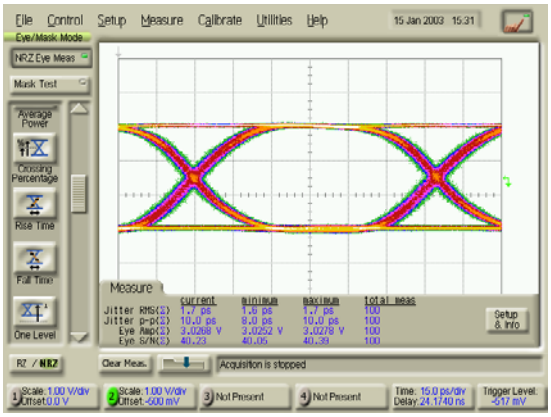
Vo=5V



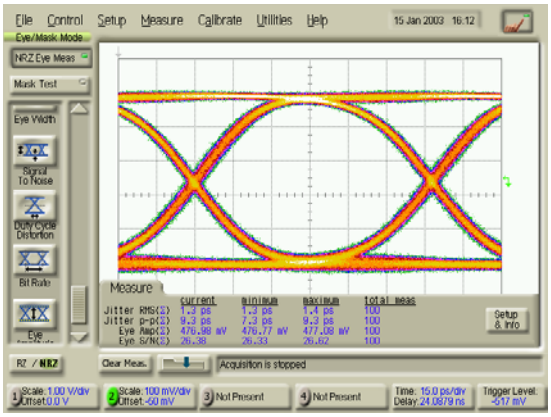
Vo=4V



Vo=3V



Input Signal Vin=500mV



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Typical Bias Conditions
Vdd=5V

Vo(V)	Vg1(V)	Vg2(V)	Id	Vctrl2
6	-0.66	-0.57	221	+0.22
5	-0.66	-0.59	198	+0.04
4	-0.66	-0.67	172	-0.14
3	-0.66	-0.74	147	-0.34

Notes:
1. Vdd=5V, Id1=65mA, and Vctrl1=-0.2V
2. Vin=500mVpp
3. 50%CPC

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Bias Procedure
Vdd=5V, Vo=6Vamp, CPC=50%

Bias ON

1. Disable the output of the PPG
2. Set Vd=0V Vctrl1=0V Vctrl2=0 Vg1=0V and Vg2=0V
3. Set Vg1=-1.5V Vg2=-1.5V **Vctrl1=-0.2V**
4. Increase Vd to 5V observing Id.
   - Assure Id=0mA
5. Set Vctrl2=+0.2V
   - Id should still be 0mA
6. Make Vg1 more positive until **Idd=65mA**.
   - This is Id1 (current into the first stage)
   - Typical value for **Vg1 is -0.65V**
7. Make Vg2 more positive until Idd=220mA.
   - This sets Id2T to 155mA.
   - Typical value for Vg2 is -0.55V
8. Enable the output of the PPG.
   - Set Vin=500mV
9. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
   - Typical value for **Vctrl2 is +0.22V** for Vo=6V.
10. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.
    - Typical value for **Vg2 is -0.57V** to center crossover with Vo=6V.

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl2=0V
3. Set Vd=0V
4. Set Vctrl1=0V
5. Set Vg2=0V
6. Set Vg1=0V

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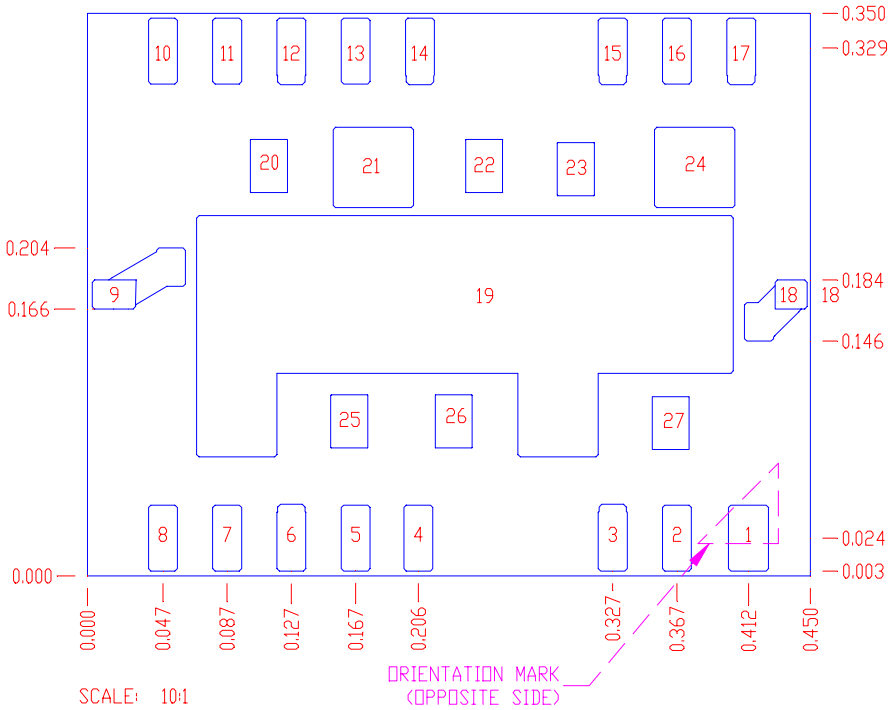
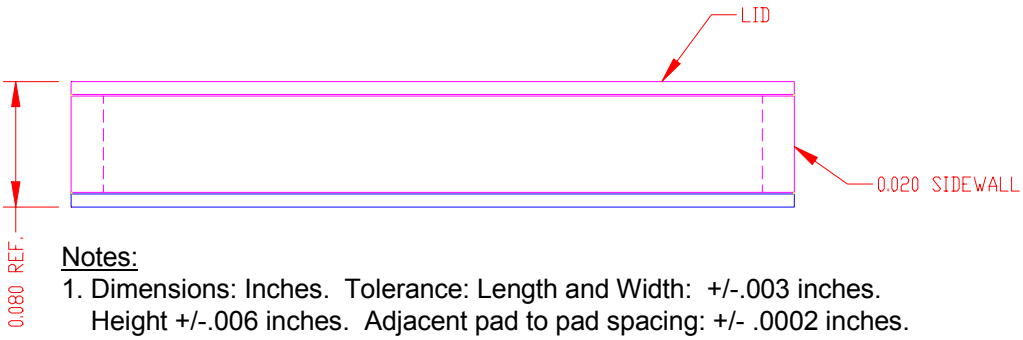
TGA4953 Mechanical Drawing



PIN	FUNCTION		PIN	FUNCTION	
1	N/C		10	N/C	
2	N/C		11	N/C	
3	VG1	(0.018″ x 0.041″)	12	VD2T	(0.018″ x 0.041″)
4	N/C		13	VD2	
5	N/C		14	VCTRL2	(0.018″ x 0.041″)
6	VG2	(0.018″ x 0.041″)	15	VD1	(0.018″ x 0.041″)
7	N/C		16	N/C	
8	N/C		17	VCTRL1	(0.018″ x 0.041″)
9	RF OUT	(0.058″ x 0.038″)	18	RF IN	(0.039″ x 0.038″)
			19 thru 27	GND	



Notes:

1. Dimensions: Inches. Tolerance: Length and Width: +/-.003 inches.
   Height +/-.006 inches. Adjacent pad to pad spacing: +/- .0002 inches.
   Pad Size: +/- .001 inches.
2. Surface Mount Interface:
   Material: RO4003 (thickness=.008 inches), 1/2oz copper (thickness=.0007 inches)
   Plating Finish: 100-350 microinches nickel underplate, with 5-10 microinches flash gold overplate.

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