

1.0 General Description

The AMIS-710409-A4 (PI409MC-A4) is a contact image sensor (CIS) module. It is a long CIS module that uses MOS image sensor technology for high-speed performance and high sensitivity. Its four parallel video outputs give the AMIS710409-A4 its high speed performance. The AMIS-710409-A4 is suitable for scanning A4 size (216mm) documents with 15.8 dots per millimeter (dpi) resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- Ultra high speed
- Four parallel analog video outputs clocked at 5.0MHz
- 180usec/line scanning speed @ 5.0MHz clock speed
- 15.8dpm resolution, 216mm scanning length
- Wide dynamic range
- Red light source 660nm
- Standard A4 size \cong 14mm x 19mm x 232mm
- Low power
- Light weight

3.0 Functional Description

The AMIS-710409-A4 imaging module consists of 27 AMIS-720442 (PI3042) imaging chips, produced by AMIS. The sensor chips are monolithic devices with 128 photo sensing elements. Twenty seven of these imaging chips are cascaded to provide a 3456 photo-elements module. The AMIS-720442 chips are integrated with the associated multiplex switches of the photo sensors, a digital shift register and a chip selection switch. The shift register sequentially clocks out the integrated image charges from each of the sensing elements and passes them through the chip-select switch and out onto the video line. The chip-select switches are sequentially switched as each predecessor chip completes its scan. These 27 sensors, bonded on a PCB, are grouped into four sub-cascaded sections. Each contiguously cascaded chip section is connected on separate video lines, therefore providing four video outputs, VOUT1, VOUT2, VOUT3, and VOUT4. Before the signal charges from the four video lines appear at their respective outputs, they are converted to signal voltages by four on-board buffer amplifiers; one for each of its corresponding video section. The first three sections, VOUT1, VOUT2 and VOUT3 have seven sensor chips, while the VOUT4 has six sensor chips. Since each sensor chip has 128 pixels, there are a total of 3456 pixels (see Figure 1).

Mounted in the module housing along with the PCB, is a one-to-one graded indexed micro lens array, which focuses image of the scanned documents onto the sensing line of the sensor chips. The third major component mounted in the module is the LED light source (see Figure 2). The pictorial cross section shows the LED bar light source and its illumination path as it reflects the image from the document and focuses through the ROD lens onto the image sensing line of the sensing chips. All components are housed in a small plastic housing, which has a cover glass. This cover glass also serves as the window. It is the focal point for the object being scanned and protects all of the critical components within the housing from dust. I/O to the module is a 12-pin connector located on one end of the module (see Figure 5).

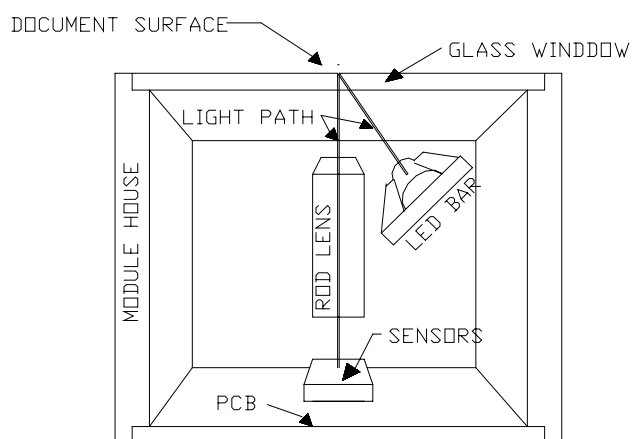
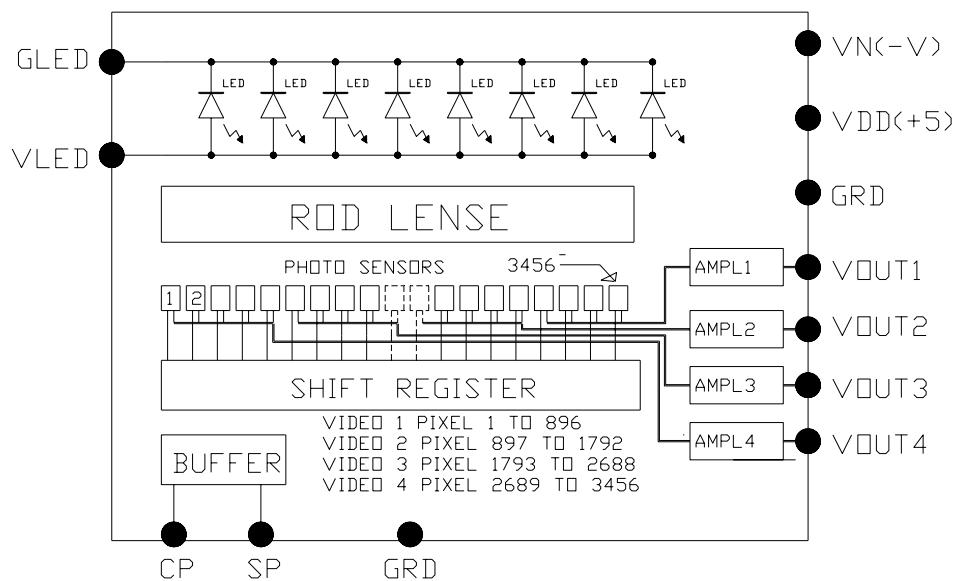


Figure 2: AMIS-710409-A4 Cross Section

4.0 I/O Designation

Table 1 lists the pin numbers and their designations for the I/O connector. It is a JAE IL-Z-12P-S125L3-E connector.

Table 1: Pin Configuration

Pin Number	Symbol	Names and Functions
1	VOUT1	Analog video output 1
2	VOUT2	Analog video output 2
3	GND	Ground; 0V
4	VOUT3	Analog video output 3
5	VOUT4	Analog video output 4
6	Vdd	Positive power supply
7	SP (START)	Shift register start pulse
8	GND	Ground; 0V
9	CP (CLOCK)	Sampling clock pulse
10	Vn	Negative power supply
11	GLED	Ground for the light source; 0V
12	VLED	Supply for the light source

5.0 Absolute Maximum Rating

Table 2: Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply voltage	Vdd	7	V
	Idd	100	ma
	Vn	-15	V
	In	35	ma
	VLED	6	V
	ILED	600	ma
Input clock pulse (high level)	Vih	Vdd – 0.5V	V
Input clock pulse (low level)	Vil	-0.5	V

Note: These parameters are absolute maximums. Do not operate under these conditions.

6.0 Environmental Specifications

Table 3: Operating and Storage Environment

Parameters	Symbols	Maximum Rating	Units
Operating temperature ⁽¹⁾	Top	0 to 50	°C
Operating humidity ⁽¹⁾	Hop	10 to 90	%
Storage temperature ⁽¹⁾	Tstg	-20 to +75	°C
Storage humidity ⁽¹⁾	Hstg	10 to 90	%

Note:

(1) These are standard specifications for the CIS modules.

7.0 Electro-Optical Characteristics (25°C)

Table 4: Electro-Optical Characteristics at 25°C

Parameter	Symbol	Parameter	Units	Note
Total number of photo detectors		3456	Elements	
Section 1, 2 & 3 number of photo detectors		896	Elements	
Section 4 number of detectors		768	Elements	
Pixel-to-pixel spacing		63.5	μm	
Line scanning rate	Tint ⁽¹⁾	180	μsec	@ 5.0MHz clock frequency
Clock frequency ⁽²⁾	f	5.0	MHz	
Bright output voltage ⁽³⁾	Video output	500	mVolt	
Bright output non-uniformity ⁽⁴⁾	Up	+/-30	%	
Dark non-uniformity ⁽⁵⁾	Ud	<140	mV	
Dark output voltage ⁽⁶⁾	Dark level (DL)	<600	mV	
Modulation transfer function ⁽⁷⁾	MTF	>50	%	

- Notes:**
- (1) Tint: line scanning rate or integration time. Tint is determined by the interval between two start pulses (SP).
 - (2) f: main clock frequency also equals the video sampling frequency.
 - (3) Video output level is controlled with an adjustment as well as the integration time
 - (4) $Up = \{[Vp(max) - Vp(min)] / Vp(max)\} \times 100\%$
Where Vp(max) = maximum peak pixel and Vp(min) = minimum pixel.
 - (5) $Ud = Vdmax - Vdmin$
Vdmin is the minimum output voltage with LED off.
Vdmax is maximum output voltage with LED on.
 - (6) This level is measured from the reset level, which is located between the pixels, during the pixel reset duration. The reset level is at or near ground, 0V. Note that the gain is adjustable on each output. However, it is recommended that the gain should not be increased above the level where the reset ground level starts to increase above zero.
 - (7) A graph of a typical MTF is shown in Figure 3.

8.0 MTF Graph and its Discussion

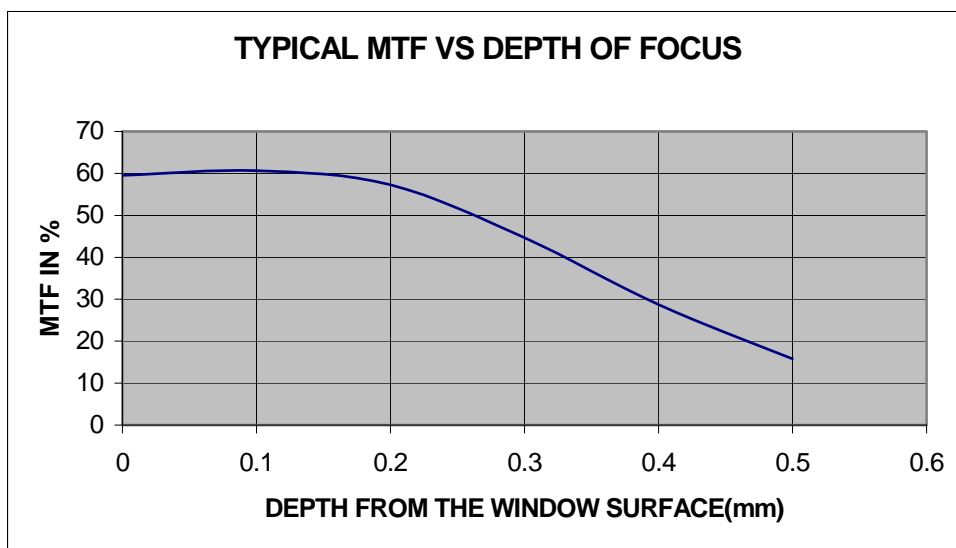


Figure 3: MTF versus Distance

The graph in figure 3 depicts the working depth of focus. Since this module is a 400dpi module, a pixel density of 400 pixels per inch, the MTF was measured with a 200dpi or a 100 line-pair per inch optical bar pattern. The test was conducted with the pixel rate set to 2.5MHz (see Figure 3).

The effective algorithm used in the measurements is as described by the following equation:

$$MTF = \frac{[Vp(n) + Vp(n+1)]/2 - [Vp(n+2) + Vp(n+3)]/2}{[Vp(n) + Vp(n+1)]/2 + [Vp(n+2) + Vp(n+3)]/2}$$

Where n is 1, 2,3456th, Vp(n) is the signal amplitude of the nth pixel.

9.0 Recommended Operating Conditions (25°C)

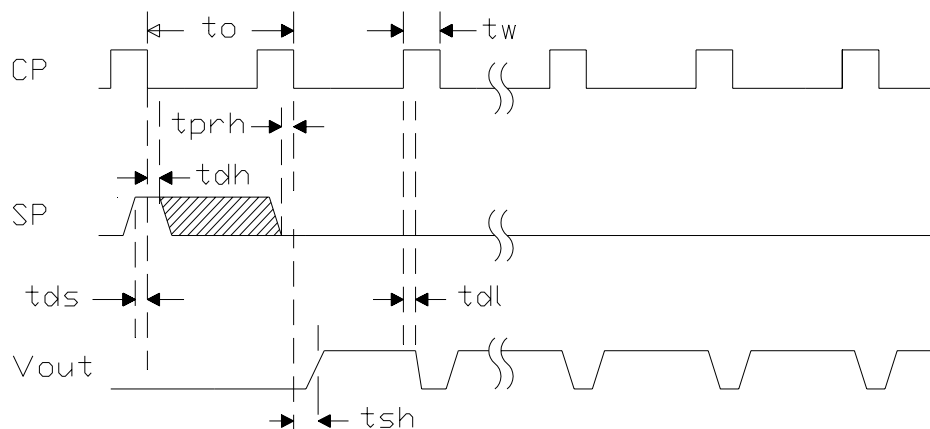
Table 5: Recommended Operating Conditions (25°C)

Item	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd	4.5	5.0	5.5	V
	Vn.	-13	-5	-4.0	V
	Idd		87	95	ma
	In		25	30	ma
	ILED		450	550	ma
	VLED		5	5.5	V
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.6	V
Clock frequency	f	0.	5.0	6.0	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration			50		ns
Integration time	Tint		180		μs
Operating temperature ⁽¹⁾	Top		25	50	C

Note:

(1) See the note under Table 3.

10.0 Switching Characteristics (25°C)



MODULE TIMING DIAGRAM

Figure 4: Module Timing Diagram

The switching characteristics (at 25°C) for the I/O clocks are shown in Figure 4. For the timing symbol definitions, see Table 6.

Note: Only one video output is shown because all four videos have identical electrical characteristics. The only physical difference between them is in Section 4 output, VOUT4. Section 4 has only six sensor chips, hence its active scan is shorter by 128 pixels.

Table 6: Timing Symbol's Definition and Timing Values

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	t_o	0.20		4.0	μ s
Clock pulse width	t_w	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of SP ⁽¹⁾	t_{prh}	0			ns
Data setup time	t_{ds}	20			ns
Data hold time	t_{dh}	0			ns
Signal delay time	t_{dl}	20			ns
Signal settling time	t_{sh}	100			ns

Note:

- (1) "Prohibit crossing of start pulse" is to indicate that the start pulse should not be active high between any two consecutive high going clock pulses or two consecutive low going clock pulses (see Figure 4). Only one high going clock under the active high start pulse initiates the internal shift register and it must not be active over two high going clocks. All low going clock pulses will not initiate the shift register. To ensure that the start pulse will not be actively high during two consecutive high going clocks, the circuit should be designed to keep the start pulse active only for one high going clock cycle.

11.0 Mechanical Structure of the Module

The isometric sketch of the housing is shown to demonstrate the connector location, the approximate overall dimensions and the general geometric layout of the module (see Figure 5). It is not intended for use as a design reference. A detailed drawing of the AMIS-710409-A4 module housing is available upon request.

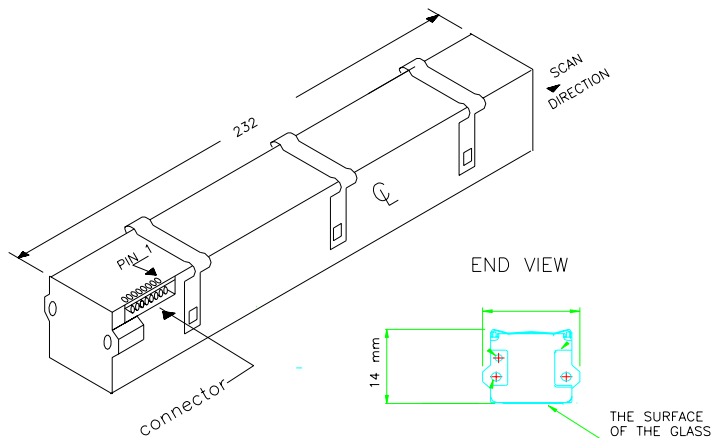


Figure 5: AMIS-710409-A4 Module Housing Sketch

12.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our Web site at: <http://www.amis.com>

North America

Tel: +1.208.233.4690

Fax: +1.208.234.6795

Europe

Tel: +32 (0) 55.33.22.11

Fax: +32 (0) 55.31.81.12

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