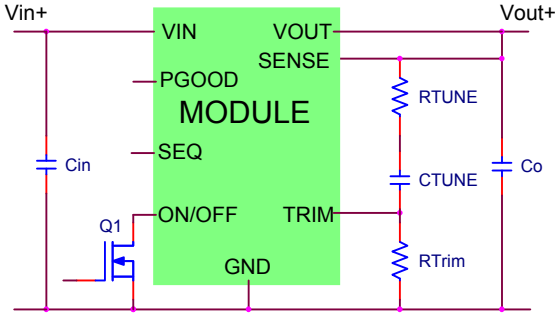
Data Sheet
January 21, 2010

12V TLynx™ Non-Isolated DC-DC Power Modules: 4.5 – 14Vdc input; 0.69Vdc to 5.5Vdc output; 20A Output Current

RoHS Compliant EZ-SEQUENCE™ Applications

- **Distributed power architectures**
- **Intermediate bus voltage applications**
- Telecommunications equipment
- **Servers and storage applications**
- Networking equipment
- Industrial equipment



Features

- Compliant to RoHS EU Directive 2002/95/EC (Z versions)
- Compatible in a Pb-free or SnPb reflow environment (Z versions)
- Wide Input voltage range (4.5Vdc-14Vdc)
- Output voltage programmable from 0.69Vdc to 5.5 Vdc via external resistor
- Tunable Loop™ to optimize dynamic output voltage response
- Flexible output voltage sequencing EZ-SEQUENCE (APTS versions)
- Fixed switching freqeuency and ability to synchronize with external clock
- Output overcurrent protection (non-latching)
- Overtemperature protection
- Remote On/Off
- Remote Sense
- Power Good signal
- Ability to sink and source current
- Small size:

  33 mm x 13.46 mm x 8.5 mm

  (1.3 in x 0.53 in x 0.334 in)
- Wide operating temperature range [-40°C to 105°C(Ruggedized: -D), 85°C(Regular)]
- Ruggedized (-D) version able to withstand high levels of shock and vibration
- *UL** 60950-1Recognized, *CSA*† C22.2 No. 60950-1-03 Certified, and *VDE*‡ 0805:2001-12 (EN60950-1) Licensed
- ISO** 9001 and ISO 14001 certified manufacturing facilities

Description

The 12V TLynx™ series of power modules are non-isolated dc-dc converters that can deliver up to 20A of output current. These modules operate over a wide range of input voltage (V_{IN} = 4.5Vdc-14Vdc) and provide a precisely regulated output voltage from 0.69Vdc to 5.5Vdc, programmable via an external resistor. Features include frequency synchronization, remote On/Off, adjustable output voltage, over current and temperature protection, power good and output voltage sequencing. The Ruggedized version (-D) is capable of operation up to 105°C and withstand high levels of shock and vibration. The Tunable Loop™, allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.
† *CSA* is a registered trademark of Canadian Standards Association.
‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.
** ISO is a registered trademark of the International Organization of Standards

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Symbol	Min	Max	Unit
Input Voltage Continuous	All	V_{IN}	-0.3	15	Vdc
Voltage on SEQ terminal	All	V_{SEQ}	-0.3	V_{IN}	Vdc
Voltage on SYNC terminal	All	V_{SYNC}	-0.3	12	Vdc
Voltage on PG terminal	All	V_{PG}	-0.3	6	Vdc
Operating Ambient Temperature (see Thermal Considerations section)	All -D version	T_A T_A	-40 -40	85 105	°C °C
Storage Temperature	All	T_{stg}	-55	125	°C

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	V_{IN}	4.5	—	14	Vdc
Maximum Input Current (V_{IN}=4.5V to 14V, I_O=$I_{O,max}$)	All	$I_{IN,max}$			20	Adc
Input No Load Current (V_{IN} = 10.0Vdc, I_O = 0, module enabled) (V_{IN} = 12.0Vdc, I_O = 0, module enabled)	 $V_{O,set}$ = 0.69 Vdc $V_{O,set}$ = 3.3Vdc	 $I_{IN,No\ load}$ $I_{IN,No\ load}$		 42 74		 mA mA
Input Stand-by Current (V_{IN} = 12.0Vdc, module disabled)	All	$I_{IN,stand-by}$		3		mA
Inrush Transient	All	I^2t			1	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1µH source impedance; V_{IN} =4.5V to 14V, I_O= I_{Omax} ; See Test Configurations)	All			43		mAp-p
Input Ripple Rejection (120Hz)	All			45		dB

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This power module can be used in a wide variety of applications, ranging from simple standalone operation to an integrated part of sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included; however, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fast-acting fuse with a maximum rating of 20 A (see Safety Considerations section). Based on the information provided in this data sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's data sheet for further information.

Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage Set-point	All	$V_{O, set}$	-1.5		+1.5	% $V_{O, set}$
Output Voltage (Over all operating input voltage, resistive load, and temperature conditions until end of life)	All	$V_{O, set}$	-2.5	—	+2.5	% $V_{O, set}$
Adjustment Range (selected by an external resistor) (Some output voltages may not be possible depending on the input voltage – see Feature Descriptions Section)	All	V_O	0.69		5.5	Vdc
Output Regulation (for $V_O \geq 2.5$Vdc)						
Line (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$)	All			—	+0.4	% $V_{O, set}$
Load (I_O=$I_{O, min}$ to $I_{O, max}$)	All			—	10	mV
Output Regulation (for $V_O < 2.5$Vdc)						
Line (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$)	All			—	10	mV
Load (I_O=$I_{O, min}$ to $I_{O, max}$)	All			—	5	mV
Temperature (T_{ref}=$T_{A, min}$ to $T_{A, max}$)	All			—	0.5	% $V_{O, set}$
Remote Sense Range	All				0.5	Vdc
Output Ripple and Noise on nominal output (V_{IN}=$V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ Co = 0.1µF // 10 µF ceramic capacitors)						
Peak-to-Peak (5Hz to 20MHz bandwidth)	All			—	30	80	mV_{pk-pk}
RMS					14	28	mV_{rms}
External Capacitance[1]						
Without the Tunable Loop™						
ESR ≥ 1 mΩ	All	$C_{O, max}$	0	—	200	µF
With the Tunable Loop™						
ESR ≥ 0.15 mΩ	All	$C_{O, max}$	0	—	1000	µF
ESR ≥ 10 mΩ	All	$C_{O, max}$	0	—	10000	µF
Output Current	All	I_o	0		20	Adc
Output Current Limit Inception (Hiccup Mode)	All	$I_{O, lim}$		120		% $I_{o,max}$
Output Short-Circuit Current (V_O≤250mV) (Hiccup Mode)	All	$I_{O, s/c}$		2.6		Adc
Efficiency (V_{IN}= 10Vdc)	$V_{O,set}$ = 0.69Vdc	η		72.1		%
V_{IN}= 12Vdc, T_A=25°C	$V_{O,set}$ = 1.2Vdc	η		81.3		%
I_O=$I_{O, max}$, V_O= $V_{O,set}$	$V_{O,set}$ = 1.8Vdc	η		85.7		%
	$V_{O, set}$ = 2.5Vdc	η		88.0		%
	$V_{O,set}$ = 3.3Vdc	η		89.7		%
	$V_{O,set}$ = 5.0Vdc	η		91.8		%

[1] External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Switching Frequency	All	f_{sw}	—	550	—	kHz
Frequency Synchronization						
Synchronization Frequency Range			520		600	kHz
High-Level Input Voltage	All	V_{IH}	2.5			V
Low-Level Input Voltage	All	V_{IL}			0.8	V
Input Current, SYNC	V_{SYNC}=2.5V	I_{SYNC}			1	mA
Minimum Pulse Width, SYNC	All	t_{SYNC}	250			ns
Minimum Setup/Hold Time, SYNC[2]	All	t_{SYNC_SH}	250			ns
Dynamic Load Response						
(dIo/dt=10A/µs; V_{IN} = $V_{IN, nom}$; V_{out} = 1.5V, T_A=25°C)						
Load Change from Io= 50% to 100% of Io,max; Co = 0						
Peak Deviation	All	V_{pk}		380		mV
Settling Time (Vo<10% peak deviation)	All	t_s		30		µs
Load Change from Io= 100% to 50%of Io,max: Co = 0						
Peak Deviation	All	V_{pk}		300		mV
Settling Time (Vo<10% peak deviation)	All	t_s		30		µs

[2] To meet set up time requirements for the synchronization circuit, the logic low width of the pulse must be greater than 100 ns wide.

General Specifications

Parameter	Min	Typ	Max	Unit
Calculated MTBF (I_O=0.8$I_{O, max}$, V_O=5V, T_A=40°C) Telecordia Method Issue 2, Method I Case 3		14,262,200		Hours
Weight	—	6.05 (0.213)	—	g (oz.)

Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typ	Max	Units
On/Off Signal Interface (V_{IN}=$V_{IN,min}$ to $V_{IN,max}$; open collector or equivalent, Signal referenced to GND)						
Device is with suffix "4" – Positive Logic (See Ordering Information) Logic High (Module ON)						
Input High Current	All	I_{IH}		—	25	µA
Input High Voltage	All	V_{IH}	V_{IN} – 1	—	$V_{IN,max}$	V
Logic Low (Module OFF)						
Input Low Current	All	I_{IL}	—	—	3	mA
Input Low Voltage	All	V_{IL}	—	—	3.5	V
Device Code with no suffix – Negative Logic (See Ordering Information) (On/OFF pin is open collector/drain logic input with external pull-up resistor; signal referenced to GND) Logic High (Module OFF)						
Input High Current	All	I_{IH}	—	—	1	mA
Input High Voltage	All	V_{IH}	2.0	—	$V_{IN,max}$	Vdc
Logic Low (Module ON)						
Input low Current	All	I_{IL}	—	—	10	µA
Input Low Voltage	All	V_{IL}	0	—	1	Vdc
Turn-On Delay and Rise Times						
(V_{IN}=$V_{IN,nom}$, I_O=$I_{O,max}$, V_O to within ±1% of steady state)						
Case 1: On/Off input is enabled and then input power is applied (delay from instant at which V_{IN} = $V_{IN,min}$ until V_o = 10% of $V_{o,set}$)	All	Tdelay	—	2	—	msec
Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until V_o = 10% of $V_{o,set}$)	All	Tdelay	—	2	—	msec
Output voltage Rise time (time for V_o to rise from 10% of Vo, set to 90% of Vo, set)	All	Trise	—	5	—	msec
Output voltage overshoot (T_A = 25°C V_{IN}= $V_{IN,min}$ to $V_{IN,max}$, I_O = $I_{O,min}$ to $I_{O,max}$) With or without maximum external capacitance					3.0	% $V_{O,set}$
Over Temperature Protection (See Thermal Considerations section)	All	T_{ref}		135		°C
Sequencing Delay time Delay from $V_{IN,min}$ to application of voltage on SEQ pin	All	$T_{SEQ-delay}$	10			msec
Tracking Accuracy (Power-Up: 2V/ms)	All	V_{SEQ} –V_o			150	mV
(Power-Down: 2V/ms)	All	V_{SEQ} –V_o			100	mV
($V_{IN,min}$ to $V_{IN,max}$; $I_{O,min}$ to $I_{O,max}$ V_{SEQ} < V_o)						
Input Undervoltage Lockout Turn-on Threshold	All			4.45		Vdc
Turn-off Threshold	All			4.2		Vdc
Hysteresis	All			0.25		Vdc

Feature Specifications (cont.)

Parameter	Device	Symbol	Min	Typ	Max	Units
PGOOD (Power Good)						
Signal Interface Open Drain, $V_{supply} \leq 6VDC$						
Overvoltage threshold for PGOOD				110.8		$\%V_{O, set}$
Undervoltage threshold for PGOOD				89.1		$\%V_{O, set}$
Pulldown resistance of PGOOD pin	All			7	50	Ω

Characteristic Curves

The following figures provide typical characteristics for the 12V TLynx™ at 0.69Vo and at 25°C.

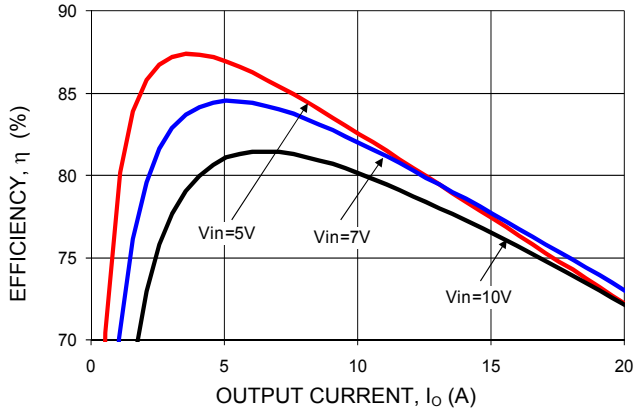


Figure 1. Converter Efficiency versus Output Current.

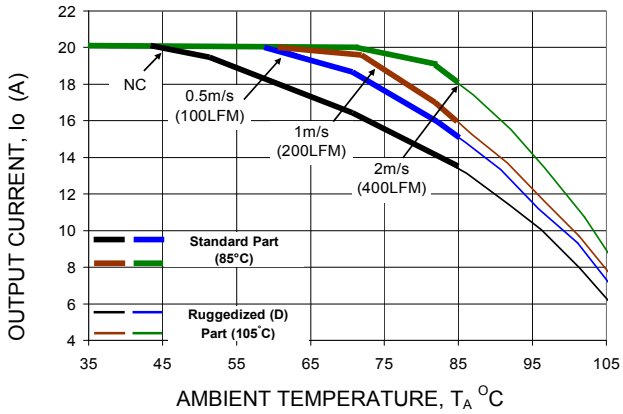


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

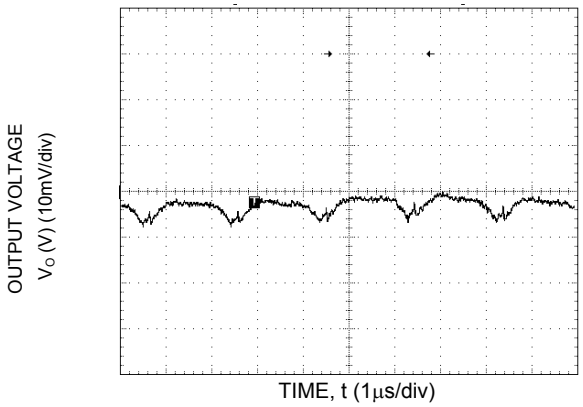


Figure 3. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

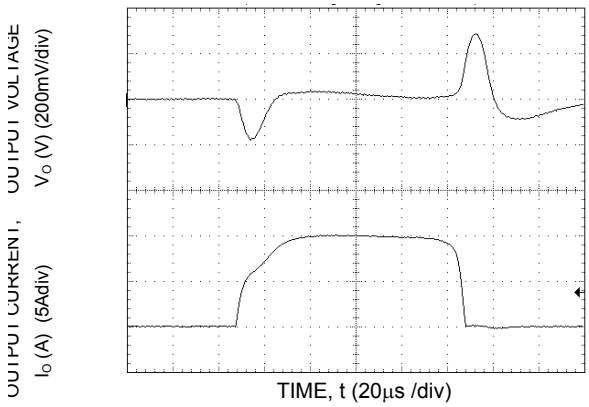


Figure 4. Transient Response to Dynamic Load Change from 0% to 50% to 0%.

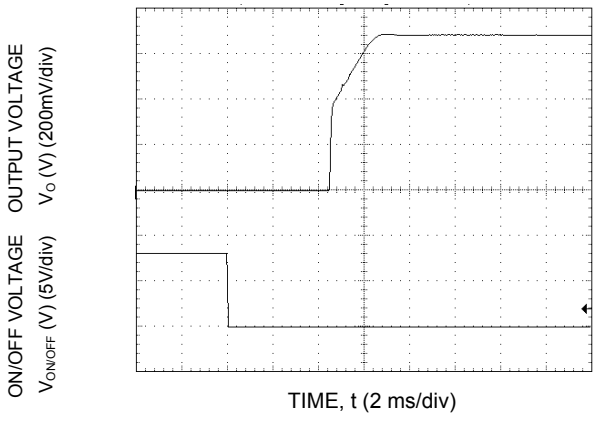


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

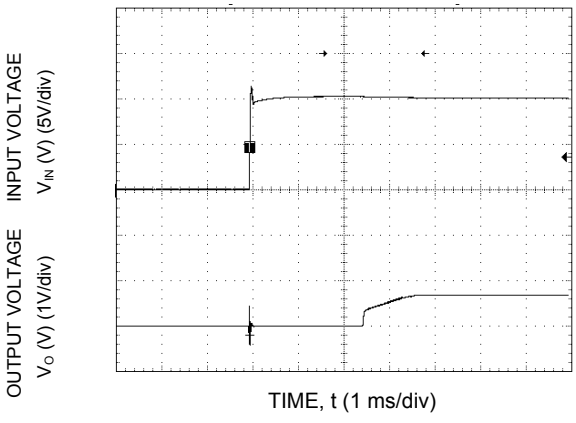


Figure 6. Typical Start-up Using Input Voltage (V_{IN} = 10V, I_o = $I_{o,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12V TLynx™ at 1.2Vo and at 25°C.

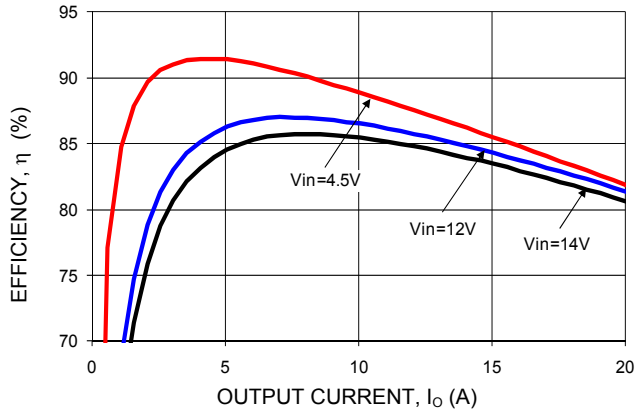


Figure 7. Converter Efficiency versus Output Current.

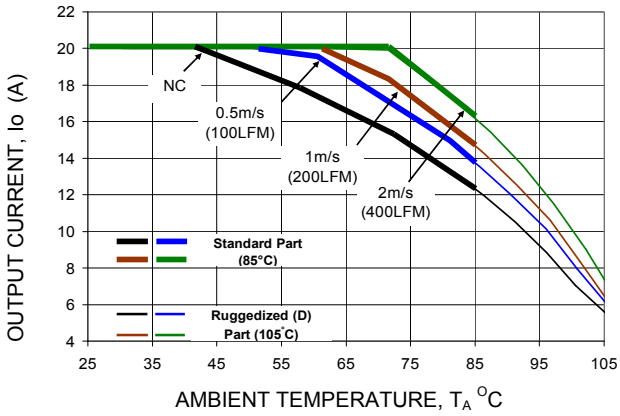


Figure 8. Derating Output Current versus Ambient Temperature and Airflow.

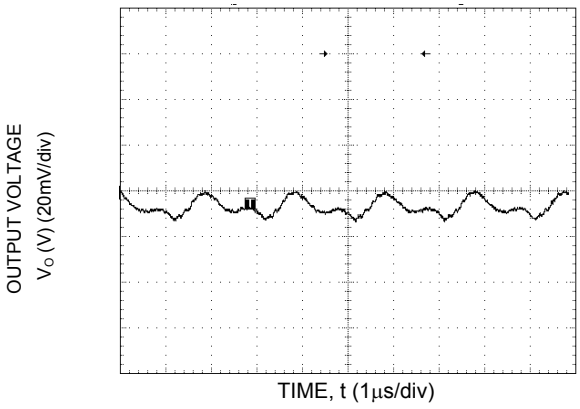


Figure 9. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

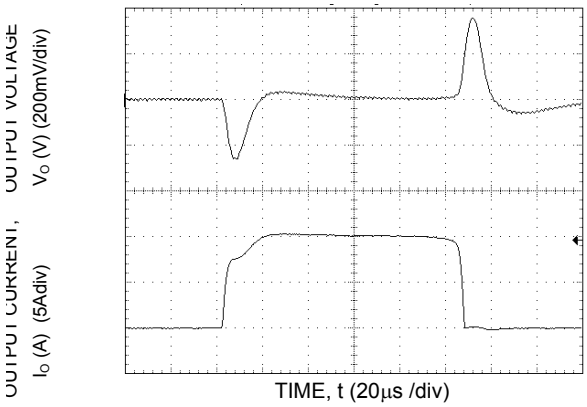


Figure 10. Transient Response to Dynamic Load Change from 0% to 50% to 0%.

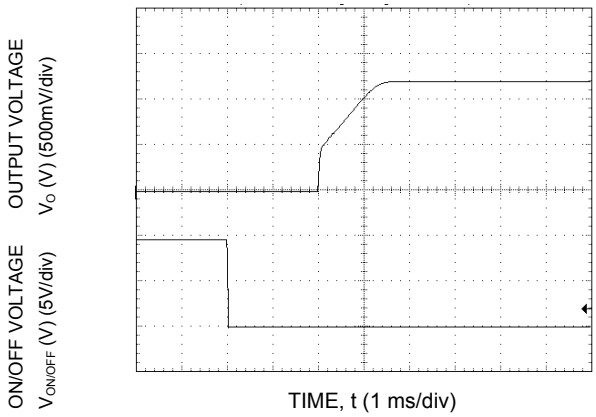


Figure 11. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

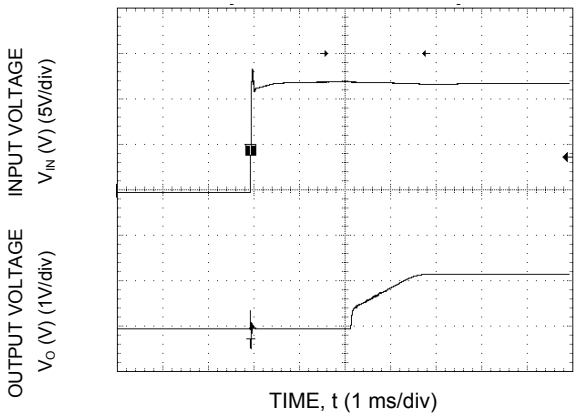


Figure 12. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12V TLynx™ at 1.8Vo and at 25°C.

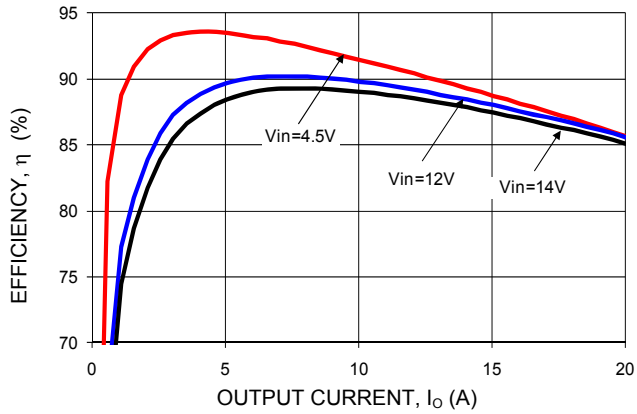


Figure 13. Converter Efficiency versus Output Current.

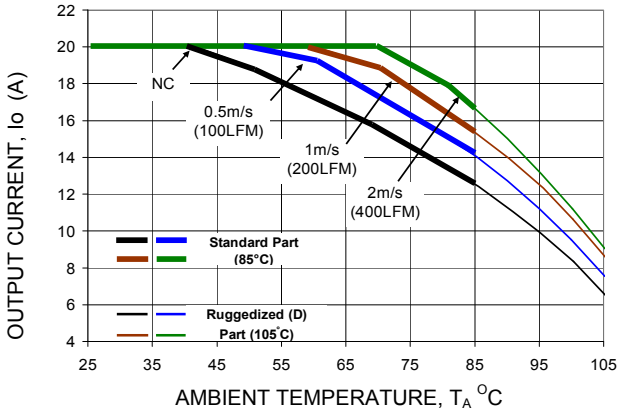


Figure 14. Derating Output Current versus Ambient Temperature and Airflow.

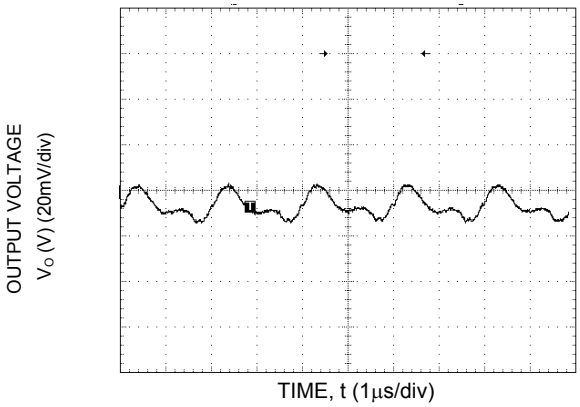


Figure 15. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

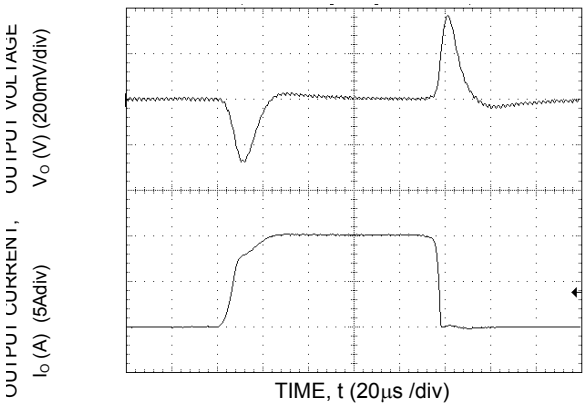


Figure 16. Transient Response to Dynamic Load Change from 0% to 50% to 0%.

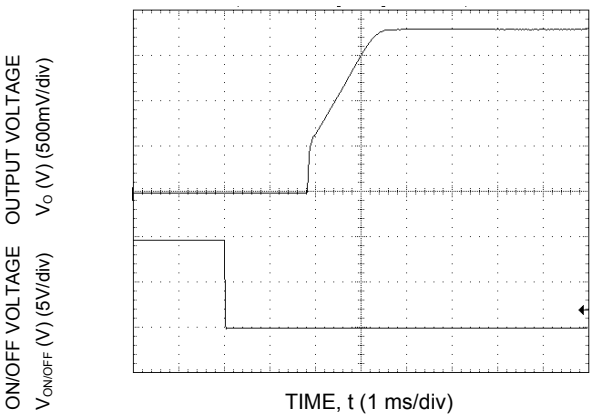


Figure 17. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

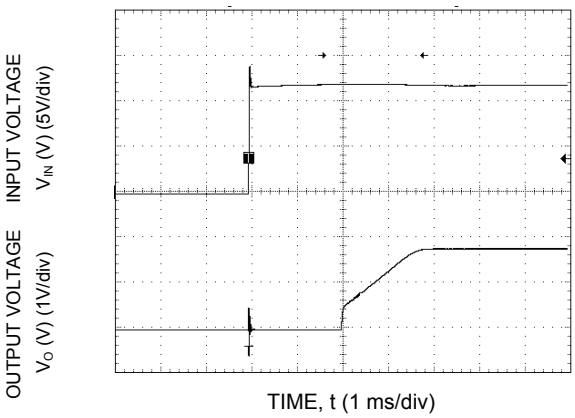


Figure 18. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12V TLynx™ at 2.5Vo and at 25°C.

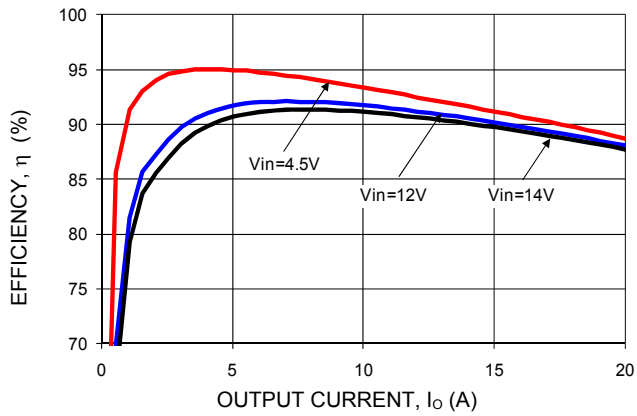


Figure 19. Converter Efficiency versus Output Current.

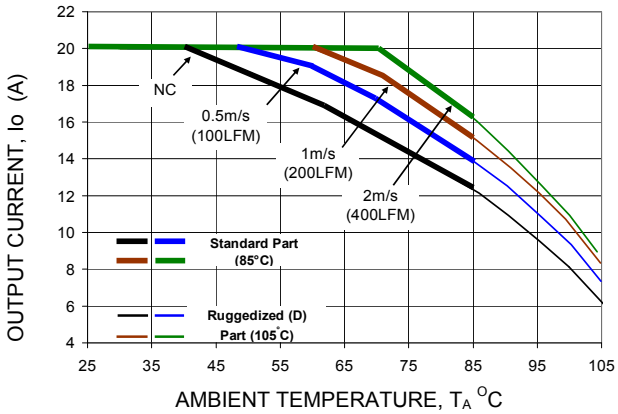


Figure 20. Derating Output Current versus Ambient Temperature and Airflow.

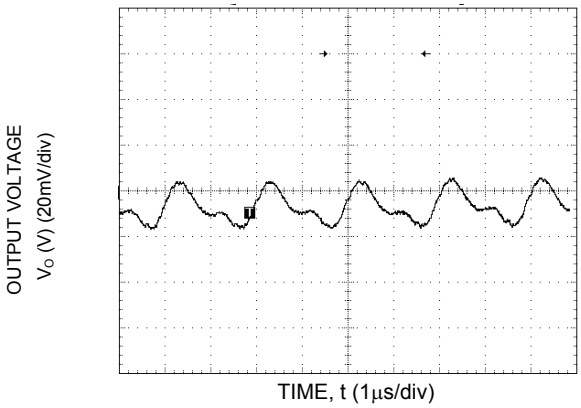


Figure 21. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

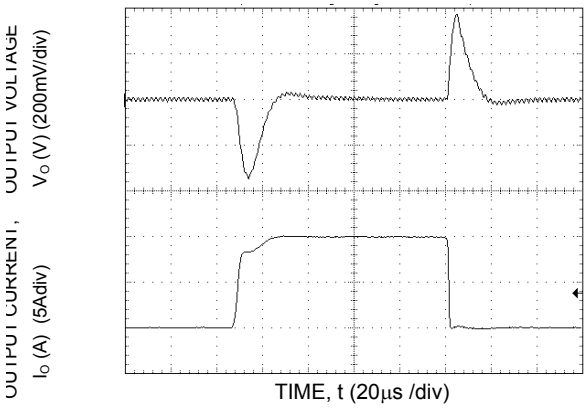


Figure 22. Transient Response to Dynamic Load Change from 0% to 50% to 0%.

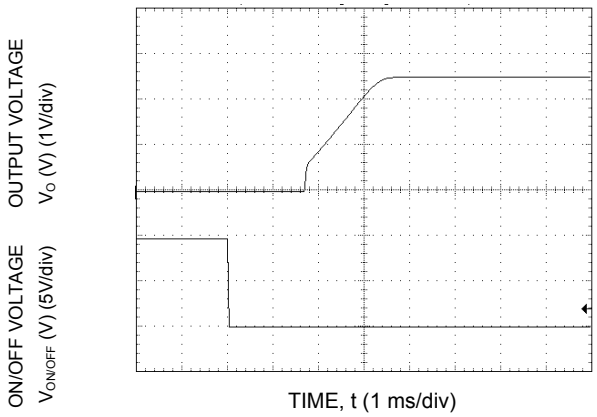


Figure 23. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

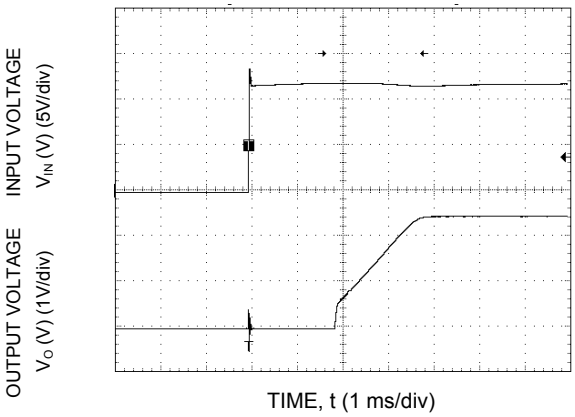


Figure 24. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12V TLynx™ at 3.3Vo and at 25°C.

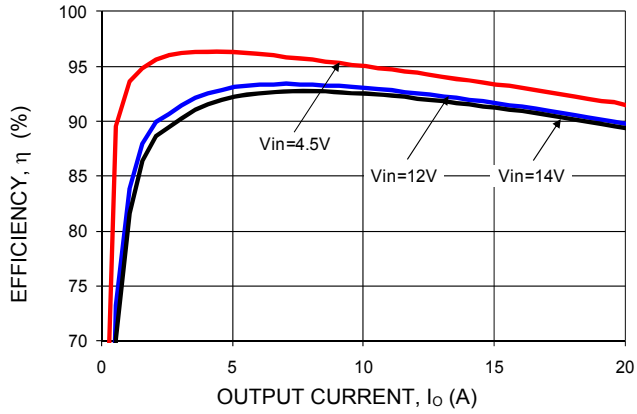


Figure 25. Converter Efficiency versus Output Current.

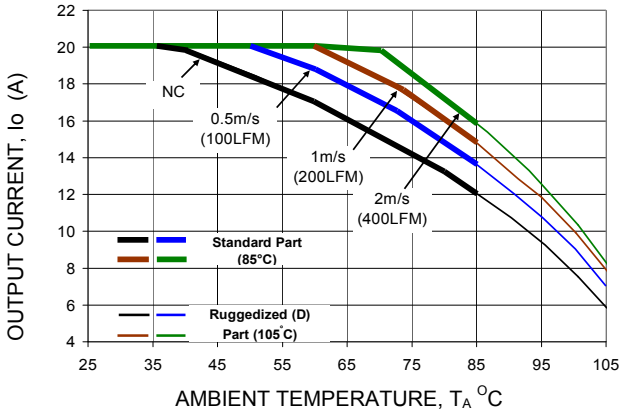


Figure 26. Derating Output Current versus Ambient Temperature and Airflow.

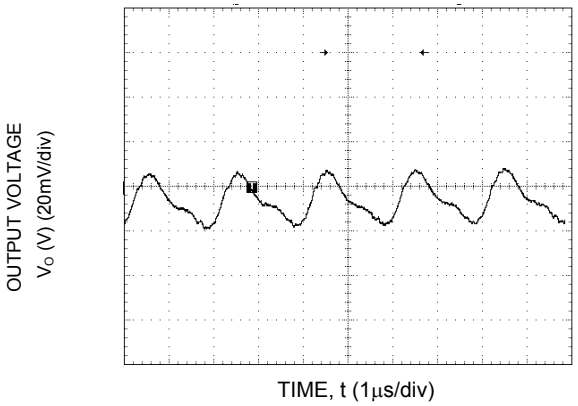


Figure 27. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

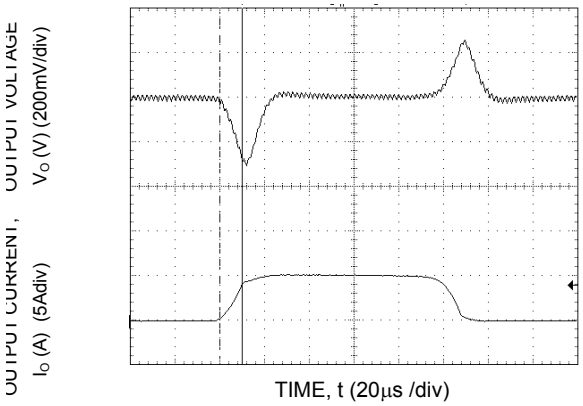


Figure 28. Transient Response to Dynamic Load Change from 0% 50% to 0%.

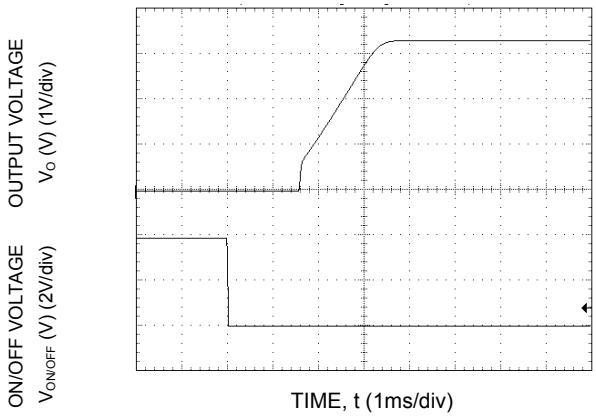


Figure 29. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

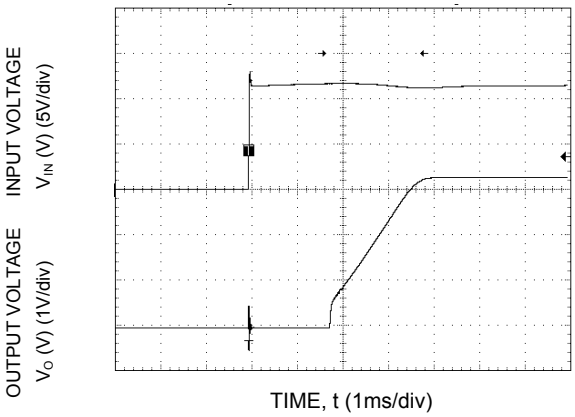


Figure 30. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12V TLynx™ at 5Vo and at 25°C.

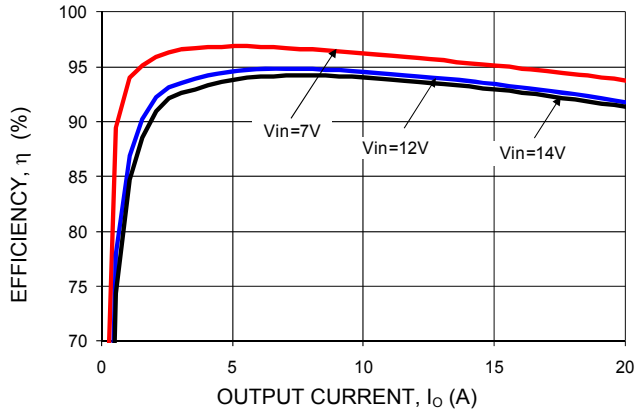


Figure 31. Converter Efficiency versus Output Current.

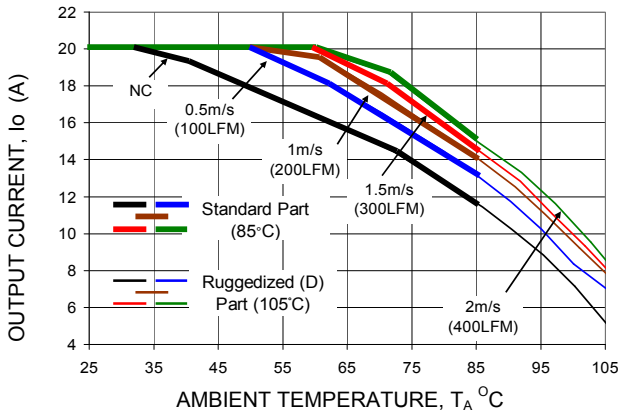


Figure 34. Derating Output Current versus Ambient Temperature and Airflow.

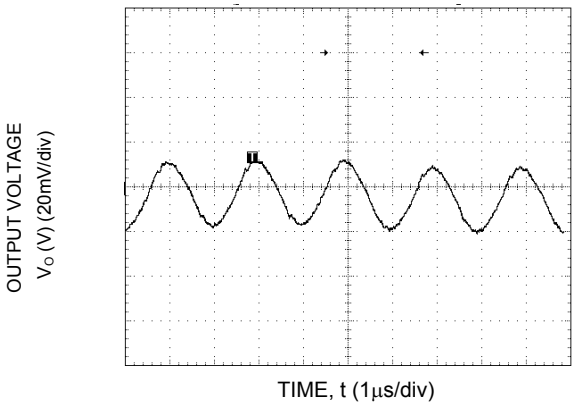


Figure 32. Typical output ripple and noise (V_{IN} = 12V, I_o = $I_{o,max}$).

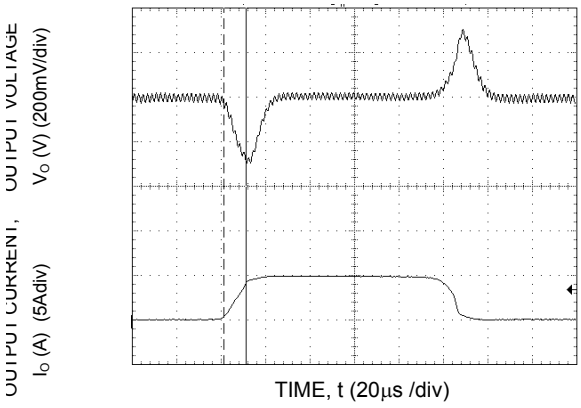


Figure 35. Transient Response to Dynamic Load Change from 0% 50% to 0%.

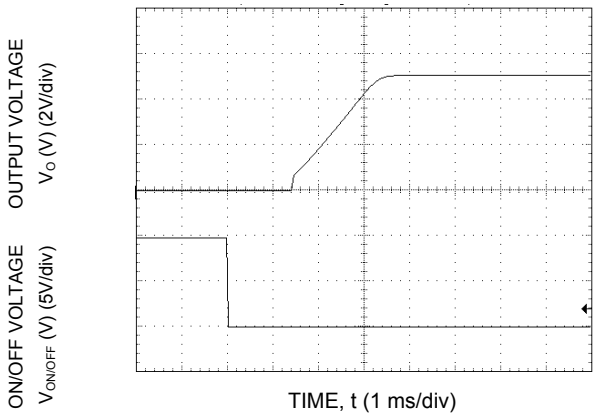


Figure 33. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

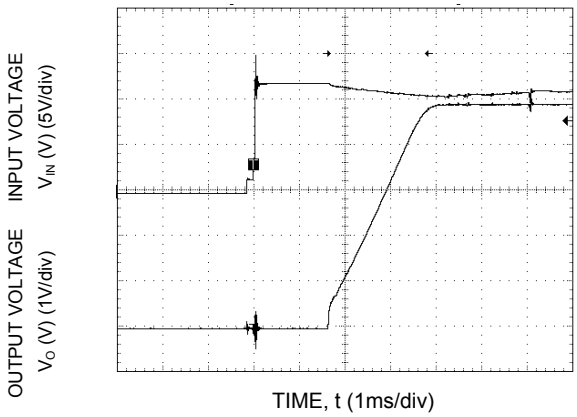
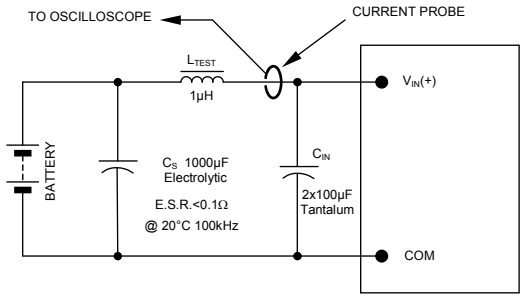


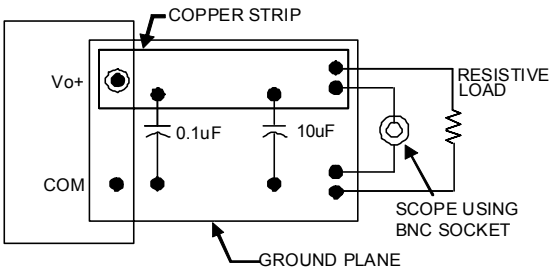
Figure 36. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Test Configurations



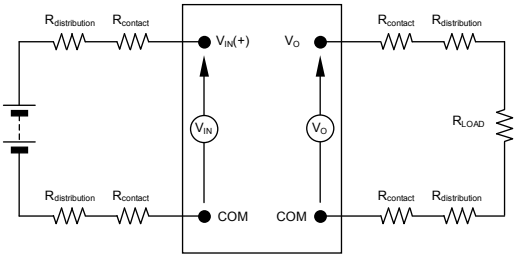
NOTE: Measure input reflected ripple current with a simulated source inductance (L_{TEST}) of 1µH. Capacitor C_S offsets possible battery impedance. Measure current as shown above.

Figure 37. Input Reflected Ripple Current Test Setup.



NOTE: All voltage measurements to be taken at the module terminals, as shown above. If sockets are used then Kelvin connections are required at the module terminals to avoid measurement errors due to socket contact resistance.

Figure 38. Output Ripple and Noise Test Setup.



NOTE: All voltage measurements to be taken at the module terminals, as shown above. If sockets are used then Kelvin connections are required at the module terminals to avoid measurement errors due to socket contact resistance.

Figure 39. Output Voltage and Efficiency Test Setup.

$$\text{Efficiency} \quad \eta = \frac{V_O . I_O}{V_{IN} . I_{IN}} \times 100 \ \%$$

Design Considerations

Input Filtering

The 12V TLynx™ module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, low-ESR polymer and ceramic capacitors are recommended at the input of the module.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 40 shows the input ripple voltage for various output voltages at 20A of load current with 2x22 µF or 3x22 µF ceramic capacitors and an input of 12V.

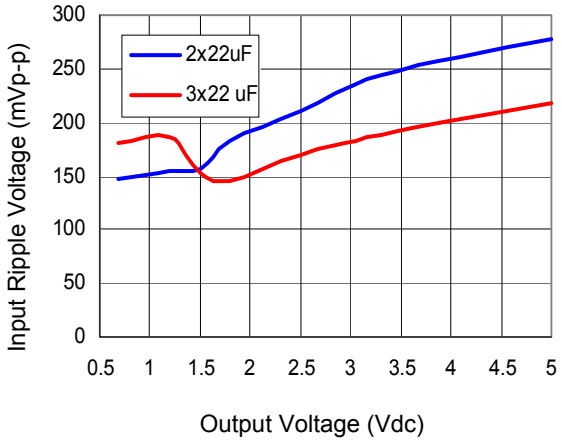


Figure 40. Input ripple voltage for various output voltages with 2x22 µF or 3x22 µF ceramic capacitors at the input (20A load). Input voltage is 12V.

Output Filtering

The 12V TLynx™ modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1 µF ceramic and 10 µF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 41 provides output ripple information for different

external capacitance values at various Vo and for a full load current of 20A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

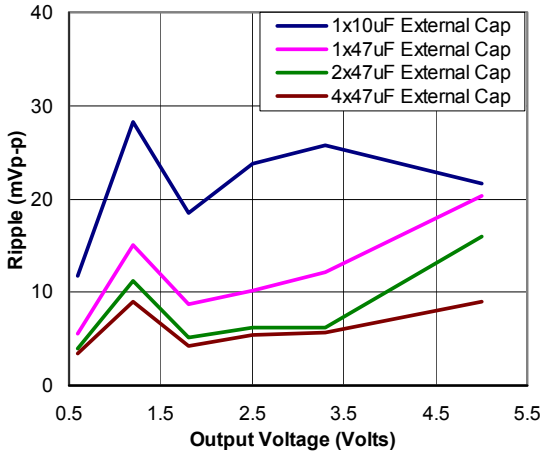


Figure 41. Output ripple voltage for various output voltages with external 1x10 µF, 1x47 µF, 2x47 µF or 4x47 µF ceramic capacitors at the output (20A load). Input voltage is 12V.

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1, CSA C22.2 No. 60950-1-03, and VDE 0850:2001-12 (EN60950-1) Licensed.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast-acting fuse with a maximum rating of 20 A in the positive input lead.

Feature Descriptions

Remote Enable

The 12V TLynx™ modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix “4” – see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (no device code suffix, see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal is always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 42. When the external transistor Q1 is in the OFF state, the internal PWM Enable signal is pulled high through an internal 24.9kΩ resistor and the external pullup resistor and the module is ON. When transistor Q1 is turned ON, the On/Off pin is pulled low and the module is OFF. A suggested value for R_{pullup} is 20kΩ.

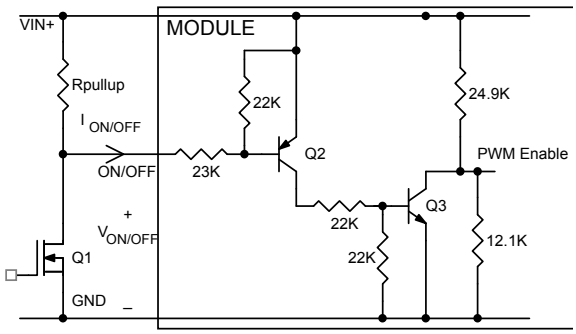


Figure 42. Circuit configuration for using positive On/Off logic.

For negative logic On/Off modules, the circuit configuration is shown in Fig. 43. The On/Off pin should be pulled high with an external pull-up resistor (suggested value for the 4.5V to 14V input range is 20Kohms). When transistor Q1 is in the OFF state, the On/Off pin is pulled high, internal transistor Q2 is turned ON and the module is OFF. To turn the module ON, Q1 is turned ON pulling the On/Off pin low, turning transistor Q2 OFF resulting in the PWM Enable pin going high and the module turning ON.

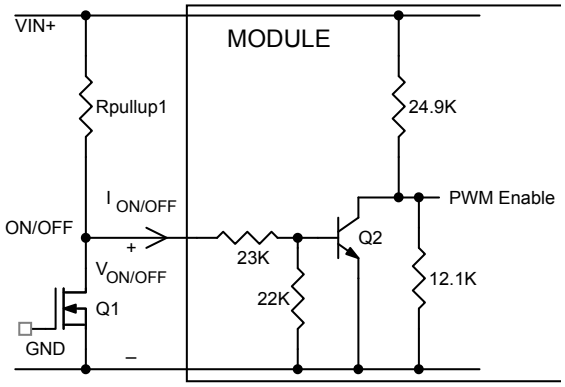


Figure 43. Circuit configuration for using negative On/Off logic.

Overcurrent Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

Over Temperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shutdown if the overtemperature threshold of 135°C is exceeded at the thermal reference point T_{ref} . The thermal shutdown is not intended as a guarantee that the unit will survive temperatures beyond its rating. Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

Output Voltage Programming

The output voltage of the 12V TLynx™ module can be programmed to any voltage from 0.69dc to 5.5Vdc by connecting a resistor between the Trim and GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig. 44. The Upper Limit curve shows that for output voltages of 0.9V and lower, the input voltage must be lower than the maximum of 14V. The Lower Limit curve shows that for output voltages of 3.3V and higher, the input voltage needs to be larger than the minimum of 4.5V.

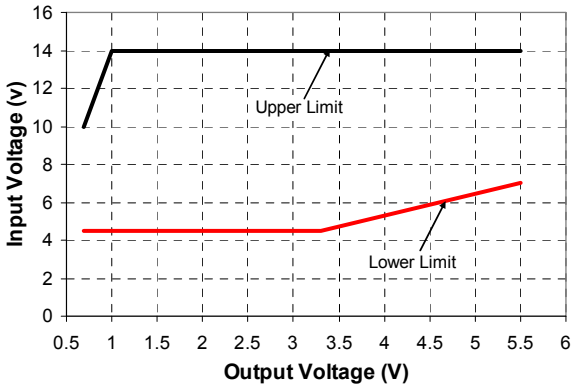


Figure 44. Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

Without an external resistor between Trim and GND pins, the output of the module will be 0.69Vdc. To calculate the value of the trim resistor, *Rtrim* for a desired output voltage, use the following equation:

$$Rtrim = \left[\frac{6.9}{(Vo - 0.69)}\right] k\Omega$$

Rtrim is the external resistor in kΩ

Vo is the desired output voltage.

Table 1 provides Rtrim values required for some common output voltages.

Table 1

$V_{O,\,set}$ (V)	*Rtrim* (KΩ)
0.7	690
1.0	22.26
1.2	13.53
1.5	8.519
1.8	6.216
2.5	3.812
3.3	2.644
5.0	1.601

By using a ±0.5% tolerance trim resistor with a TC of ±100ppm, a set point tolerance of ±1.5% can be achieved as specified in the electrical specification.

Remote Sense

The 12V TLynx™ power modules have a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the S+ and S– pins. The voltage between the S– and GND pins of the module must not drop below –0.2V. If Remote

Sense is being used, the voltage between S+ and S– cannot be more than 0.5V larger than the voltage between VOUT and GND. Note that the output voltage of the module cannot exceed the specified maximum value. When the Remote Sense feature is not being used, connect the S+ pin to the VOUT pin and the S– pin to the GND pin.

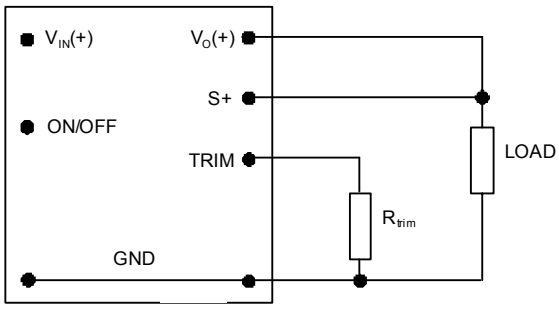


Figure 45. Circuit configuration for programming output voltage using an external resistor.

Voltage Margining

Output voltage margining can be implemented in the 12V TLynx™ modules by connecting a resistor, $R_{margin-up}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{margin-down}$, from the Trim pin to output pin for margining-down. Figure 46 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at www.lineagepower.com under the Design Tools section, also calculates the values of $R_{margin-up}$ and $R_{margin-down}$ for a specific output voltage and % margin. Please consult your local Lineage Power Technical Representative for additional details.

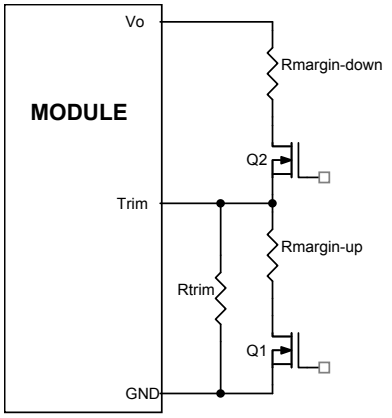


Figure 46. Circuit Configuration for margining Output voltage

Monotonic Start-up and Shutdown

The 12V TLynx™ modules have monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

Startup into Pre-biased Output

The 12V Pico TLynx™ 20A modules can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage. Note that prebias operation is not supported when output voltage sequencing is used.

Output Voltage Sequencing

The 12V TLynx™ modules include a sequencing feature, EZ-SEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, either tie the SEQ pin to V_{IN} or leave it unconnected.

When an analog voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the SEQ voltage must be set higher than the set-point voltage of the module. The output voltage follows the voltage on the SEQ pin on a one-to-one volt basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

For proper voltage sequencing, first, input voltage is applied to the module. The On/Off pin of the module is left unconnected (or tied to GND for negative logic modules or tied to V_{IN} for positive logic modules) so that the module is ON by default. After applying input voltage to the module, a minimum 10msec delay is required before applying voltage on the SEQ pin. During this time, a voltage of 50mV (± 20 mV) is maintained on the SEQ pin. This delay gives the module enough time to complete its internal power-up soft-start cycle. During the delay time, the SEQ pin should be held close to ground (nominally 50mV ± 20 mV). This is required to keep the internal op-amp out of saturation thus preventing output overshoot during the start of the sequencing ramp. By selecting resistor R1 (see fig. 47) according to the following equation

$$R1 = \frac{24950}{V_{IN} - 0.05} \text{ ohms,}$$

the voltage at the sequencing pin will be 50mV when the sequencing signal is at zero.

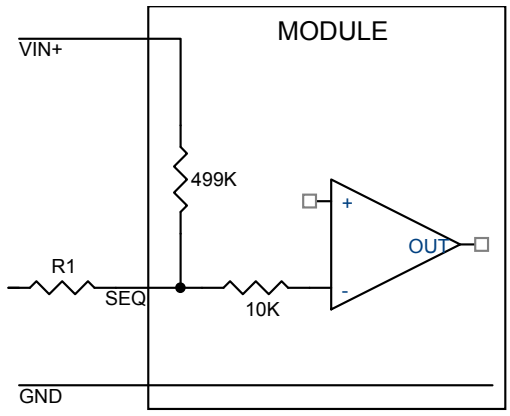


Figure 47. Circuit showing connection of the sequencing signal to the SEQ pin.

After the 10msec delay, an analog voltage is applied to the SEQ pin and the output voltage of the module will track this voltage on a one-to-one volt bases until the output reaches the set-point voltage. To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

When using the EZ-SEQUENCE™ feature to control start-up of the module, pre-bias immunity during start-up is disabled. The pre-bias immunity feature of the module relies on the module being in the diode-mode during start-up. When using the EZ-SEQUENCE™ feature, modules goes through an internal set-up time of 10msec, and will be in synchronous rectification mode when the voltage at the SEQ pin is applied. This will result in the module sinking current if a pre-bias voltage is present at the output of the module. When pre-bias immunity during start-up is required, the EZ-SEQUENCE™ feature must be disabled. For additional guidelines on using the EZ-SEQUENCE™ feature please refer to Application Note AN04-008 "Application Guidelines for Non-Isolated Converters: Guidelines for Sequencing of Multiple Modules", or contact the Lineage Power Technical representative for additional information.

Power Good

The 12V TLynx™ modules provide a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going ±11% outside the setpoint value. The PGOOD terminal should be connected through a pullup resistor (suggested value 100KΩ) to a source of 6VDC or less.

Synchronization

The 12V TLynx™ series of modules can be synchronized using an external signal. Details of the SYNC signal are provided in the Electrical Specifications table. If the synchronization function is not being used, leave the SYNC pin floating.

Tunable Loop™

The 12V TLynx™ 20A modules have a new feature that optimizes transient response of the module called Tunable Loop™.

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Figure 41) and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the SENSE and TRIM pins of the module, as shown in Fig. 47. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

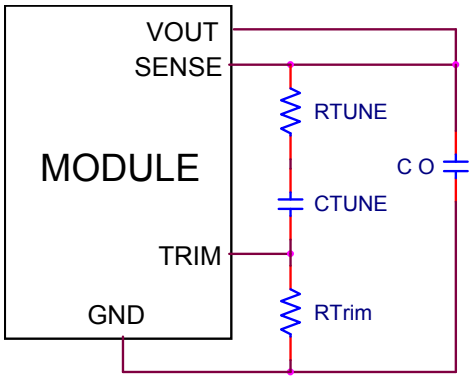


Figure. 48. Circuit diagram showing connection of R_{TUME} and C_{TUNE} to tune the control loop of the module.

Recommended values of R_{TUNE} and C_{TUNE} for different output capacitor combinations are given in Tables 2 and 3. Table 2 shows the recommended values of R_{TUNE} and C_{TUNE} for different values of ceramic output capacitors up to 940μF that might be needed for an

application to meet output ripple and noise requirements. Selecting R_{TUNE} and C_{TUNE} according to Table 2 will ensure stable operation of the module.

In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of R_{TUNE} and C_{TUNE} in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 10A to 20A step change (50% of full load), with an input voltage of 12V.

Please contact your Lineage Power technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values or input voltages other than 12V.

Table 2. General recommended values of of R_{TUNE} and C_{TUNE} for Vin=12V and various external ceramic capacitor combinations.

Co	1x47µF	2x47µF	4x47µF	10x47µF	20x47µF
R_{TUNE}	240	240	240	150	150
C_{TUNE}	1500pF	2700pF	5600pF	12nF	15nF

Table 3. General Recommended values of R_{TUNE} and C_{TUNE} to obtain transient deviation of 2% of Vout for a 10A step load with Vin=12V.

Vo	5V	3.3V	2.5V	1.8V	1.2V	0.69V
Co	6x47µF	5x47µF + 330µF Polymer	2x 330µF Polymer	6x47µF + 2x330µF Polymer	6x47µF + 4x330µF Polymer	12 x330µF Polymer
R_{TUNE}	220	220	200	150	150	150
C_{TUNE}	5600pF	7500pF	18nF	33nF	120nF	120nF
ΔV	99mV	66mV	50mV	36mV	24mV	12mV

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 49. The preferred airflow direction for the module is in Figure 50. The derating data applies to airflow in either direction of the module's long axis.

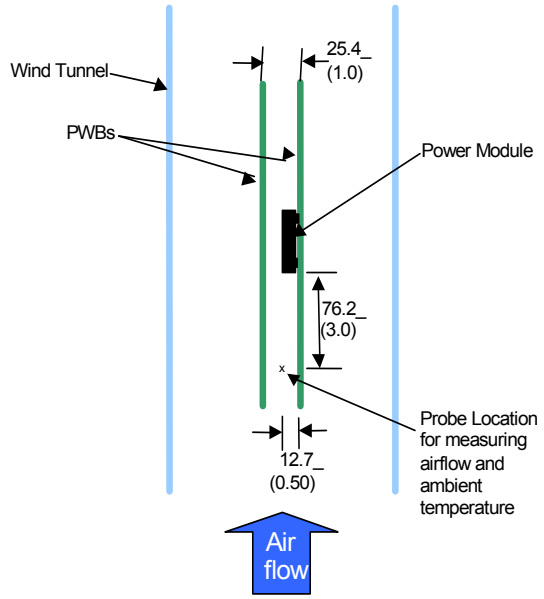


Figure 49. Thermal Test Setup.

The thermal reference points, T_{ref} used in the specifications are also shown in Figure 50. For reliable operation the temperatures at these points should not exceed 125°C. The output power of the module should not exceed the rated power of the module (Vo,set x Io,max).

Please refer to the Application Note "Thermal Characterization Process For Open-Frame Board-Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures.

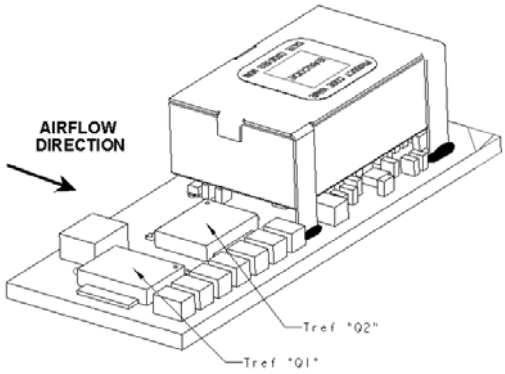


Figure 50. Preferred airflow direction and location of hot-spot of the module (Tref).

Modules marked ruggedized with a "D" suffix operate up to an ambient of 105°C. For the remaining types de-rating curves for individual output voltages meet existing specifications up to 85°C.

Shock and Vibration

The ruggedized (-D version) of the modules are designed to withstand elevated levels of shock and vibration to be able to operate in harsh environments. The ruggedized modules have been successfully tested to the following conditions:

Non operating random vibration:
Random vibration tests conducted at 25C, 10 to 2000Hz, for 30 minutes each level, starting from 30Grms (Z axis) and up to 50Grms (Z axis). The units were then subjected to two more tests of 50Grms at 30 minutes each for a total of 90 minutes.

Operating shock to 40G per Mil Std. 810F, Method 516.4 Procedure I:
The modules were tested in opposing directions along each of three orthogonal axes, with waveform and amplitude of the shock impulse characteristics as follows:

All shocks were half sine pulses, 11 milliseconds (ms) in duration in all 3 axes.

Units were tested to the Functional Shock Test of MIL-STD-810, Method 516.4, Procedure I - Figure 516.4-4. A shock magnitude of 40G was utilized. The operational units were subjected to three shocks in each direction along three axes for a total of eighteen shocks.

Operating vibration per Mil Std 810F, Method 514.5 Procedure I:

The ruggedized (-D version) modules are designed and tested to vibration levels as outlined in MIL-STD-810F, Method 514.5, and Procedure 1, using the Power Spectral Density (PSD) profiles as shown in Table 1 and Table 2 for all axes. Full compliance with performance specifications was required during the performance test. No damage was allowed to the module and full compliance to performance specifications was required when the endurance environment was removed. The module was tested per MIL-STD-810, Method 514.5, Procedure I, for functional (performance) and endurance random vibration using the performance and endurance levels shown in Table 1 and Table 2 for all axes. The performance test has been split, with one half accomplished before the endurance test and one half after the endurance test (in each axis). The duration of the performance test was at least 16 minutes total per axis and at least 120 minutes total per axis for the endurance test. The endurance test period was 2 hours minimum per axis.

Table 1: Performance Vibration Qualification - All Axes

Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)
10	1.14E-03	170	2.54E-03	690	1.03E-03
30	5.96E-03	230	3.70E-03	800	7.29E-03
40	9.53E-04	290	7.99E-04	890	1.00E-03
50	2.08E-03	340	1.12E-02	1070	2.67E-03
90	2.08E-03	370	1.12E-02	1240	1.08E-03
110	7.05E-04	430	8.84E-04	1550	2.54E-03
130	5.00E-03	490	1.54E-03	1780	2.88E-03
140	8.20E-04	560	5.62E-04	2000	5.62E-04

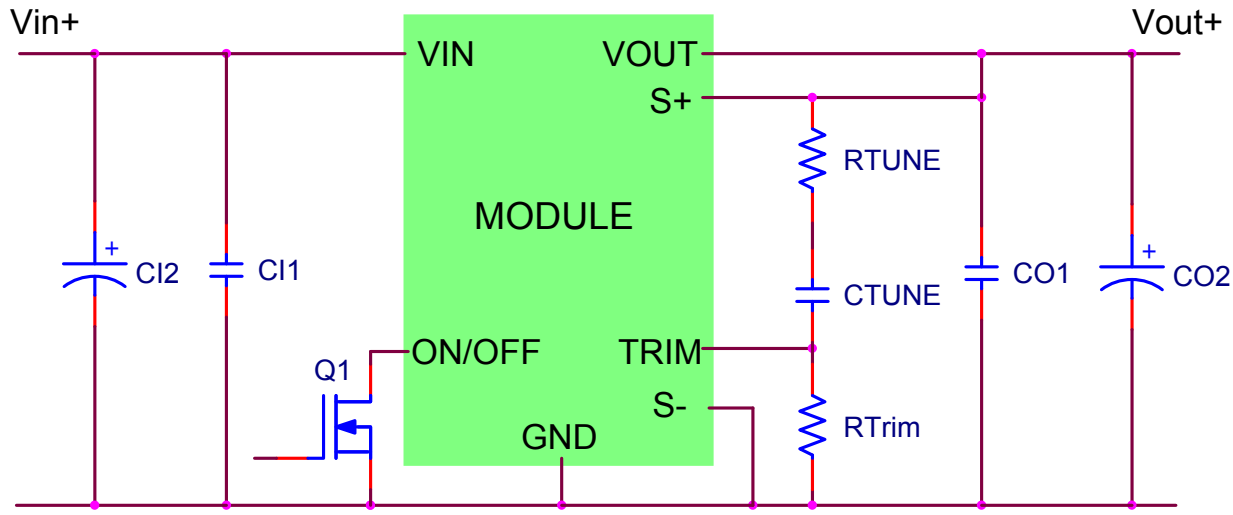
Table 2: Endurance Vibration Qualification - All Axes

Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)
10	0.00803	170	0.01795	690	0.00727
30	0.04216	230	0.02616	800	0.05155
40	0.00674	290	0.00565	890	0.00709
50	0.01468	340	0.07901	1070	0.01887
90	0.01468	370	0.07901	1240	0.00764
110	0.00498	430	0.00625	1550	0.01795
130	0.03536	490	0.01086	1780	0.02035
140	0.0058	560	0.00398	2000	0.00398

Example Application Circuit

Requirements:

Vin:	**12V**
Vout:	**1.8V**
Iout:	**15A max., worst case load transient is from 10A to 15A**
ΔVout:	**1.5% of Vout (36mV) for worst case load transient**
Vin, ripple	**1.5% of Vin (180mV, p-p)**



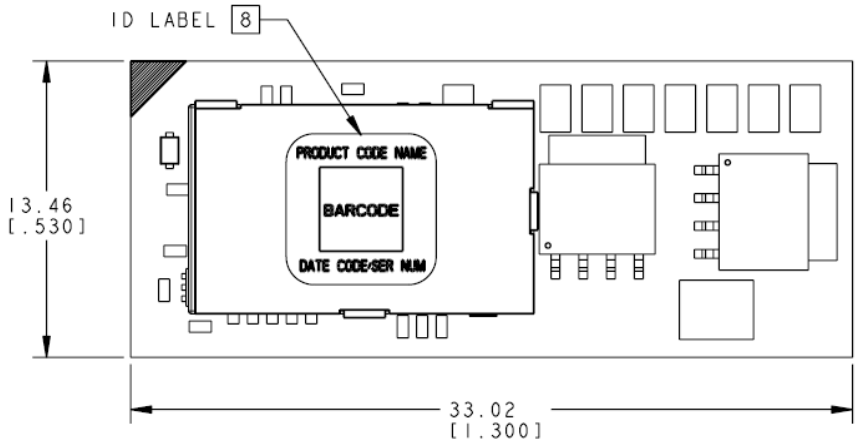
CI1	2 x 22μF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)
CI2	200μF/16V bulk electrolytic
CO1	5 x 47μF/6.3V ceramic capacitor (e.g. Murata GRM31CR60J476ME19)
CO2	2 x 330μF/6.3V Polymer (e.g. Sanyo, Poscap)
CTune	22nF ceramic capacitor (can be 1206, 0805 or 0603 size)
RTune	150 ohms SMT resistor (can be 1206, 0805 or 0603 size)
RTrim	6.19kΩ SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

Mechanical Outline

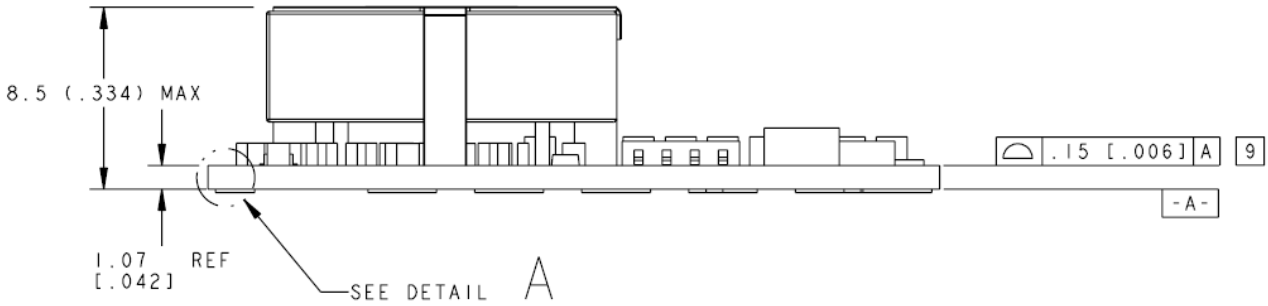
Dimensions are in millimeters and (inches).

Tolerances: x.xx in. ± 0.02 in. (x.x mm ± 0.5 mm) [unless otherwise indicated]

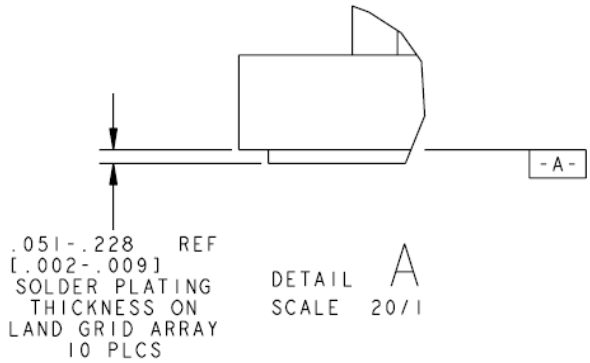
x.xxx in ± 0.010 in. (x.xx mm ± 0.25 mm)



Top View



Side View

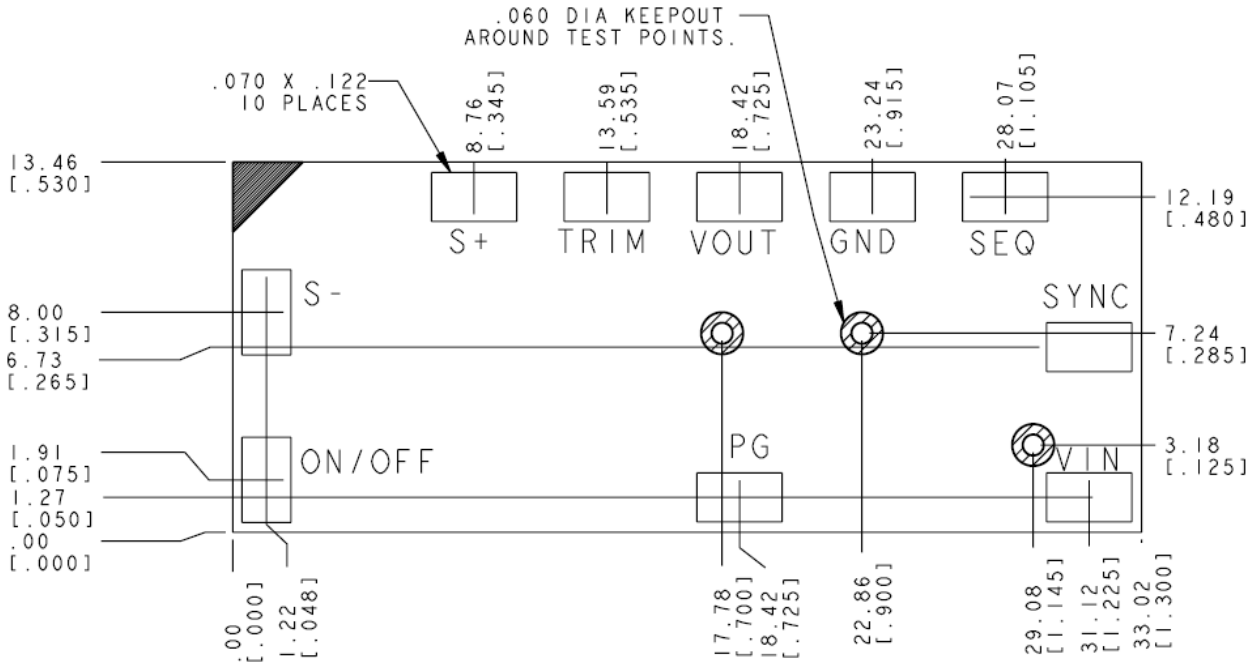


Recommended Pad Layout

Dimensions are in millimeters and (inches).

Tolerances: x.xx in. ± 0.02 in. (x.x mm ± 0.5 mm) [unless otherwise indicated]

x.xxx in ± 0.010 in. (x.xx mm ± 0.25 mm)



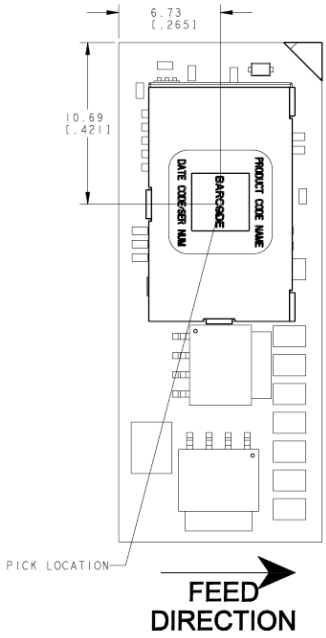
RECOMMENDED FOOTPRINT
-THRU THE BOARD-

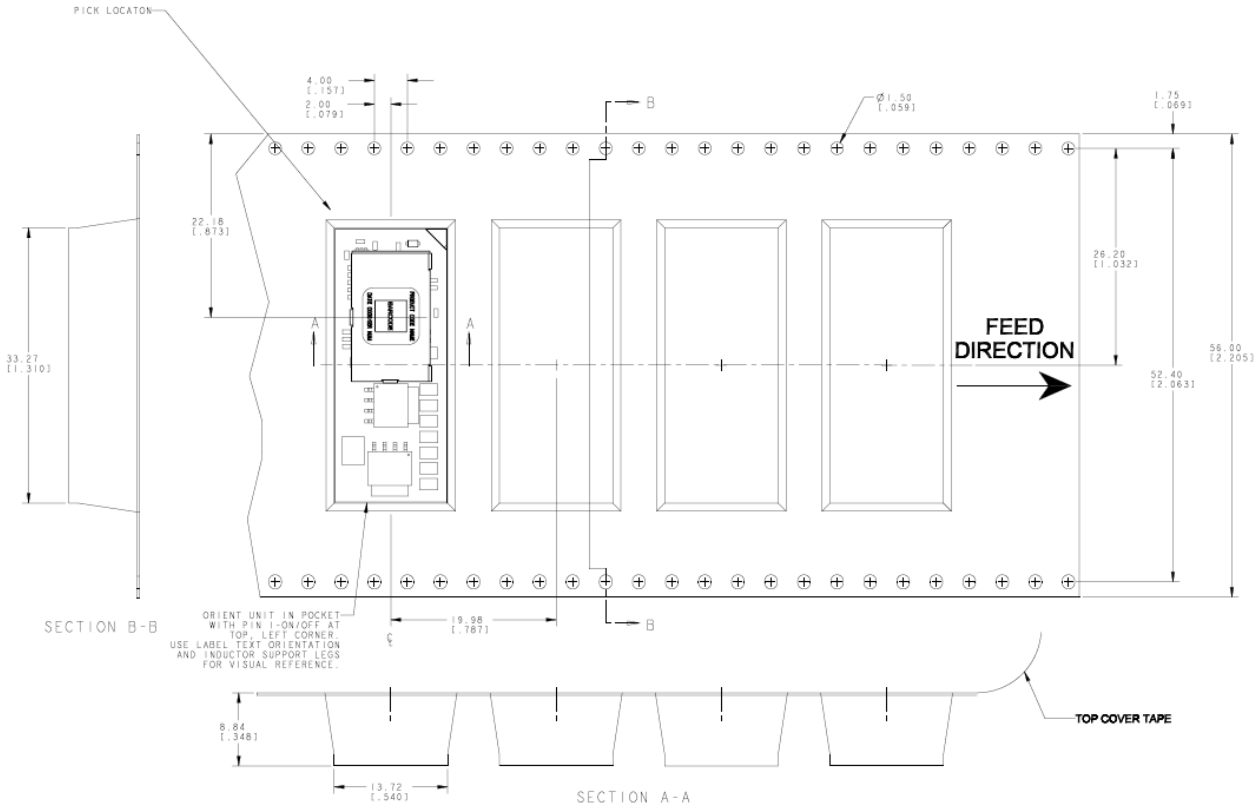
PIN	FUNCTION
1	ON/OFF
2	VIN
3	SEQ
4	GND
5	VOUT
6	TRIM
7	S+
8	S-
9	PGOOD
10	SYNC

Packaging Details

The 12V TLynx™ modules are supplied in tape & reel as standard. Modules are shipped in quantities of 250 modules per reel.

All Dimensions are in millimeters and (in inches).





Reel Dimensions:

Outside Dimensions:	330.2 mm (13.00”)
Inside Dimensions:	177.8 mm (7.00”)
Tape Width:	24.00 mm (0.945”)

Surface Mount Information

Pick and Place

The 12V TLynx™ modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Lead Free Soldering

The 12V TLynx™ modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. C (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 50. Soldering outside of the recommended profile requires testing to verify results and performance.

MSL Rating

The 12V TLynx™ modules have a MSL rating of 2.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of ≤ 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

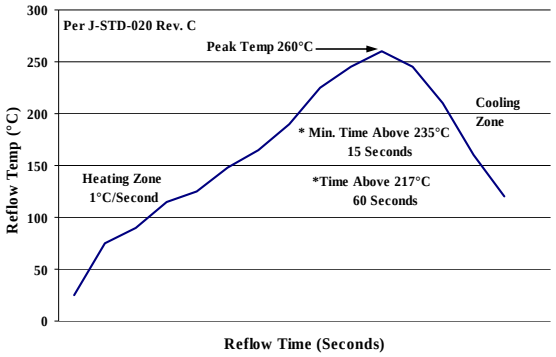


Figure 50. Recommended linear reflow profile using Sn/Ag/Cu solder.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning* Application Note (AN04-001).

Ordering Information

Please contact your Lineage Power Sales Representative for pricing, availability and optional features.

Table 4. Device Codes

Device Code	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Comcodes
APTS020A0X3-SRZ	4.5 – 14Vdc	0.69 – 5.5Vdc	20A	Negative	CC109127115
APTS020A0X43-SRZ	4.5 – 14Vdc	0.69 – 5.5Vdc	20A	Positive	CC109127123
APTS020A0X3-SRDZ	4.5 – 14Vdc	0.69 – 5.5Vdc	20A	Negative	CC109150232

Table 5. Coding Scheme

TLynx family	Sequencing feature.	Input voltage range	Output current	Output voltage	On/Off logic	Options		ROHS Compliance
AP	**T**	**S**	**020A0**	**X**	**4**	**-SR**	**-D**	**Z**
	T = with Seq. X = w/o Seq.	S = 4.5 - 14V	20.0A	X = programmable output	4 = positive No entry = negative	S = Surface Mount R = Tape&Reel	D = 105C operating ambient, 40G operating shock as per MIL Std 810F	Z = ROHS6

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