

Document Title**1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM****Revision History**

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Dec. 22 nd , 2003	Preliminary
0.1	Add Direct DPD Modify MRS Entry Modify PASR Current	Mar. 15 th , 2004	Preliminary
0.2	Change speed from 60nsec to 55nsec Modify ISB1, PASR Current	Sep. 21 th , 2004	Final
0.3	Modified functional description & MRS update timing Minor Changes	Nov. 8 th , 2004	Final
0.4	Added <u>G(Pb-Free)</u> and <u>H(Pb-Free & Halogen Free)</u> descriptions	Nov. 1 st , 2005	Final
0.5	Add AC Parameter (tCP)	Jul. 25 th , 2006	Final

1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 1M x 16
- Power Supply Voltage : 2.7~3.3V
- Low Power & Page Modes
 - CMP1617BX1 : support the PASR/MRS DPD function
 - CMP1617BX2 : support the Direct DPD function
 - CMP1617BX4 : support the PASR/MRS DPD/PAGE function
 - CMP1617BX5 : support the Direct DPD/PAGE function
- Three state output and TTL Compatible
- Package Type : 48-FBGA-6.00x8.00 mm²
- Separated I/O power(VCCQ) & Core Power(VCC)
- Page read/write operation by 16 words (CMP1617BA4, CMP1617BA5)
- DPD mode by using MRS only (CMP1617BA1, CMP1617BA4)
- Direct DPD mode when /ZZ goes low (CMP1617BA2, CMP1617BA5)

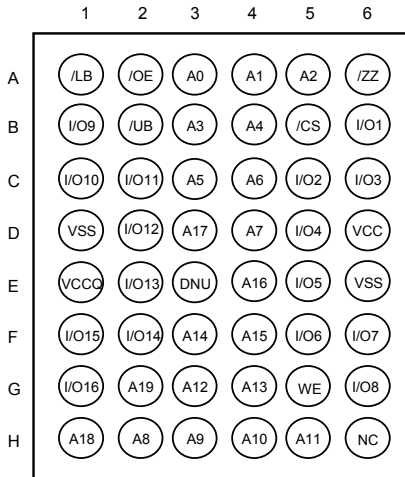
PRODUCT FAMILY

Product Family	Operating Temperature	Operating Voltage (V)			Speed	Power Dissipation					
		Min.	Typ.	Max.		ICC1		ICC2		ISB1 (CMOS Standby Current)	
						f = 1MHz		f = fmax			
						Typ.	Max.	Typ.	Max.	Typ.	Max.
CMP1617BAx-F60E CMP1617BAx-F70E	Extended (-25~85°C)	2.7	3.0	3.3	60ns 70ns	1.5mA	3mA	15mA 12mA	25mA	50uA	100uA

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (typ) and T_A = 25C.

2. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

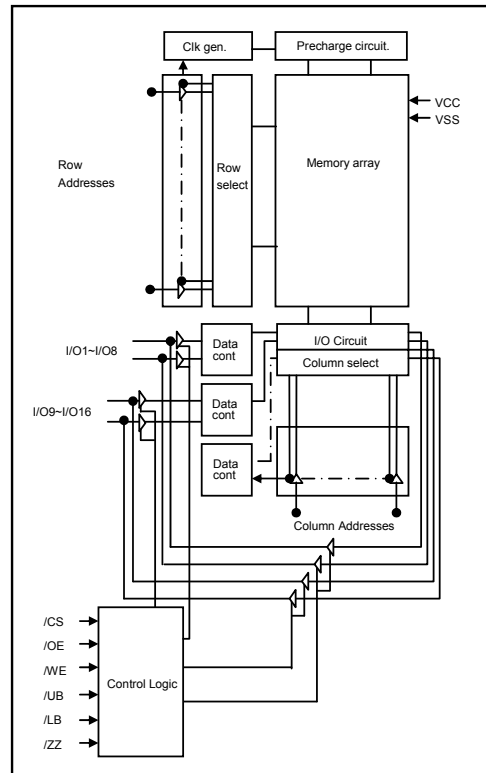
PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
/ZZ	Low Power Modes	VCC	Core Power
/CS	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A19	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use
NC	No Connection		

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Extended Temperature Products(-25~85°C)	
Part Name	Function
CMP1617BAx-F60E	48-FBGA, 60ns, VCC=3.0V, VCCQ=3.0V(2.5V,1.8V)
CMP1617BAx-F70E	48-FBGA, 70ns, VCC=3.0V, VCCQ=3.0V(2.5V,1.8V)

1. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

FUNCTIONAL DESCRIPTION

/CS	/ZZ	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Direct DPD ²⁾
H	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Low Power Modes ³⁾
X ¹⁾	H	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

2. In case of CMP1617BA2 & CMP1617BA5 product

3. In case of CMP1617BA1 & CMP1617BA4 product

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.2 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 3.6	V
Power Dissipation	PD	1.0	W
Storage temperature	TSTG	-65 to 150	°C
Operating Temperature	TA	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	CMP1617BA						Unit
		Min	Max	Min	Max	Min	Max	
Supply voltage	VCC	2.7	3.3	2.7	3.3	2.7	3.3	V
I/O operating voltage (VCCQ ≤ VCC)	VCCQ	2.7	3.3	2.25	2.75	1.65	1.95	V
Ground	VSS	0	0	0	0	0	0	V
Input high voltage	VIH	0.8VCCQ	VCC+0.2 ²⁾	0.8VCCQ	VCC+0.2 ²⁾	0.8VCCQ	VCC+0.2 ²⁾	V
Input low voltage	VIL	-0.2 ³⁾	0.2VCCQ	-0.2 ³⁾	0.2VCCQ	-0.2 ³⁾	0.2VCCQ	V

Note :

1.TA=-25 to 85°C, otherwise specified.

2. Overshoot : Vcc+1.0V in case of pulse width≤20ns.

3. Undershoot : -1.0V in case of pulse width≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

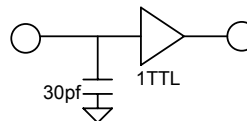
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	uA
Output leakage current	I _{LO}	/CS=V _{IH} , /ZZ=V _{IH} , /OE=V _{IH} or /WE=V _L , V _{IO} =V _{SS} to V _{CC}	-1	-	1	uA
Average operating current	I _{CC1}	Cycle time=1us, 100%duty, I _{IO} =0mA, /CS≤0.2V, /ZZ=V _{IH} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	3	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, /CS=V _L , /ZZ=V _{IH} , V _{IN} =V _L or V _{IH}	-	-	25	mA
Output low voltage	V _{OL}	I _{OL} =0.5mA			0.2V _{CCQ}	V
Output high voltage	V _{OH}	I _{OH} =-0.5mA	0.8V _{CCQ}			V
Standby Current(TTL)	ISB	/CS=V _{IH} , /ZZ=V _{IH} , Other inputs=V _{IH} or V _L	-	-	0.3	mA
Standby Current(CMOS)	ISB1	/CS≥V _{CC} -0.2V, /ZZ≥V _{CC} -0.2V, Other inputs=0~V _{CC}	-	-	100	uA
Low Power Modes	ISB0	/ZZ≤0.2V, Other inputs=0~V _{CC} , No refresh(DPD)	-	-	10	uA
	ISB0a	/ZZ≤0.2V, Other inputs=0~V _{CC} , ¼ refresh area selection	-	-	55	uA
	ISB0b	/ZZ≤0.2V, Other inputs=0~V _{CC} , ½ refresh area selection	-	-	70	uA
	ISB0c	/ZZ≤0.2V, Other inputs=0~V _{CC} , All refresh area selection	-	-	100	uA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.2 to VCC-0.2V
 Input rising and falling time : 5ns
 Input and output reference voltage : 0.5*VCCQ
 Output load (see right) : CL=30pF+1TTL



AC CHARACTERISTICS (VCC=2.7V~3.3V, Extended product : TA=-25 to 85°C)

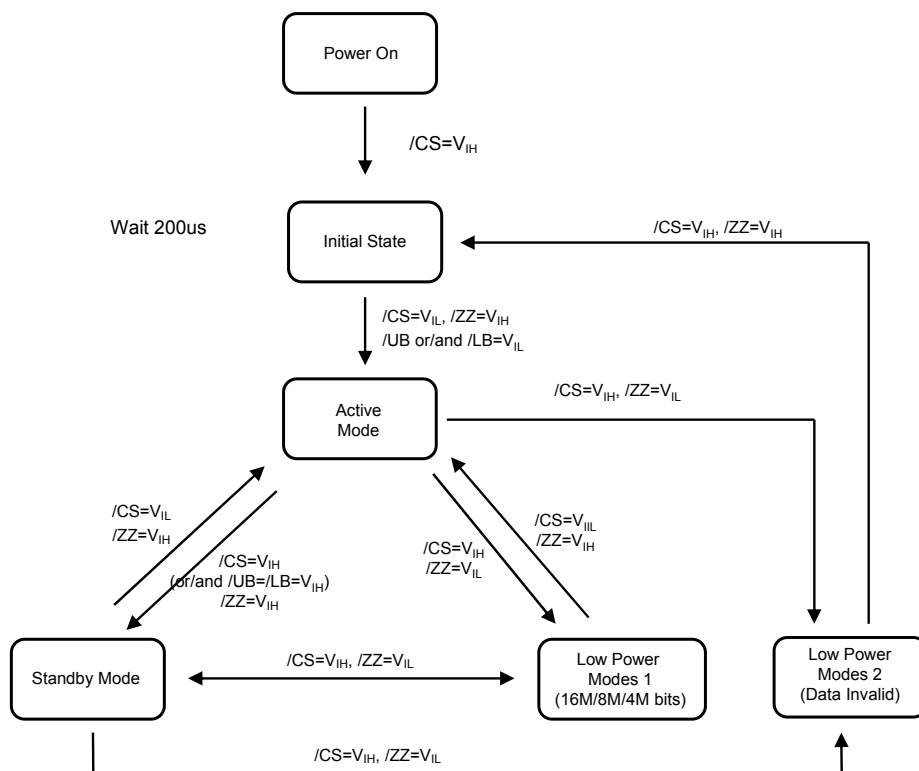
Parameter List		Symbol	Speed Bins				Units
			60ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	60	40k	70	40k	ns
	Address Access Time	tAA	-	60	-	70	ns
	Chip Select to Output	tCO	-	60	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	25	ns
	/UB, /LB Access Time	tBA	-	60	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	0	5	ns
Output Hold from Address Change	tOH	5	-	5	-	ns	
Write	Write Cycle Time	tWC	60	40k	70	40k	ns
	Chip Select to End of Write	tCW	50	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	50	-	60	-	ns
	/UB, /LB Valid to End of Write	tBW	50	-	60	-	ns
	Write Pulse Width	tWP	50	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	5	0	5	ns
	Data to Write Time Overlap	tDW	20	-	20	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	5	-	5	-	ns	
Page	Page Mode Cycle Time	tPC	25	-	25	-	ns
	Page Mode Address Access Time	tPAA	-	25	-	25	ns
	Maximum Cycle Time	tMRC	-	40k	-	40k	ns
/CS High Pulse Width		tCP	10	-	10	-	ns

1. /CS High Pulse Width is defined by /CS or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CS=V_{IH}

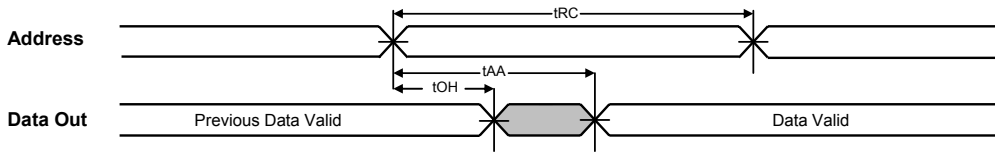
Standby Mode State machines



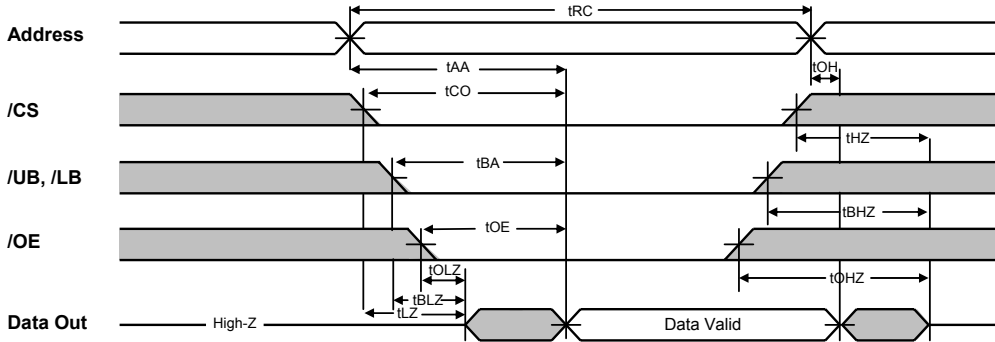
Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	100 (ISB1)	0
Low Power Modes	Invalid	10 (ISB0)	200
	¼ valid	55 (ISB0a)	0
	½ valid	70 (ISB0b)	0
	valid	100 (ISB0c)	0

READ CYCLE (1) (Address controlled, /CS=/OE=VIL, /ZZ=/WE=VIH, /UB or/and /LB=VIL)

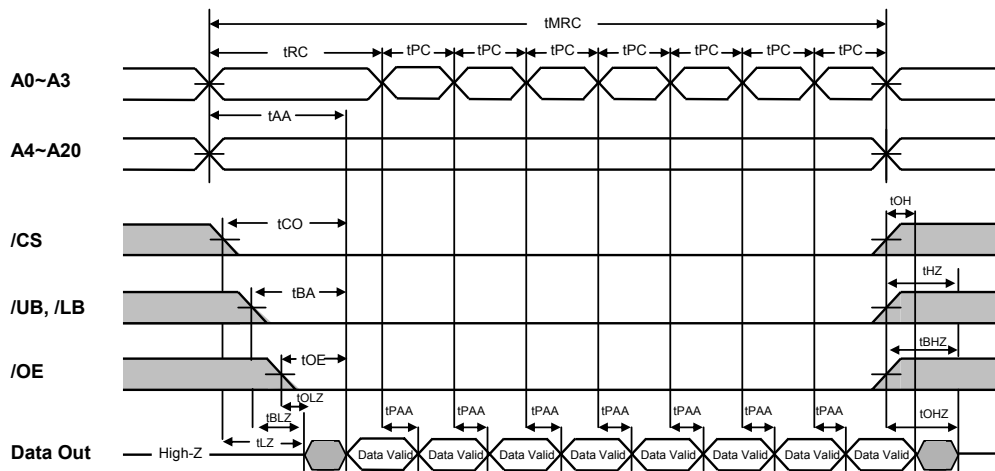


READ CYCLE (2) (/ZZ=/WE=VIH)



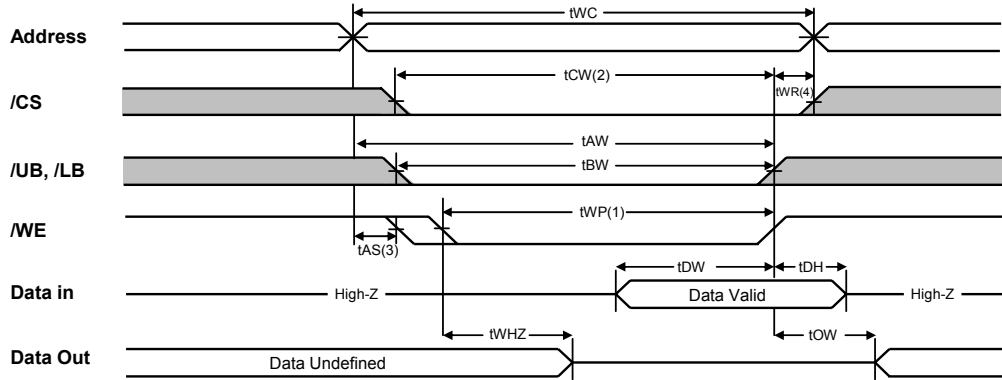
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 40 μ s.

PAGE READ CYCLE (/ZZ=/WE=VIH, 16 words access)

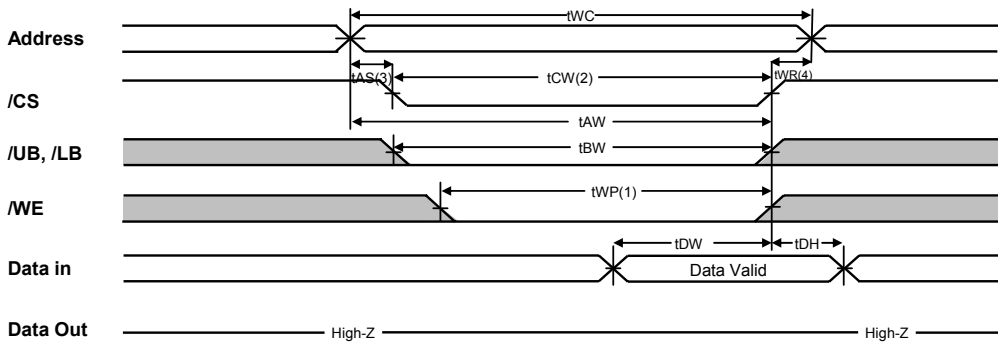


1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 40 μ s.

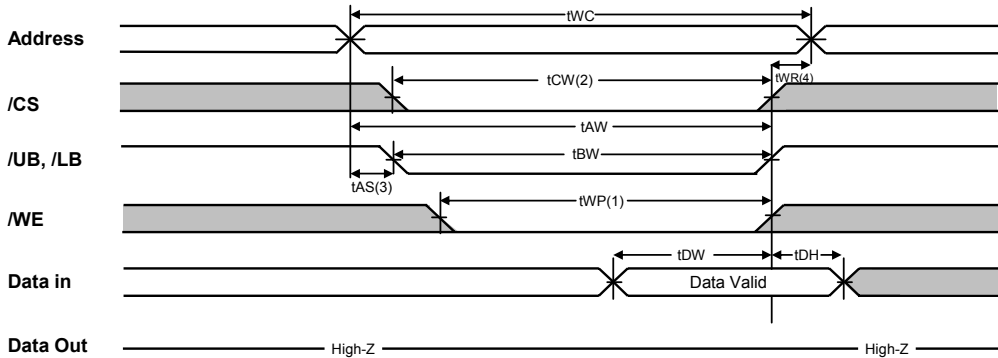
WRITE CYCLE (1) (/WE controlled, /ZZ=VIH)



WRITE CYCLE (2) (/CS controlled, /ZZ=/WE=VIH)

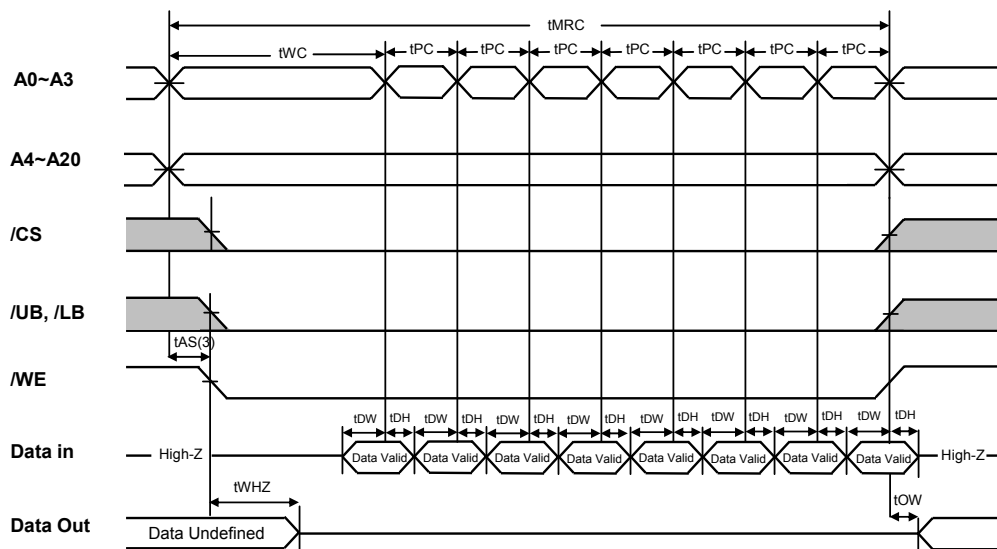


WRITE CYCLE (3) (/UB, /LB controlled, /ZZ=VIH)



1. A write occurs during the overlap (t_{WP}) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the /CS going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 40us.

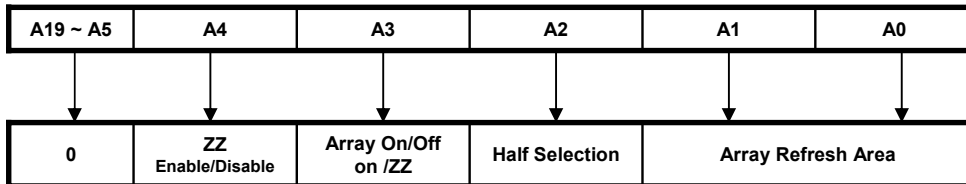
PAGE WRITE CYCLE (Address controlled, /ZZ=VIH)



1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and /WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 40us.

LOW POWER MODES

1. Mode Register Set



/ZZ Enable/Disable

A4	Type
0	Deep Power Down Enable
1	DPD Disable (Default)

Note: If the register is written to enable the Deep Power Down, the part will go into Deep Power Down during the following time that /ZZ is driven low and there is no MRS update. When /ZZ is driven high, all of the register settings will return to default state for the part (i.e. full array refresh, Deep Power Down Disabled).

Array On/Off on /ZZ

A3	Type
0	Partial Array Refresh Mode (Default)
1	Reduced Memory Size Mode

Note: The RMS(Reduced Memory Size) mode is enabled after /ZZ goes high and remains enabled after /ZZ goes high. To change to a different mode, the mode register will have to be rewritten.

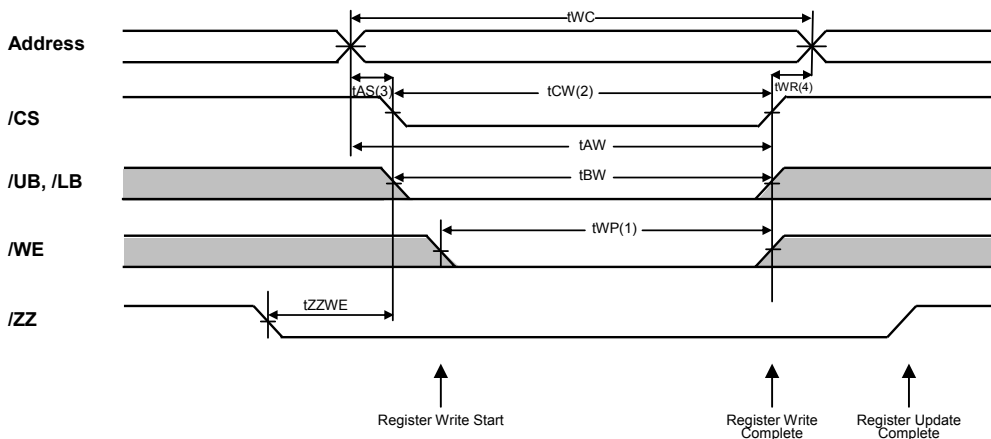
Half Selection (Top / Bottom)

A2	Type
0	Bottom (Default)
1	Top

Array Refresh Area

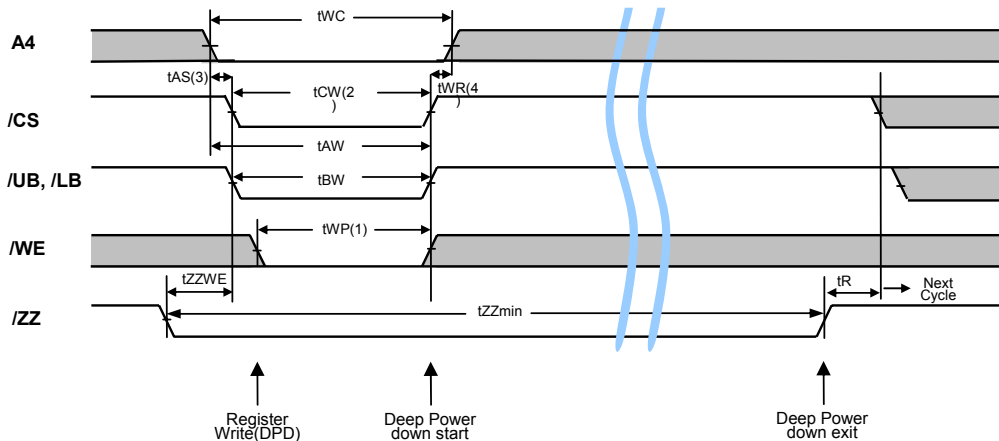
A1	A0	Type
0	0	Full Array (Default)
0	1	RFU
1	0	½ Array
1	1	¼ Array

2. MRS Update



The register update take place on the rising edge of /ZZ. Once the register is updated, the next time /ZZ goes low, without any updates to the register starting within the tZZWE max time of 1us, the part will refresh the array selected. The data bus is a don't care When /ZZ is low during the register updates.

3. Deep Power Down Mode Entry/Exit



Parameter	Description	Min	Max	Units
tZZWE	ZZ low to Write Enable Low	0	1	us
tR(Deep Power Down Mode only)	Operation Recovery Time	200	-	us
tZZmin	Low Power Mode Time	10	-	us

4. Address Information

Partial Array Refresh Mode (A3=0, A4=1)

A2	A1,A0	Refresh Section	Address	Size	Density
0	11	1/4	00000h-3FFFFh	256Kbx16	4Mb
0	10	1/2	00000h-7FFFFh	512Kbx16	8Mb
X	00	Full	00000h-FFFFFFh	1Mbx16	16Mb
1	11	1/4	C0000h-FFFFFFh	256Kbx16	4Mb
1	10	1/2	80000h-FFFFFFh	512Kbx16	8Mb

Reduced Memory Size Mode (A3=1, A4=1)

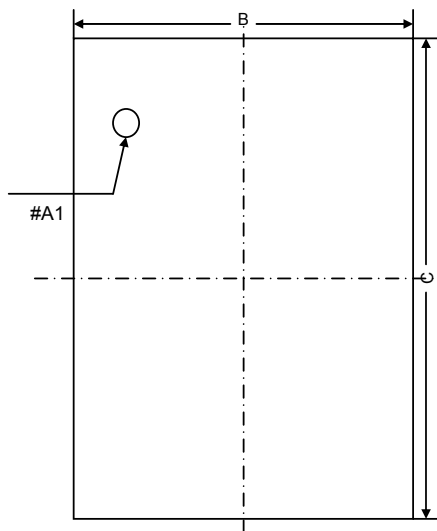
A2	A1,A0	Refresh Section	Address	Size	Density
0	11	1/4	00000h-3FFFFh	256Kbx16	4Mb
0	10	1/2	00000h-7FFFFh	512Kbx16	8Mb
1	11	1/4	C0000h-FFFFFFh	256Kbx16	4Mb
1	10	1/2	80000h-FFFFFFh	512Kbx16	8Mb

PACKAGE DIMENSION

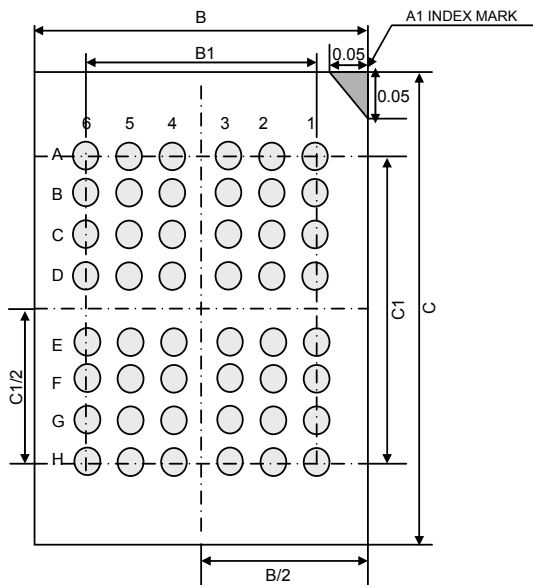
Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

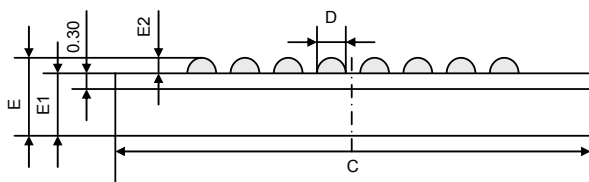
Top View



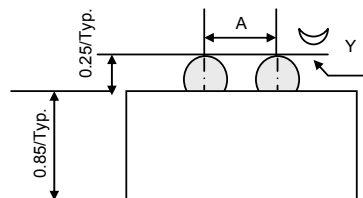
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

- Bump counts : 48(8row x 6column)
- Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
- All tolerance are +/-0.050 unless otherwise specified.
- Typ : Typical
- Y is coplanarity : 0.08(Max)