GAL22V10/883

High Performance E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 166 MHz**
  - **— 7ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 12 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices**
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

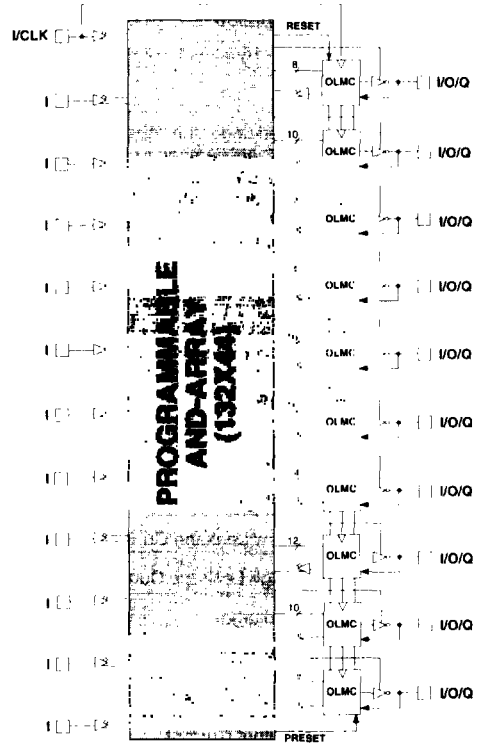
DESCRIPTION

The GAL22V10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

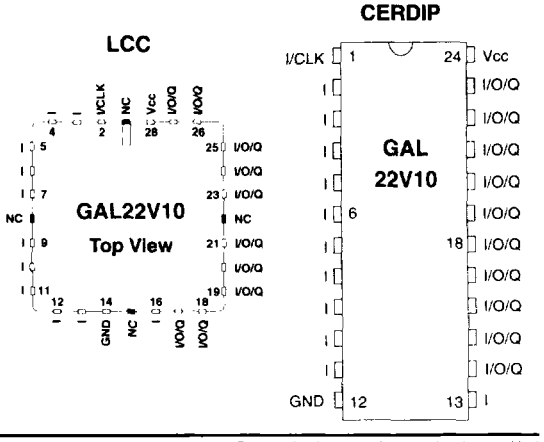
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss - 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}'	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	-2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-10 MIN.	-10 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	—	10	ns
tco	A	Clock to Output Delay	—	7	ns
tcf[2]	—	Clock to Feedback Delay	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	6	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	76.9	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	MHz
twh	—	Clock Pulse Duration, High	3	—	ns
twl	—	Clock Pulse Duration, Low	3	—	ns
ten	B	Input or I/O to Output Enabled	—	10	ns
tdis	C	Input or I/O to Output Disabled	—	12	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	12	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	6	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	10	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

CAPACITANCE (T_A = 25 °C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}'	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open — L -15/-20/-25/-30	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	15	—	20	—	25	—	30	ns
t_{co}	A	Clock to Output Delay	—	8	—	15	—	20	—	20	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	8	—	15	—	20	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	12	—	17	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	33	—	33	—	25	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	15	—	15	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	15	—	15	—	20	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	—	25	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	—	25	—	25	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	20	—	25	—	30	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	20	—	25	—	30	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	20	—	25	—	30	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	17	—	20	—	25	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

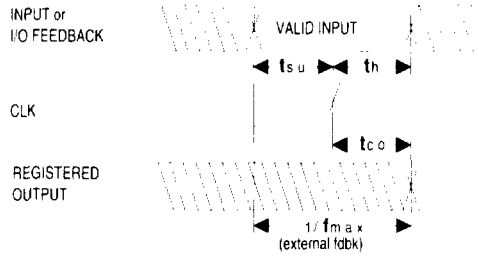
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

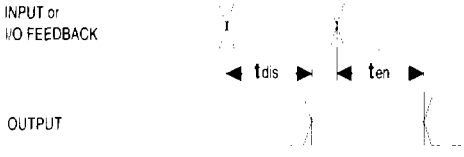
*Guaranteed but not 100% tested.

SWITCHING WAVEFORMS

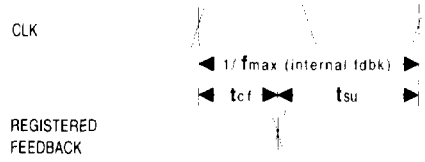
Combinatorial Output



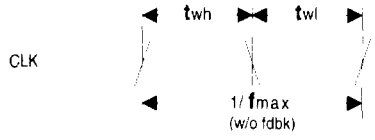
Registered Output



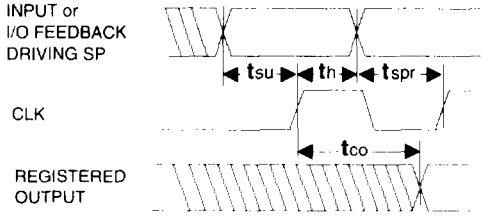
Input or I/O to Output Enable/Disable



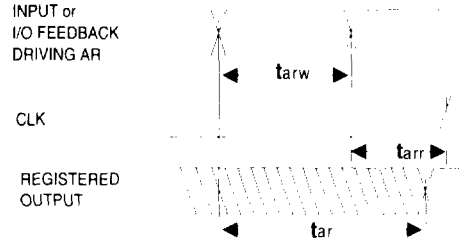
fmax with Feedback



Clock Width

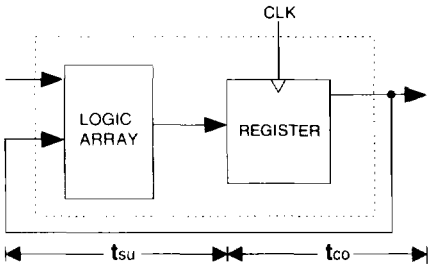


Synchronous Preset



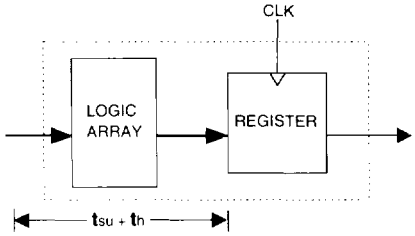
Asynchronous Reset

fmax DESCRIPTIONS



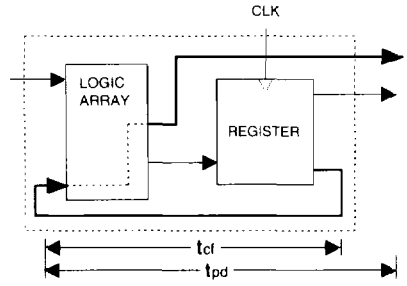
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

5

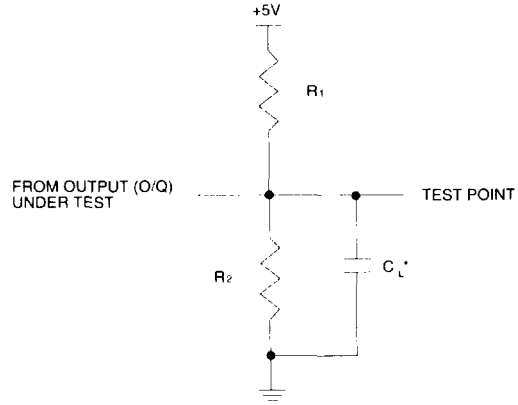
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



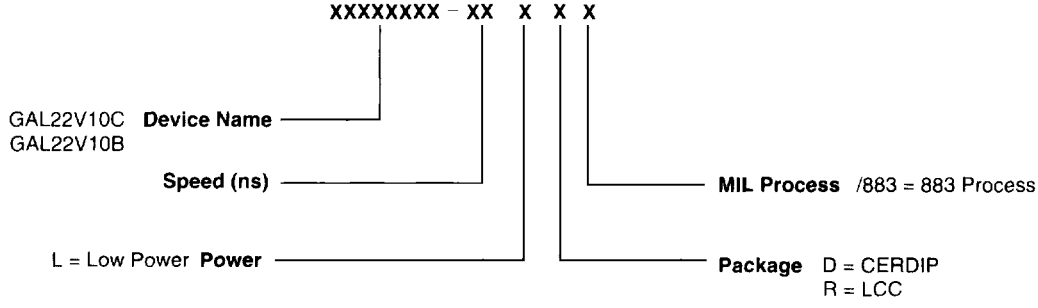
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10 ORDERING INFORMATION (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
10	6	7	150	24-Pin CERDIP	GAL22V10C-10LD/883	5962-8984106LA
			150	28-Pin LCC	GAL22V10C-10LR/883	5962-89841063A
15	12	8	150	24-Pin CERDIP	GAL22V10B-15LD/883	5962-8984103LA
			150	28-Pin LCC	GAL22V10B-15LR/883	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10B-20LD/883	5962-8984102LA
			150	28-Pin LCC	GAL22V10B-20LR/883	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10B-25LD/883	5962-8984104LA
30	25	20	150	24-Pin CERDIP	GAL22V10B-30LD/883	5962-8984101LA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

PART NUMBER DESCRIPTION



Section 6

Lattice Semiconductor Design Tool Strategy

Introduction

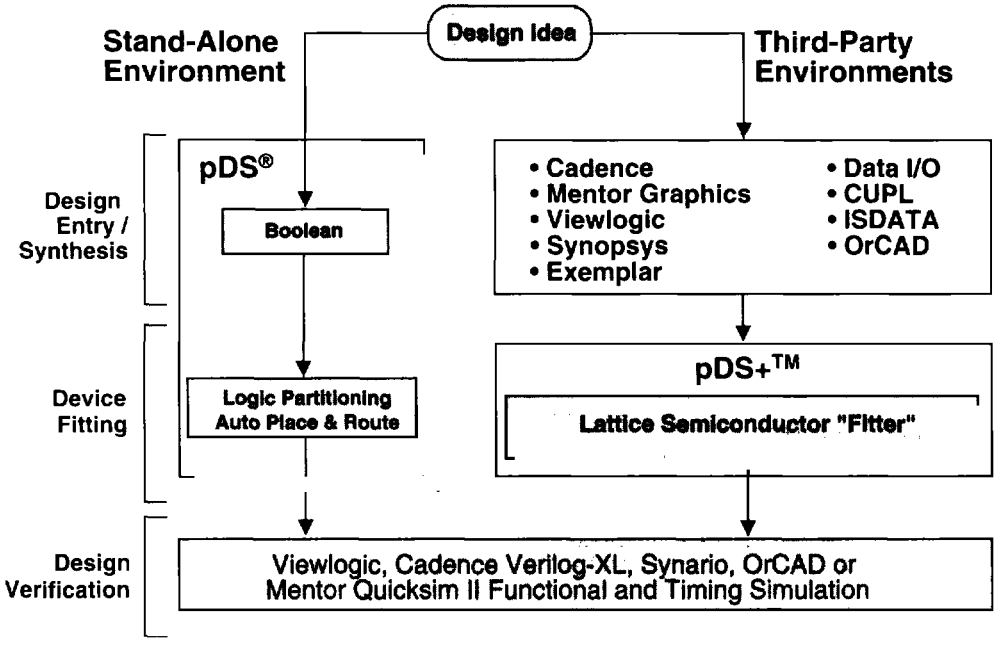
The Lattice Semiconductor Corporation (LSC) design tool strategy for the ispLSI and pLSI families is to support a wide range of design environments. LSC provides both a proprietary PC-based solution (pDS®) as well as third-party compatible CAE tools (pDS+™ Fitters) that run on PC, Sun and Hewlett Packard (HP) workstation platforms.

The LSC pDS pLSI/ispLSI software provides a comprehensive, high-performance, low-cost package for logic development. Developed and supported by LSC, pDS provides an easy-to-use Windows-based graphical interface using a mouse and pull-down menus. Design entry includes Boolean equations, standard and TTL macros. For simulation, timing tables are included as a standard offering. Additionally, pDS interfaces with Viewlogic's Viewsim, OrCAD's VST, and Data I/O's Synario simulation package for full functional and timing simulation. pDS software generates industry standard JEDEC programming files and supports direct download into ispLSI devices.

LSC's pDS+ (pDS Plus) solution supports multiple third-party CAE tools, providing designers with the capability to design in familiar CAE environments. These third-party CAE tools offer schematic capture, hardware description language (such as VHDL), state machine language, Boolean equation, and macro design entry as well as functional and timing simulators for design verification.

LSC's pDS and pDS+ solutions give designers powerful, easy to use, cost-effective design tools to meet their development needs. Each third-party vendor must adhere to strict quality and certification requirements before becoming qualified, thus ensuring superior support.

Figure 1. pDS and pDS+ Design Flows



Lattice Semiconductor Design Tool Strategy

Design Flow

There are three steps in the LSC ispLSI and pLSI design flow: design entry, device fitting (logic partitioning, place and route), and design verification. (See the pDS and pDS+ Design Flow). This section outlines the design flow of the pDS and pDS+ solutions.

pDS

LSC's pDS solution is a comprehensive, self-contained design solution which operates on a PC under Microsoft Windows™. pDS uses familiar ABEL-like Boolean equations, standard macros and a library of TTL macros for design entry, and provides manual partitioning, high speed automatic place and route, and simulation timing tables for design verification. A variety of simulators, such as Viewlogic's Viewsim simulation package, are compatible with pDS for functional and timing simulation.

After the development work has been completed, the design is ready to be programmed into a device. For third-party programming support, the pDS package generates a JEDEC fusemap . Alternatively, the ispLSI devices can be programmed directly from the PC or Sun workstation with the LSC isp Engineering Kit.

The pDS development systems are ideal for designers who desire a cost-effective, user friendly approach to ispLSI and pLSI design.

pDS+

The pDS+ solution combines third-party CAE tools for design entry and verification with the LSC pDS+ Fitter for device fitting to offer a powerful and complete development solution. LSC pDS+ Fitters support a broad range of third party design tools, including:

Vendor	Design Tool
Cadence	Concept, Synergy, Verilog-XL, Leapfrog
Data I/O	ABEL, Synario
Exemplar Logic	Galileo Logic Explorer
ISDATA	LOG/iC Classic, LOG/iC 2
Mentor Graphics	Design Architect, Autologic & Autologic II, Quicksim II, QuickVHDL, System V (Model Tech)
Logical Devices	CUPL
OrCAD	SDT, PLD, VST 386+, Capture for Windows, Simulate for Windows
Synopsys	Design Compiler Expert & Professional, FPGA Compiler, VSS
Viewlogic	PRO Series, Workview Plus, Powerview, Workview Office

The design entry step is typically performed with schematic capture, Boolean equations, state machines, truth tables or a Hardware Description Language (HDL). Once design entry is complete, the design is ready to be implemented into a LSC ispLSI or pLSI device.

The LSC pDS+ Fitter uses architecture-specific algorithms to synthesize a logic description into an ispLSI or pLSI device. Steps in the device fitting process include logic optimization and minimization, automatic logic partitioning, and automatic place and route.

pDS+ also supports design verification. Design verification options include both functional and timing simulation. Various combinations of graphical and text-based functional and timing simulators are supported by third-party CAE vendors.

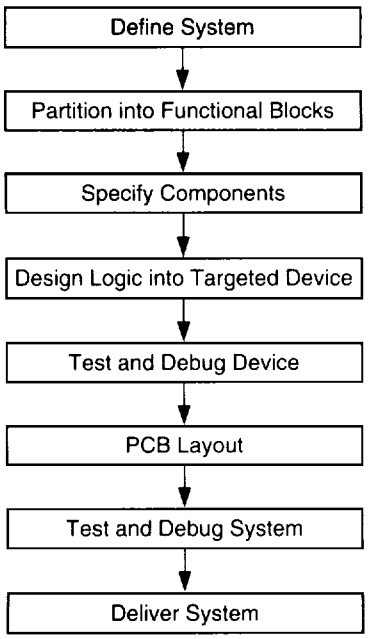
Following design verification, the LSC pDS+ Fitter generates a JEDEC fusemap for device programming. The design can be programmed into a pLSI device using third-party programmers. In addition, the ispLSI devices can be programmed directly from a PC using LSC's isp Engineering Kit, or from dedicated logic designed into the end-system.

System Design Process

Introduction

Conceptually, system definition is the first step in the design process. This involves visualizing the PLD's interaction with the rest of the electronic system and defining a general flow diagram to determine the design's basic sequential behavior. This organizational flow, used to integrate an entire subsystem into high density devices, is described in the following topics and shown in figure 1.

Figure 1. System Design Flow



Partitioning

After completing the conceptual design, the designer partitions the system into modules or functional blocks. These blocks can be a few components or multiple circuit boards with numerous components. The designer organizes these functional blocks to match the capabilities of the devices being targeted, for example, the number of I/O pins, flip-flops and gates needed. The user should also consider the frequency at which the targeted device must operate, the number of clocks required, and the timing relationships of signals (AC specifications).

Specifying Components

After the partitioning is defined, the designer chooses the components which will be used to implement the desired functions. The design should meet the system specifications using the least number of components in order to keep the system cost as low as possible while keeping the system reliability as high as possible.

System specifications calling for low weight, low power and reduced size also drive designers to higher levels of logic integration. These added requirements can adversely affect the design schedule and project completion. The ispLSI and pLSI high-density devices can meet such design requirements while delivering excellent performance. The ispLSI and pLSI family of high-speed, high-density PLDs supported by easy-to-use effective software for fast design implementation and verification.

Design Entry and Optimization

After the functional partitioning and component specifications are completed, the logic necessary to implement the functions is defined block by block. The logic may include standard TTL functions, CMOS logic functions, or functions from a library, such as the Lattice Semiconductor Corporation (LSC) Macro or TTL library. The implementation of logic into a high density device is optimized for the targeted device by the design software. The partitioning also affects the optimization. Optimization can be for speed, utilization or a combination of both.

Logic entry for an LSC high-density device is done with the pLSI/ispLSI Development System (pDS) or with any of the third-party CAE tools supported by LSC's pDS+ Fitters. The pDS software utilizes the Graphical User Interface (GUI) of Microsoft's Windows™ to provide a complete design flow from logic entry to programming ispLSI/pLSI devices within hours. pDS+ Fitters, in conjunction with third-party CAE tools, support textual design entry using a Hardware Description Language (HDL); standard CAE schematic design entry; and/or Boolean, truth table or state machine entry.

Test and Debug

When designing a system, or a portion of a system, it is easier to test and debug pieces or modules rather than the entire system. In this manner, the designer can

confirm module designs, or functional blocks, and find problems earlier in the design cycle.

Logic can be verified by either timing simulation or actual testing of the programmed device. Simulation can be accomplished using a variety of logic simulators. Design errors detected by software simulation can be corrected by the designer before the printed circuit board is laid out and manufactured, which saves time and reduces cost. Board and system level simulation can be accomplished through behavioral simulation using Synopsys Logic Modeling Division models.

Reprogrammable devices allow the designer to test, debug, and modify logic right on the p.c. board. ispLSI and pLSI devices can be reprogrammed multiple times. This reprogrammability further assists the designers by allowing them to temporarily program the devices with diagnostic and design verification logic.

The designer should always attempt to design logic with testability in mind. Testability means different things to different designers. Key guidelines to be aware of are:

- Large counters should be segmented for quick and easy testing.
- Logic should be designed for controllability and observability.
- There should be no floating nets.
- All nets should be at a known state or are able to be set or reset.

To assist system testability, the ispLSI devices offer preload and verification features. These features allow register contents to be verified without using logic analyzers or other debugging tools.

Printed Circuit Board Layout

Once the logic has been verified, the Printed Circuit Board (PCB) is laid out and manufactured. Since the logic may be changed during design, this phase of the system design is usually executed after the logic has been validated. It is recommended that board design and layout be done after verifying designs using ispLSI and pLSI parts.

System Test and Debug

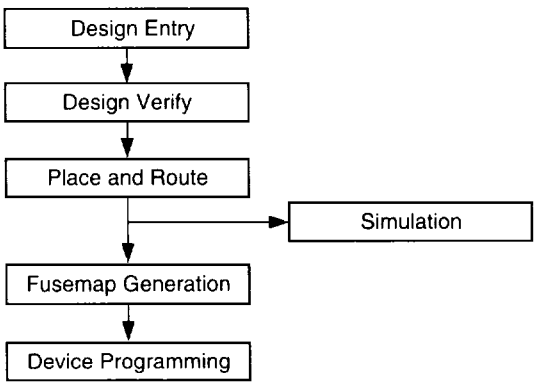
System test and debug is the final stage of the design process. The logic and the PCB are tested as a system and minor enhancements or bug fixes are implemented. Because of the flexibility of the ispLSI and pLSI devices, minor changes can be made without greatly affecting the layout of the PCB or the pinout of the device.

ispLSI and pLSI Design Flow

Introduction

Once the system design has been organized into functional components, and the logic functions which need to be incorporated in the selected components defined, the logic design phase begins. The general design flow is shown in figure 1. An ispLSI or pLSI design may be implemented from a number of design environments: including pLSI/ispLSI Development System (pDS) and numerous third-party CAE tools.

Figure 1. General Design Flow



These design environments offer various levels of design implementation from logic entry through programming the device. They support a variety of user interfaces and entry methods including: MS Windows GUI, Verilog-HDL, VHDL, truth tables, state machines and Boolean equations.

Design Entry

The pDS software allows the user to manually partition the logic to control design fit and performance. Using the MS Windows environment, logic functions are placed into Generic Logic Blocks (GLBs) and I/O Cells. This can be done by using the Edit, Cut, Copy, and Paste functions to enter Boolean equations and/or pre-defined functions from the LSC Macro and TTL libraries.

In addition to Boolean design entry, the pDS+ Fitters (in conjunction with third-party CAE tools) allow high-level descriptions of counters, adders, comparators, etc. High-level languages also support state machines, truth tables and case constructs for behavioral design implementations.

For standard CAE schematic designs, the pDS+ Fitters/ third-party CAE tools provide support for graphical and hierarchical logic implementations using the Lattice Semiconductor Corporation (LSC) libraries of primitives and macros. The integrated user interfaces also allow easy integration of system or user-created functions into a hierarchical schematic using a top-down or bottom-up design methodology.

Design Verification

Verification using the pDS software is accomplished in two steps after logic has been placed. First, each cell may be individually verified to ensure that the minimized logic will fit into the GLB architecture. After all GLB and I/O cells are incrementally checked, the entire design is then verified to ensure that all nets have proper sources and destinations.

Because the advanced pDS+ tools perform automatic partitioning, design verification is done at a higher-level (pre-partitioned). For example, in the ABEL environment, the Compile (ahdl2pla) function performs the syntax and design rule checks. After the Compile phase, the Optimize (plaopt) function (optionally) minimizes the design.

In the pDS+Viewlogic environment, pre-partitioned design verification is performed by the Design Analyzer which ensures the logic conforms to the LSC design rules. Other CAE tools may perform these functions differently, but each has been tested for completeness and accuracy.

Partitioning

Partitioning using the pDS software is done by the user as part of the design entry process. The advanced pDS+ tools incorporate LSC's automatic partitioner which accepts converted data from designs entered using the third-party CAE tool of choice. LSC specific attributes for design entry are available to guide the partitioner in order to optimize usage of device features and performance.

Place and Route

All LSC design tools offer automatic place and route. This entails placement of GLB and IOC logic and then routing (or interconnecting) the source signals to their destinations. In the ispLSI and pLSI devices, the Global

Routing Pool (GRP) provides fast interconnects from external inputs and GLB feedbacks to the GLB inputs. The Output Routing Pool (ORP) provides flexible interconnects from GLB outputs to external pins.

Post-Route Simulation

After place and route, a netlist for full timing and function simulation may be passed to the third-party simulator. Many of these simulators offer both textual and graphical input and interfaces. Board and system level simulation models are available from Synopsys Logic Modeling Division.

Documentation

Report files, containing partitioned equations and pin-out information, may be generated for routed or un-routed designs. The pDS software can also generate reports with post-route maximum timing delays. In addition, the design can be exported in a variety of design formats. This supports design interfaces to standard third-party CAE tools.

Device Programming

Programming information is generated on a routed design by the FuseMap Generator for a specific ispLSI and pLSI device. It is an ASCII file written in the JEDEC format.

Two programming methods are used to program the ispLSI and pLSI devices. The first method uses the Device Programming Mode for both types of devices. This method facilitates device programming support from third-party vendors. The second method uses the LSC In-System Programming Mode and applies to the ispLSI family of devices.

Both methods of device programming allow the user to program and read back the fuesmap from the programmed device for verification (if the security cell has not been set).

Figure 2. pDS Design Flow

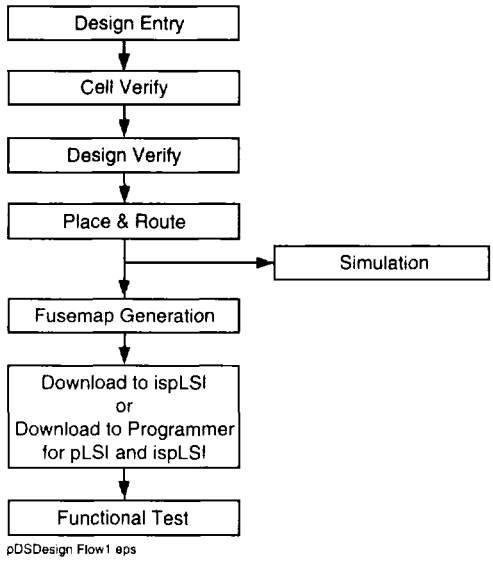
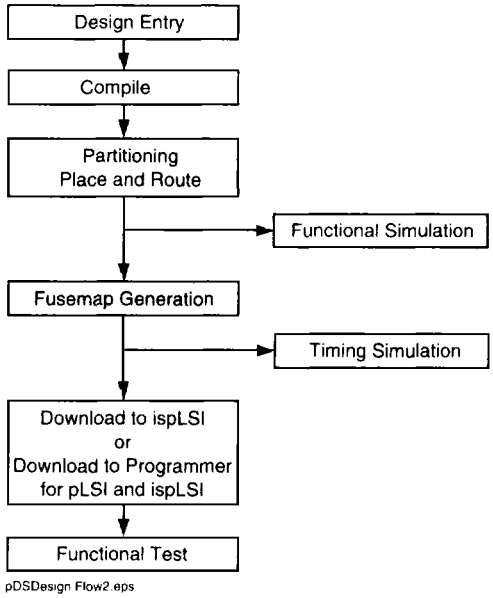


Figure 2a. Typical pDS+ Design Flow



Lattice Semiconductor Corporation

pDS® Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **Supports ispLSI and pLSI 1000/E and 2000**
  - **Upgrade to Support ispLSI and pLSI 3000 and 6000**
- **DESIGN ENTRY WITH EASY-TO-USE WINDOWS™ ENVIRONMENT**
  - **ABEL-Like Boolean Equation Entry**
  - **Logic Macro Entry with Over 275 "TTL-Like" Macros and Over 200 TTL Macros**
  - **Manual Device Partitioning Ensures Tight Control of Performance and Utilization**
- **FAST DESIGN COMPILATION**
  - **Multi-Level Logic Synthesis**
  - **Efficient Design Optimization and Minimization**
  - **"Hands-Free" Automatic Place and Route**
  - **Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **Functional and Timing Simulation Options**
- **INDUSTRY STANDARD JEDEC PROGRAMMING FILE GENERATION**
  - **Standard JEDEC Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **ispCODE™ C Source Routines Included**
  - **ISP Daisy Chain Download**
  - **ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **PC Windows 3.1/Windows 95/ Windows NT**

Introduction

The pDS software is a comprehensive design package for the Lattice Semiconductor Corporation (LSC) ispLSI and pLSI device families giving full design entry and device implementation capabilities under the Windows design environment. The pDS software provides the best solution for high performance designs which require direct control of the logic implementation. It offers designers complete control over the performance and utilization of the device. The pDS software allows designers to quickly move from concept to a programmed logic device.

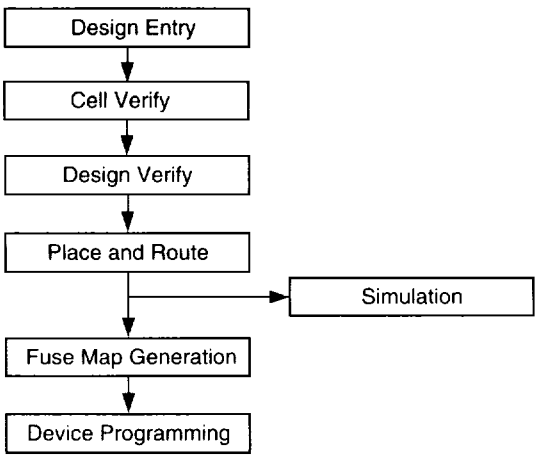
The pDS software also offers simulation options for full functional and timing simulation of designs using a variety of third-party simulators.

pDS Software

Using the pDS software, designs can be defined completely using simple Boolean equations and "TTL-like" or TTL logic macros. Automated design capabilities shorten design cycles allowing designers to explore several design solutions before deciding on the one that provides the best solution.

Designs can be entered in two ways: either through the integrated edit windows within the pDS software, or by using a standard ASCII text editor to create a design file that can be imported into the pDS environment. The Place and Route software automatically places the logic and routes the interconnections. The fuse map program generates a fuse file which can then be downloaded into a device programmer or directly to an ispLSI device (see figure 1).

Figure 1. pDS Design Flow



Design Entry

pDS software offers an easy to use interface as shown in figure 2. Designers can quickly enter the design into GLBs and I/O cells through this interface. An example of an edit window is shown in figure 3. Tables 1, 2 and 3 provide a condensed list of the different operations which are supported in the pDS software.

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Figure 2. pDS Software User Interface

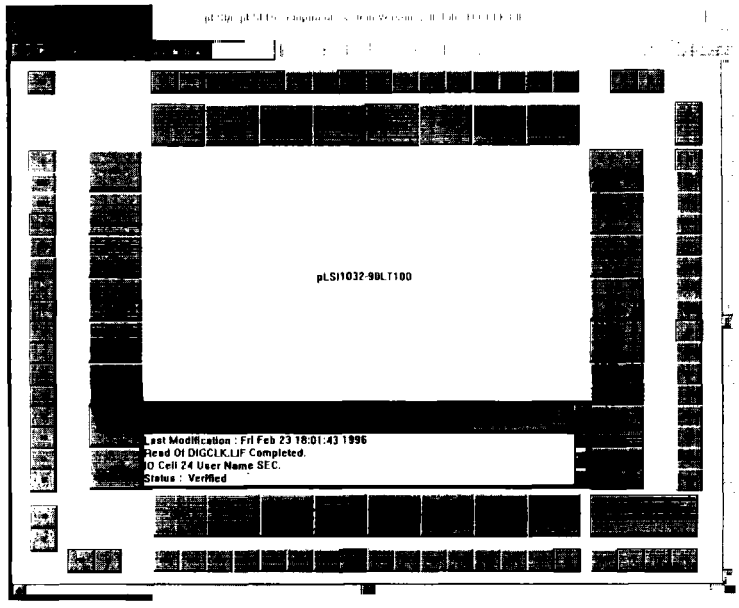

Figure 3. Sample Edit Window Illustrating Boolean Equations and Macros

```
SIGTYPE CO_P OUT;
SIGTYPE C1   REG OUT;
XOR4 (par, D1, D2, D3, D4)
EQUATIONS
     CO_P = CO_0 & CO_1 # CO_2;
     C1   = C1$$  C0;
     C1.CLK = SYSCLK;
END;
```

The following tables show some of the pDS software keywords, operators and dot extensions used.

Table 1. Keywords

Keyword	Description
CONSTANT	Assigns a value to a signal
SET	Assigns a label to a group of signals
SIGTYPE	Assigns specific attributes to a GLB output
CRIT	Used for the 4 product term bypass
XPIN	Identifies external signal in the I/O cell
LOCK	Locks an I/O cell to a pin
EQUATIONS	Beginning of the Boolean description of the logic in a GLB
//	The text that follows is a comment

Table 2. Operators

Operator	Description
=	Assignment
!	Inversion
$$	Hardware exclusive OR
&	AND
#	OR
$	Exclusive OR
!$	Exclusive NOR

Table 3. Dot Extensions

Extension	Description
.D	Identifies the signal as the D input
.Q	Identifies the signal as the Q output
.RE	Identifies the product term reset signal for the GLB
.CLK	Identifies the system clock for the GLB
.PTCLK	Identifies the product term clock for the GLB
.OE	Identifies the output enable signal for the I/O cells within the megablock

The pDS software offers an extensive selection (over 275) of TTL-like macros. These macros enable the design engineer to use familiar pre-defined functions to build a design. Table 4 shows a summary of the TTL macros also available in the pDS software.

Logic Optimization

The pDS software provides extensive design rule checking during the optimization and fitting process. After the design has been checked, the software initiates logic minimization to reduce the number of product terms needed. There are two minimization options:

— Fast Min
— Strong Min

The Fast Min option performs quick minimization to reach the debugging stage sooner. The Strong Min option performs a comprehensive logic minimization to maximize device resource utilization and ensures efficient design implementation. With the Strong Min option, small design changes can generally be performed without expensive PC board rework.

Automatic Place and Route

The pDS software provides an automatic place and route routine which eliminates the need for manual routing and provides a quicker design cycle time. The router automatically generates pinouts based on an optimal design implementation or it can use a user defined pinout.

Incremental place-and-route capability allows last-minute logic updates to be implemented without design pin-out changes.

Post Route Simulation

Complete post route design verification can be peformed using optional third party timing simulators.

Fuse Map Generation

The Lattice Semiconductor fuse map generation module outputs the file containing the fuse pattern used to implement the logic in the device. A security feature offers protection of proprietary designs from unauthorized duplication.

Table 4. Macro Summary

Function Type	Number of Macros	Number of TTL Functions
AND/NAND	20	11
OR/NOR	16	8
XOR/XNOR	4	2
Decoder/Encoder	17	16
AND/OR	8	7
Flip/Flop	28	19
Latch	10	6
Arithmetic	17	16
Counter	22	20
Shift Register	14	14
MUX/DEMUX	15	12
Miscellaneous	14	13

System Requirements

- 486/Pentium IBM Compatible PC
- MS DOS Version 3.3 or Later
- MS Windows Version 3.1 or Later
- MS Windows 95
- MS Windows NT
- 8 MB RAM and 10 MB Hard Disk Space
- Parallel Printer Port for Software Key
- VGA or Higher Resolution Display
- Mouse (Windows Compatible)

Product Ordering Information

Product Code	Description
pDS1101-PC1	pLSI/ispLSI Development System (pDS)
pDS1101-3UP/PC1	pLSI and ispLSI Development System (pDS) 3000 and 6000 Family Upgrade
pDS3302-PC2	Viewlogic Viewsim Timing & Functional Simulator
pDS1102-PC2	Viewlogic Viewsim Simulation Libraries and Interface Files
pDS1170-PC1	OrCAD VS386+ Simulation Libraries and Interface

Annual Maintenance*

pDS1101M-PC1	Maintenance for pDS1101-PC1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS3302M-PC2	Maintenance for pDS3302-PC2

*One year of maintenance is provided with every product purchase

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI deices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Table 5. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

Lattice™ Semiconductor Corporation

pDS+™ABEL Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **Supports ispLSI and pLSI 1000/E and 2000**
  - **Upgrade to Support ispLSI and pLSI 3000**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **ABEL Hardware Description Language (ABEL-HDL) or ABEL VHDL Syntax Support Boolean Equations, Truth Tables and State Machine Entry**
  - **Graphical, Menu-Driven User Interface**
- **SUPPORTS VIEWLOGIC VIEWPLD™**
- **pDS+ ABEL FITTER**
  - **Multi-Level Logic Synthesis**
  - **Efficient Design Optimization and Minimization**
  - **Automatic Mapping and Device Fitting**
  - **Automatic Partitioning with High Utilization**
  - **Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **Standard JEDEC Device Fuse Map**
- **PLATFORMS SUPPORTED**
  - **Windows 3.1/Windows 95/Windows NT**
  - **Sun SPARC 4™ and Above**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **ispCODE™ C Source Routines Included**
  - **ISP Daisy Chain Download (PC Versions)**
  - **ispATE™ Board Test Programming Utility**

Introduction

The pDS+ ABEL software from Lattice Semiconductor offers a powerful solution to fit high-density logic designs into Lattice's ispLSI and pLSI devices.

Design entry is made simple by using ABEL software from Data I/O together with the pDS+ ABEL Fitter for design implementation. The ABEL software and pDS+ ABEL Fitter offer high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Data I/O ABEL

The easy-to-use, menu-driven ABEL software packages provide a complete pre-fit design environment. Using ABEL-HDL from DATA I/O Corporation or ABEL VHDL, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other HDL descriptions. The HDL syntax allows design creation without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation as easy as clicking a mouse button.

pDS+ ABEL Fitter

The pDS+ ABEL Fitter for ispLSI and pLSI devices is completely integrated within the ABEL Software environment. The pDS+ ABEL Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation with optional test vectors, in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization & Logic Minimization

The pDS+ ABEL Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions whenever possible. In addition, the pDS+ ABEL Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ ABEL Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

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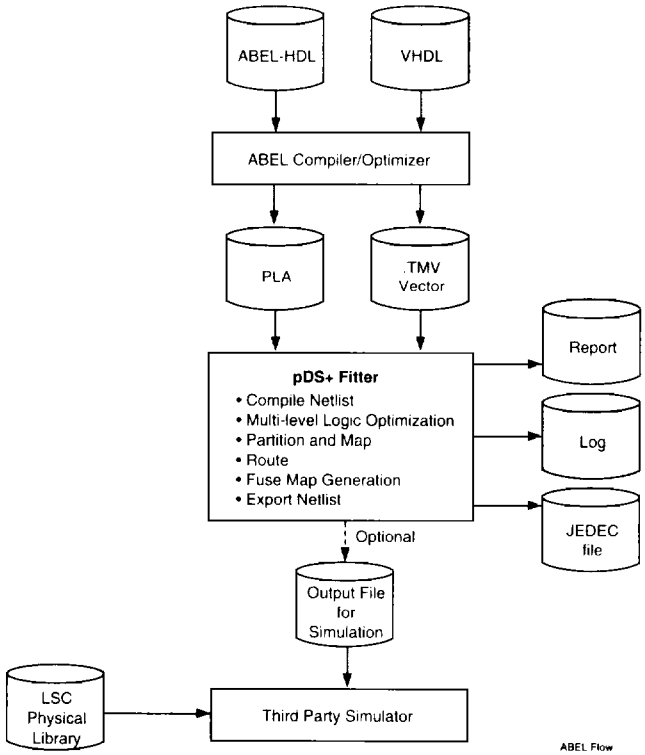
Figure 1. pDS+ ABEL Fully Integrated Design Environment



Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Router optimally interconnects signals between I/O cells and GLBs through the Global Routing Pool (GRP) and Output Routing Pool (ORP). It also performs GLB splitting and GLB output duplication to enhance routing.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ ABEL Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the ABEL design file. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Controls

Special properties can be passed to the pDS+ ABEL Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ ABEL Fitter provides a parameter file feature which helps designers eliminate guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ ABEL Fitter also provides post-route equations showing exactly how the design is implemented in the selected device.

Fuse Map Generation

The pDS+ ABEL Fitter supports a device fusemap in standard JEDEC format. A security feature gives protection of proprietary designs from unauthorized duplication. The fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Verification

The pDS+ ABEL software supports functional simulation of all ispLSI and pLSI designs using the built-in ABEL functional simulator. The simulation test vectors can be combined into the JEDEC file for device testing in a programmer.

Complete post route design verification can also be performed using optional Viewlogic Viewsim, PROsim, or other third party timing simulators. The pDS+ ABEL software generates the output file required for third-party simulation. Simulation libraries are available from Lattice Semiconductor for various PC and Sun-based CAE vendor tools. The Viewlogic PROsim simulator and Synario simulator are available from Lattice Semiconductor for the PC platform.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- ABEL 4.1 or Later
- Parallel Printer Port for Software Key

System Requirements (Sun Platform)

- Sun Sparc 4 and above
- Sun OS Version 4.x
- Open Windows 3.0
- ABEL 4.1 or Later
- 16 MB RAM with 30 MB Hard Disk Space
- 3 Button Mouse

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88

Programmer Vendor	Model
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High-pin count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2102-PC1	Fitter for DATA I/O ABEL on PC Platform
pDS2102-3UP/PC1	3000 Family Upgrade for pDS2102-3UP/PC1
pDS2102-SN1	Fitter for DATA I/O ABEL on Sun Platform
pDS2102-3UP/SN1	3000 Family Upgrade for pDS2102-3UP/SN1
pDS1102-PC2	Viewlogic Library and Interface for PC
pDS1102-SN1	Viewlogic Library and Interface for Sun
pDS3302-PC2	PROSim Simulator with Libraries
pDS1120-PC1	Synario Libraries and Interface
pDS1170-PC1	OrCAD Simulator Library and Interface
pDS1160-SN1	Cadence Verilog-XL Library and Interface
pDS1150-SN1	Mentor Graphics Quicksim II Library and Interface
Maintenance*	
pDS2102M-PC1	Maintenance for pDS2102-PC1
pDS2102M-SN1	Maintenance for pDS2102-SN1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS3302M-PC2	Maintenance for pDS3302-PC2
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS1150M-SN1	Maintenance for pDS1150-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

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