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= Preliminary =

AK7742

24bit 2ch ADC + 24bit 4ch DAC with Audio DSP

GENERAL DESCRIPTION

The AK7742 is a highly integrated audio digital processor, including two stereo 24bit DAC's and one stereo ADC with input selector. The stereo DAC and ADC feature high performance, archiving 106dB and 96dB dynamic range respectively, 8kHz to 96kHz sampling rate are supported. The audio DSP has 1536step/fs parallel processing power, and 74k-bit delay memory allows surround processing, acoustic effect and parametric equalizers. As the AK7742 is a RAM based DSP, it is programmable for user requirements. The AK7742 is available in a space saving small 48pin LQFP package.

FEATURES

■ **DSP:**
- **Word length: 24bit (Data RAM 24bit floating point)**
- **Instruction cycle: 13.6 ns (1536step/fs fs=48kHz; 9216step/fs fs=8kHz)**
- **Multiplier 20 x 16 → 36bit (double precision available)**
- **Divider 20 / 20 → 20bit**
- **ALU: 40bit arithmetic operation (overflow margin 4bit) 24bit floating point arithmetic and logic operation**
- **Program RAM: 1536 x 36bit**
- **Coefficient RAM: 1536 x 16bit**
- **Data RAM: 1536 x 24-bit (24bit floating point)**
- **Delay RAM: 74kbit (3072 x 24bit)**
- **Sampling frequency: 8kHz ~ 96kHz**
- **Master / Slave operation**
- **Serial signal input port (4ch) MSB justified 24bit / LSB justified 24 / 20 / 16bit and I^2S**
- **Serial signal output port (6ch) MSB justified 24bit / LSB justified 24 / 16bit and I^2S**

■ **ADC: 2ch (stereo)**
- **24bit 64 x Over-sampling delta sigma (fs=8kHz~48kHz)**
- **DR, S/N: 96dB (fs=48kHz, fully differential input)**
- **S/(N+D): 84dB (fs=48kHz)**
- **Differential, Single-end Inputs**
- **Digital HPF (fc=1Hz)**
- **3:1 Analog input selector**
- **Digital Volume (24dB~-103dB, 0.5dB Step, Mute)**

■ **DAC: 4ch (two stereo pairs)**
- **24bit 128 x Over-sampling advanced multi-bit (fs=8kHz~96kHz)**
- **DR, S/N: 106dB**
- **S/(N+D): 92dB**
- **Differential output**
- **Digital Volume (24dB~-103dB, 0.5dB Step, Mute)**

■ **DSP Through Mode**

■ **I^2C BUS interface for micro-controller**

■ **Power supply: +3.3V ±0.3V, internal regulator for 1.8V**

■ **Operating temperature range: -20°C~70°C**

■ **Package: 48pin LQFP (0.5mm pitch)**

■ Block Diagram

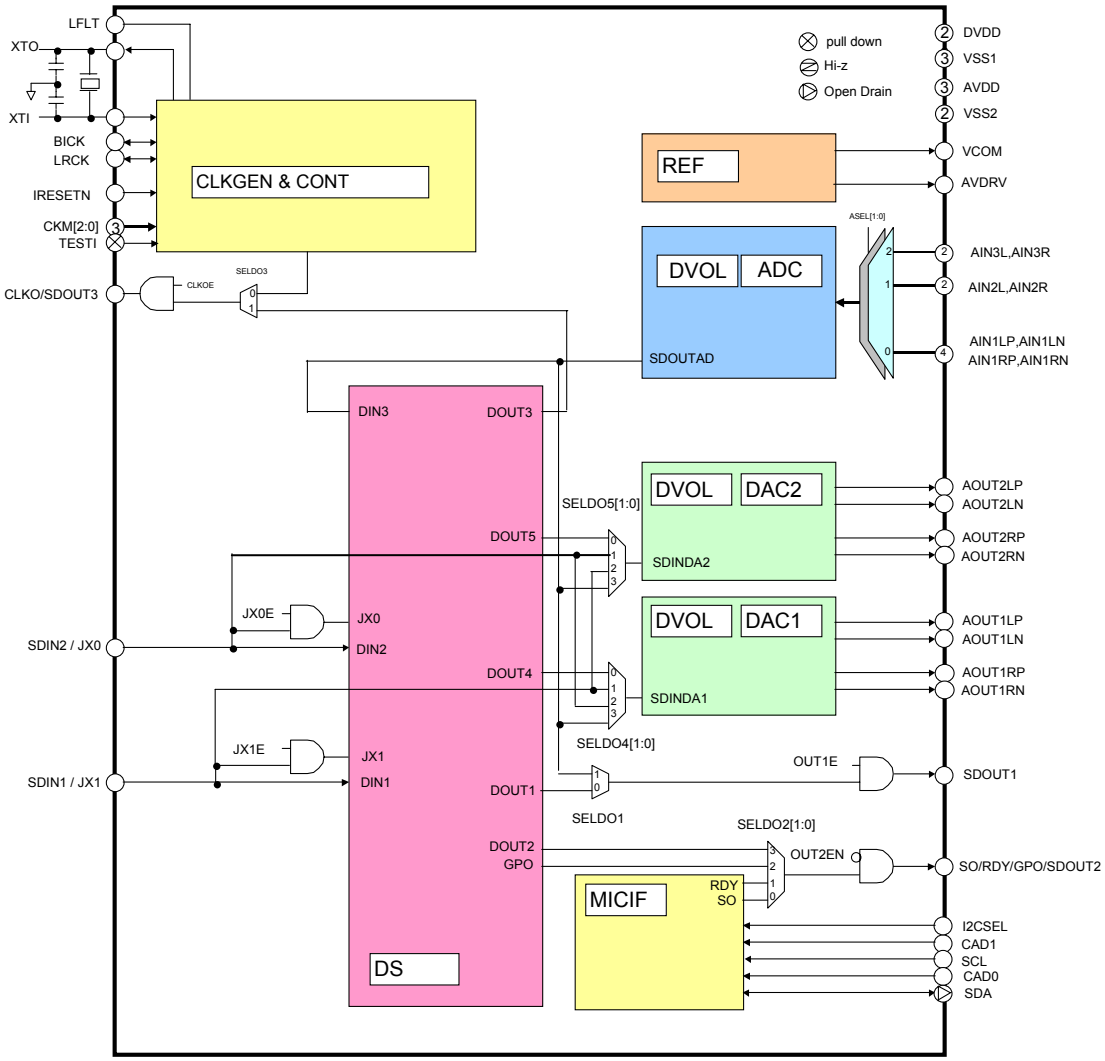


Figure 1. Block Diagram

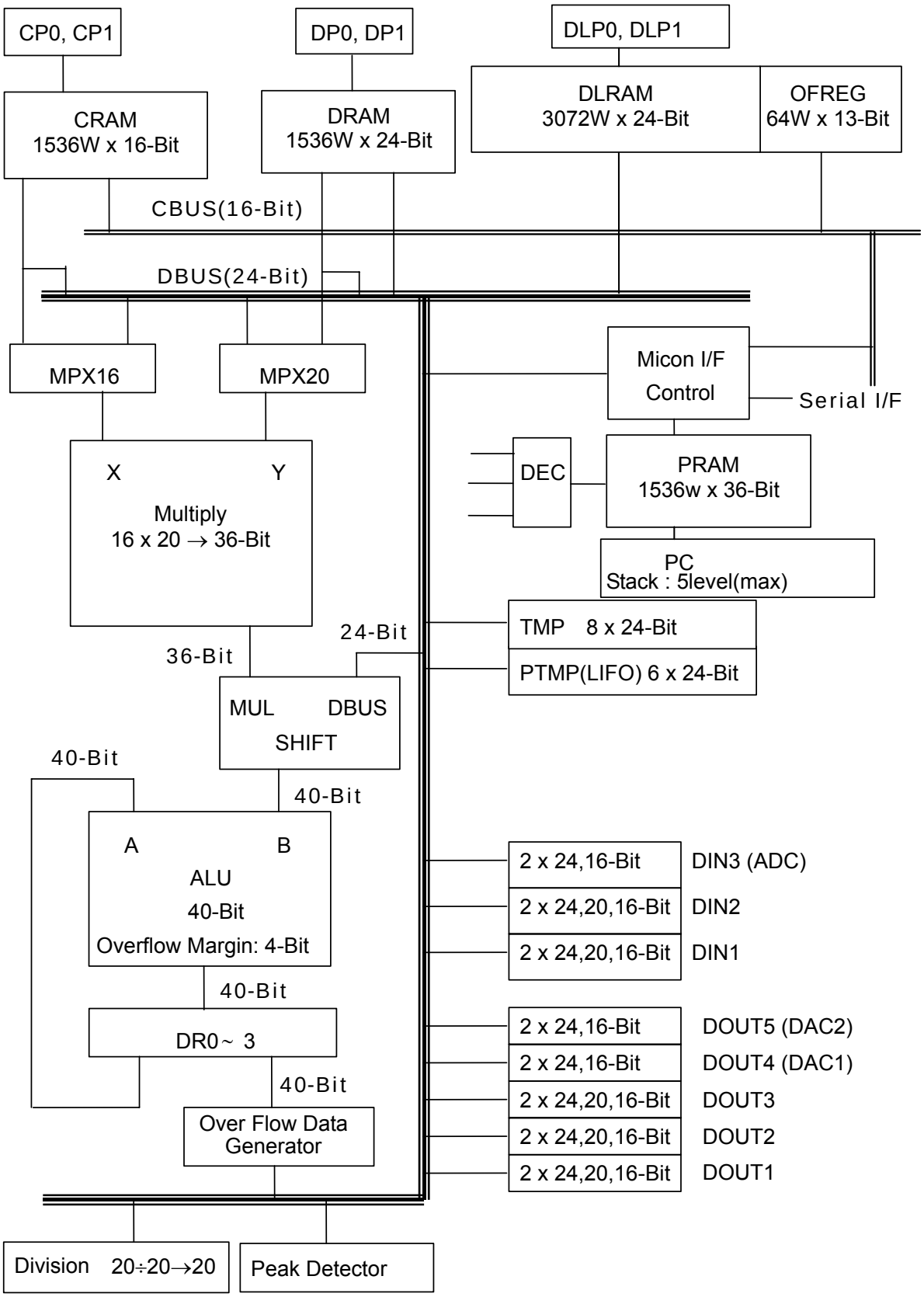
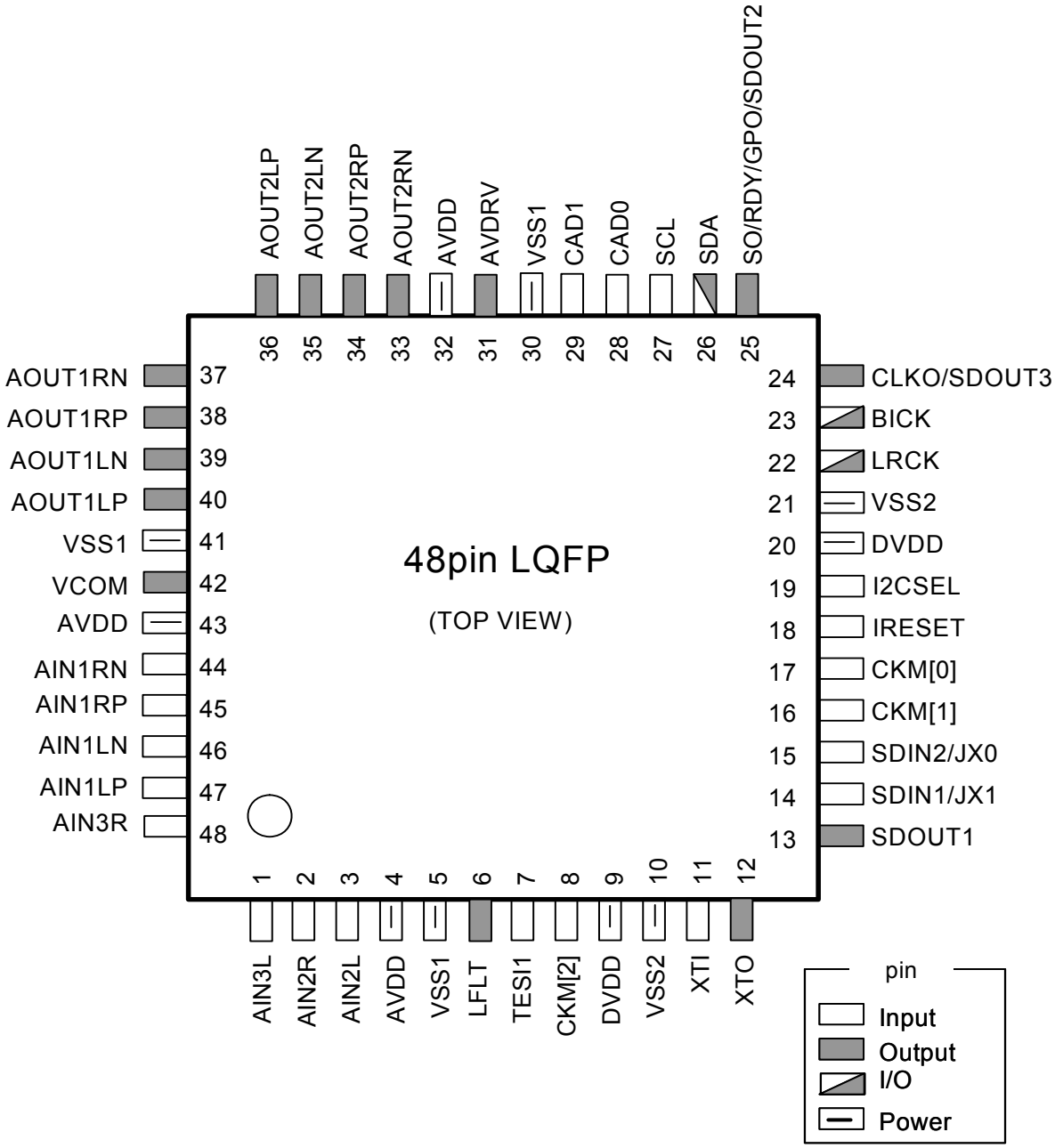


Figure 2. AK7742 DSP Block

■ Ordering Guide

AK7742EQ	-20 ~ +70°C	48pin LQFP (0.5mm pitch)
AKD7742	Evaluation board for the AK7742	

■ Pin Layout



PIN FUNCTION

No.	Pin name	I/O	Function	Classification
1	AIN3L	I	ADC Lch Single-end input 3 pin	Analog input
2	AIN2R	I	ADC Rch Single-end input 2 pin	Analog input
3	AIN2L	I	ADC Lch Single-end input 2 pin	Analog input
4	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
5	VSS1		Analog ground 0V	Analog power supply
6	LFLT	O	Filter connection pin for PLL Connect C=12nF to VSS1. "L" output during initial reset.	Analog output
7	TESTI	I	Test pin (internal pull-down resistor) Connect to VSS2	Test
8	CKM[2]	I	Clock mode select pin 2	Mode select
9	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
10	VSS2		Digital ground 0V	Digital power supply
11	XTI	I	Master clock input pin When using a crystal oscillator, connect it between this pin and XTO. When using external main clock, input to this pin with CMOS level.	Clock
12	XTO	O	Crystal oscillator output pin When using a crystal oscillator, connect it between this pin and XTI. When not using crystal oscillator, leave open. Output during initial reset is not determined.	Clock
13	SDOUT1	O	DSP serial data output pin "L" output during initial reset	Data interface
14	SDIN1/JX1	I	Serial data input pin 1 / JX1	Data interface
15	SDIN2/JX0	I	Serial data input pin 2 / JX0	Data interface
16	CKM[1]	I	Clock mode select pin 1	Mode select
17	CKM[0]	I	Clock mode select pin 0	Mode select
18	IRESETN	I	Reset pin (for initialization)	Reset
19	I2CSEL	I	I^2CBUS select pin Connect to DVDD	Microcomputer I/F
20	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
21	VSS2		Digital ground 0V	Digital power supply
22	LRCK	I/O	LR channel select clock pin "L" output during initial reset with master mode.	Data interface
23	BICK	I/O	Serial bit clock pin "L" output during initial reset with master mode.	Data interface
24	CLKO/SDOUT3	O	Clock output / DSP serial data output pin "L" output during initial reset	Clock
25	SO/RDY/GPO/ SDOUT2	O	Serial data output pin / Data write ready output pin / General purpose output / DSP serial data output pin "L" output during initial reset	Microcomputer I/F
26	SDA	I/O	SDA I^2C bus interface	Microcomputer I/F
27	SCL	I	SCL I^2C bus interface	Microcomputer I/F
28	CAD0	I	I^2C bus address pin 0	Microcomputer I/F
29	CAD1	I	I^2C bus address pin 1	Microcomputer I/F
30	VSS1		Analog ground 0V	Analog power supply

31	AVDRV	O	AVDRV Pin Connect 1μF to VSS1. Never to use for external circuit. “L” output during initial reset	Analog power supply
32	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
33	AOUT2RN	O	DAC2 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
34	AOUT2RP	O	DAC2 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
35	AOUT2LN	O	DAC2 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
36	AOUT2LP	O	DAC2 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
37	AOUT1RN	O	DAC1 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
38	AOUT1RP	O	DAC1 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
39	AOUT1LN	O	DAC1 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
40	AOUT1LP	O	DAC1 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
41	VSS1		Analog ground 0V	Analog power supply
42	VCOM	O	Analog common voltage Connect 0.1μF and 2.2μF in parallel to VSS1. Never to use for external circuit. “L” output during initial reset	Analog output
43	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
44	AIN1RN	I	ADC Rch differential inverted analog input pin	Analog input
45	AIN1RP	I	ADC Rch differential non-inverted analog input pin	Analog input
46	AIN1LN	I	ADC Lch differential inverted analog input pin	Analog input
47	AIN1LP	I	ADC Lch differential non-inverted analog input pin	Analog input
48	AIN3R	I	ADC Rch Single-end input 3 pin	Analog input

Note:

Digital input pins are never to be left open.

If analog input pins (AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R) are not used, leave them open.

ABSOLUTE MAXMUM RATING

(VSS1=VSS2=0V: Note 1)

Item	Symbol	min	max	Unit
Power supply voltage (AVDD= DVDD)				
Analog	AVDD	-0.3	4.3	V
Digital	DVDD	-0.3	4.3	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage (Note 2) AIN1LP, AINL1N, AIN1RP, AINR1N, AIN2L, AIN2R, AIN3L, AIN3R	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital input voltage (Note 3)	VIND	-0.3	(DVDD+0.3) or 4.3	V
Operating ambient temperature	Ta	-20	70	ºC
Storage temperature	Tstg	-65	150	ºC

Note 1. All indicated voltages are with respect to ground. VSS1 and VSS2 must be the same voltage.
Note 2. The maximum value of analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 3. The maximum value of digital input voltage is smaller value between (DVDD+ 0.3)V and 4.3V.

WARNING: Operating at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V: Note 1)

Item	Symbol	min	typ	max	Unit
Power supply voltage					
Analog	AVDD	3.0	3.3	3.6	V
Digital	DVDD	3.0	3.3	3.6	V

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in the datasheet.

Note) Do not turn off the power of the AK7742 during the power supplies of surrounding devices are turned on. VDD must not exceed the pull-up of SDA and SCL of I^2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

ANALOG CHARACTERISTICS

■ ADC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, ADC differential input, CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo ADC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (-1dBFS) (Note 4)	TDB	84		dB
	Dynamic range (A-weighted) (Note 4)	TDB	96		dB
	S/N (A-weighted) (Note 4)	TDB	96		dB
	Inter-channel isolation (f=1kHz) (Note 5)	90	105		dB
	DC accuracy				
	Channel gain mismatch		0.1	0.3	dB
	Analog input				
	Input voltage (differential input) (Note 6)	±1.85	±2.00	±2.15	Vp-p
	Input voltage (single-end input) (Note 7)	1.85	2.00	2.15	Vp-p
	Input impedance (Note 8)	41	62		kΩ

Note 4. This value is not guaranteed for single-ended inputs.
Note 5. Indicates isolation between L and R when -1dBFS signal is applied.
Note 6. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN.
Note 7. Target input pins are AIN2L, AIN2R, AIN3L, AIN3R.
Note 8. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R.

■ DAC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, ADC differential input, CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo DAC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (0dBFS)	TBD	92		dB
	Dynamic range (A-weighted)	TBD	106		dB
	S/N (A-weighted)	TBD	106		dB
	Inter-channel isolation (f=1kHz)(Note 9)	90	105		dB
	DC accuracy				
	Channel gain mismatch		0.2	0.5	dB
	Analog output				
	Output voltage (Note 10)	3.36	3.66	3.96	Vp-p
	Load resistance	5			kΩ
	Load capacitance			30	pF

Note 9. Indicates isolation between each DAC's of Lch and Rch when -1dBFS signal is applied.
Note 10. Full scale output voltage. The output voltage scales with AVDD.

DC CHARACTERISTICS

(Ta=-20ºC ~70ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
High level input voltage (Note 11)	VIH	80%DVDD			V
Low level input voltage (Note 11)	VIL			20%DVDD	V
SCL, SDA High level input voltage	VIH	70%DVDD			V
SCL, SDA Low level input voltage	VIL			30%DVDD	V
High level output voltage Iout=-100μA	VOH	DVDD-0.5			V
Low level output voltage Iout=100μA (Note 12)	VOL			0.5	V
SDA Low level output voltage Iout=3mA	VOL			0.4	V
Input leak current (Note 13)	Iin			±10	μA
Input leak current (pull-down) (Note 14)	Iid		22		μA
Input leak current XTI pin	Iix		26		μA

Note 11. Except for the SCL, SDA pin.
Note 12. Except for the SDA pin.
Note 13. Except for the TESTI pin, XTI pin.
Note 14. The TESTI pin has an internal pull-down device, nominally 150kΩ.

POWER CONSUMPTION

(Ta=25ºC; AVDD=DVDD=3.0~3.6V(typ=3.3V, max=3.6V))

Parameter	min	typ	max	Unit
Power supply current (Note 15)				
Normal Operation AVDD+DVDD		75	TBD	mA
Reset (IRESETN= "L" reference data) AVDD+DVDD (Note 16)		2		mA

Note 15. Depends on the system frequency and contents of DSP program.
Note 16. This is a reference value when using a crystal oscillator. Since most of the supply current at the initial reset state is in the oscillator section, the value may vary according to the crystal type and the external circuit. This value is just reference.

DIGITAL FILTER CHARACTERISTICS

■ ADC

(Ta=-20ºC ~70ºC, AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Pass band (±0.005dB) (Note 18)	PB	0		21.5	kHz
(-0.02dB)			21.768		kHz
(-6.0dB)			24.00		kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 18)	PR			±0.005	dB
Stop band attenuation (Note 19, Note 20)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		30		Ts
Digital filter + Analog filter characteristics					
Amplitude characteristic 20Hz~20.0kHz			±0.01		dB

Note 17. Each parameter is related to the sampling frequency (fs). HPF response is not included.
Note 18. Pass band is from DC to 21.5kHz when fs=48kHz.
Note 19. Stop band is from 26.5kHz to 3.0455MHz when fs=48kHz.
Note 20. When fs=48kHz, the analog modulator samples the analog input at 3.072MHz. Therefore the input signal is not attenuated by the digital filter in multiple bands (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3 …) of the sampling frequency.

■ DAC

(Ta=-20ºC ~70ºC, AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 21)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 21)	SB	26.2			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	64			dB
Group delay (Ts=1/fs) (Note 22)	GD	-	24		Ts
Digital filter + Analog filter					
Amplitude characteristic 0~20.0kHz			±0.5		dB

Note 21. Pass band and Stop band parameter is related to sampling frequency(fs). PB=0.4535fs (at-0.05dB), SB=0.5465fs.
Note 22. The digital filter's delay is calculated as the time from setting 24-bit data into the input register until an analog signal is output.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-20ºC~70ºC; AVDD=DVDD=3.0~3.6V)

Parameter		Symbol	min	typ	max	Unit
XTI						
a)with a crystal oscillator						
Frequency(256fs) CKM[2:0]= 000	fs=44.1KHz fs=48KHz	fXTI	-	11.2896 12.288	-	MHz
CKM[2:0]= 001		fXTI	-	16.9344 18.432	-	MHz
b)with an external clock						
Duty cycle		Duty	40	50	60	%
Frequency(256fs) CKM[2:0]= 000, 010	fs=44.1KHz fs=48KHz	fXTI	11.0	11.2896 12.288	12.4	MHz
Frequency (384fs) CKM[2:0]= 001	fs=44.1KHz fs=48KHz	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK frequency (Note 23)		Fs	7.35	48	96	kHz
BICK frequency						
a) CKM[2:0]= 001, 010			32	64		fs
High level width		tBCLKH	64			ns
Low level width		tBCLKL	64			ns
Frequency		fBCLK	0.46	3.072	6.144	MHz
b) CKM[2:0]= 011 (Note 25)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	2.75	3.072	3.1	MHz
c) CKM[2:0]= 100 (Note 26)				32		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	230	256	258	kHz
d) CKM[2:0]= 101 (Note 27)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	460	512	516	kHz

Note 23. LRCK frequency and sampling rate (fs) should be the same.
Note 24. The BICK must be divided 32, 48 or 64 clocks correctly. (BICK can be selected from 32fs, 48fs or 64fs)
Note 25. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.
Note 26. When BICK is resource of internal MCLK. The BICK must be divided 32 clocks correctly. 32fs fixed.
Note 27. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.

■ Reset

(Ta=-20ºC ~70ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
IRESET (Note 28)	tRST	600			ns

Note 28. It is necessity that the power is supplied and master clock is input when the IRESET pin goes to "H".

■ Audio Interface

1) SDIN1, SDIN2, SDOUT1, SDOUT2, SDOUT3

(Ta=-20ºC ~70ºC; AVDD=DVDD=3.0~3.6V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BICK frequency	fBCLK	32	64		fs
BICK low level width	tBCLKL	150			ns
BICK high level width	tBCLKH	150			ns
Delay time from BICK "↑" to LRCK (Note 29)	tBLRD	40			ns
Delay time from LRCK to BICK "↑" (Note 29)	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from LRCK to serial data output	tLRD	-10		40	ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-10		40	ns
Master mode					
BICK frequency	fBCLK		64		fs
BICK duty cycle			50		%
Delay time from BICK "↑" to LRCK	tBLRD	40			ns
Delay time from LRCK to BICK "↑"	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-30		40	ns

Note 29. BICK rising edge must not occur at the same time as LRCK edge.

Note 30. The serial data output is synchronized to BICK falling edge, and held until next BICK falling (spec -10ns) in Slave mode. In case of the LRCK edge comes before BICK edge, data will be held until LRCK edge (spec -10ns). In Master mode, serial data is held until 30ns before falling edge of BICK. Therefore, please use BICK rising edge in both slave and master modes for a safety latch.

■ I²CBUS Interface

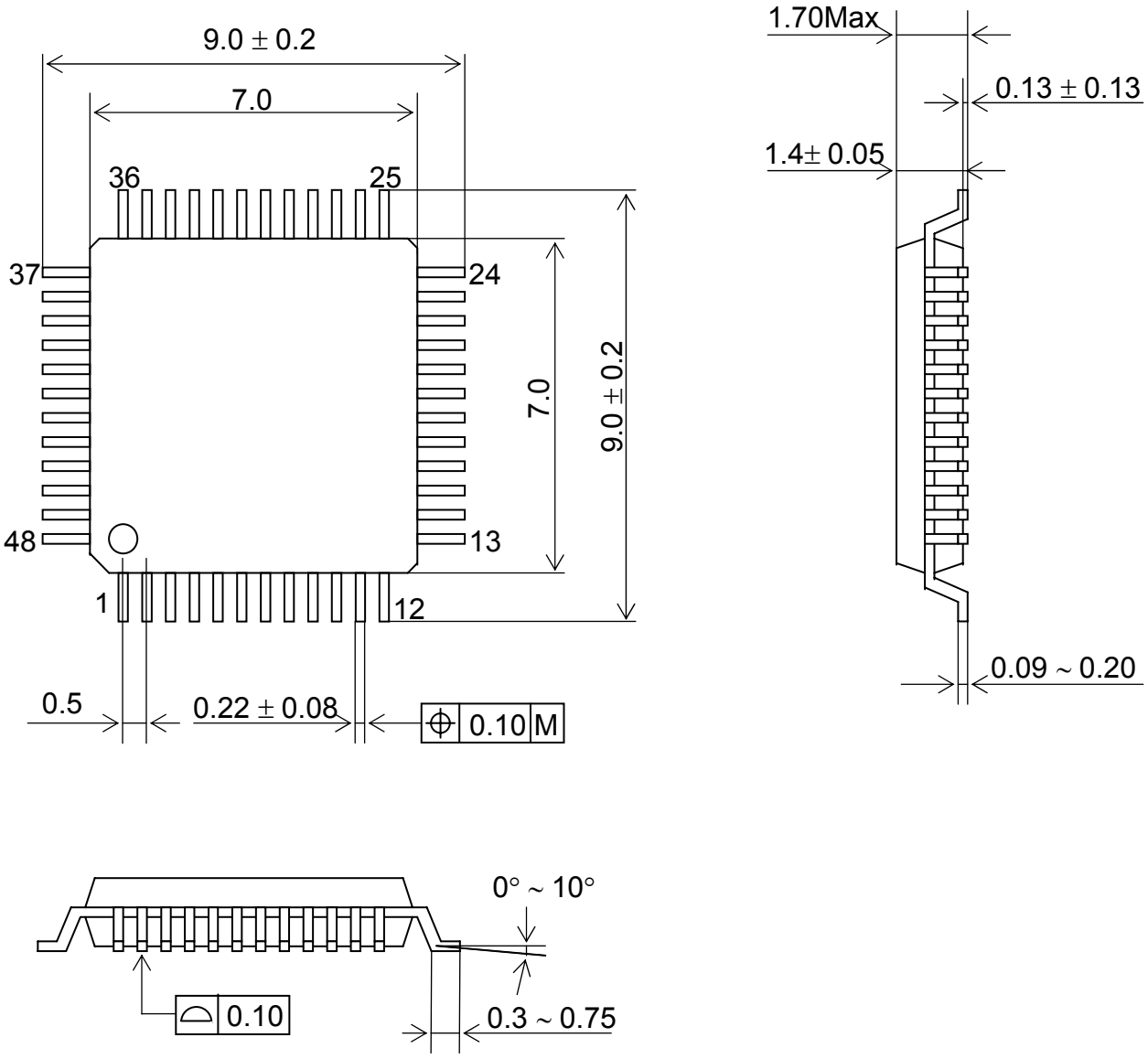
(Ta=-20ºC~70ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL			400	KHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 31. I²C is a registered trademark of Philips Semiconductors.

PACKAGE

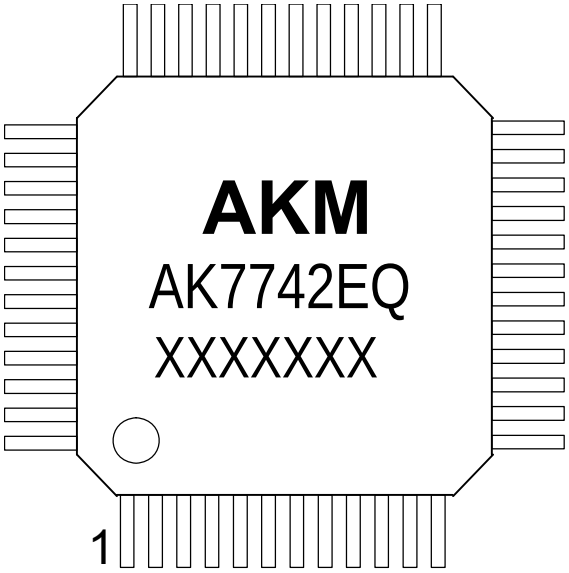
48pin LQFP (Unit: mm)



■ Materials and Lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7digits)
3) Marking Code: AK7742EQ
4) Asahi Kasei Logo

Thank you for your access to AKEMD product information.
More detail product information is available, please contact our sales office or authorized distributors.