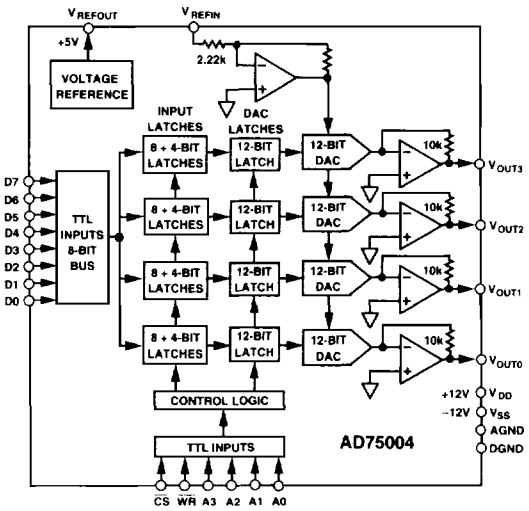
Quad 12-Bit D/A Converter

AD75004

FEATURES

- 4 Complete 12-Bit D/A Functions
- Double-Buffered Latches
- Simultaneous Update of All DACs Possible
- ±5 V Output Range
- High Stability Bandgap Reference
- Monolithic BiMOS Construction
- Guaranteed Monotonic over Temperature
- 3/4 LSB Linearity Guaranteed over Temperature
- 4 µs max Settling Time to 0.01%
- Operates with ±12 V Supplies
- Low Power: 720 mW max Including Reference
- TTL/5 V CMOS Compatible Logic Inputs
- 8-Bit Microprocessor Interface
- 24-Pin PDIP or 28-Lead PLCC Package

FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD75004 contains four complete, voltage output, 12-bit digital-to-analog converters, a high stability bandgap reference, and double-buffered input latches on a single chip. The converters use 12 precision high speed bipolar current steering switches and laser-trimmed thin-film resistor networks to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latches. The design of the input latches allows direct interface to 8-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 50 ns, allowing use with fast microprocessors.

The functional completeness and high performance of the AD75004 results from a combination of advanced switch design, the BiMOS II fabrication process, and proven laser trimming technology. BiMOS II is an epitaxial BiCMOS process optimized for analog and converter functions. The AD75004 is trimmed at the wafer level and is specified to ±1/2 LSB maximum linearity error at 25°C and ±3/4 LSB over the full operating temperature range. The on-chip output amplifiers provide an output range of ±5 V, with 1 LSB equal to 2.44 mV.

The bandgap reference on the chip has low noise, long term stability and temperature drift characteristics comparable to discrete reference diodes. The absolute value of the reference is laser trimmed to +5.00 V with 0.6% maximum error. Its temperature coefficient is also laser trimmed.

Typical full-scale gain TC is 15 ppm/°C. With guaranteed monotonicity over the full temperature range, the AD75004 is well suited for wide temperature range performance.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD75004KN	0°C to +70°C	N-24A
AD75004KP	0°C to +70°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

AD75004—SPECIFICATIONS (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
DIGITAL INPUTS (D0–D7, A0–A3, CS, WR)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	2.0		5.5	V
Input Voltage, Logic "0"	V_{IL}	0		0.8	V
Input Current, V_{IH} = 5.5 V	I_{IH}			10	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			10	μA
Input Capacitance	C_{IN}			10	pF
ACCURACY					
Resolution				12	Bits
Integral Linearity Error			±1/4	±1/2	LSB
Integral Linearity Error, T_{MIN} to T_{MAX}			±1/2	±3/4	LSB
Differential Linearity Error			±1/2	±3/4	LSB
Differential Linearity Error, T_{MIN} to T_{MAX}			Guaranteed Monotonic		
Gain (Full-Scale) Error[1]			±2	±10	LSB
Gain Error Drift, T_{MIN} to T_{MAX}[1]			±15	±30	ppm/°C
Bipolar Zero Error[1]			±1	±2	LSB
Bipolar Zero Error Drift, T_{MIN} to T_{MAX}[1]			±3	±7	ppm/°C
CHANNEL-TO-CHANNEL MISMATCH					
Integral Linearity Error			±1/2	±1	LSB
Gain Error[1]			±1	±4	LSB
Bipolar Zero Error[1]			±1	±2	LSB
DYNAMIC PERFORMANCE					
Settling Time to ±0.01% of FSR for FSR Change, 2 kΩ ‖ 500 pF Load			2	4	μs
Slew Rate, 2 kΩ ‖ 500 pF Load		5			V/μs
Digital Input Crosstalk (Static)[2]				50	dB
ANALOG OUTPUTS					
Full-Scale Range (FSR)	V_{OUT}		±5		V
Output Current	I_{OUT}	±5			mA
Short Circuit Limit Current				±40	mA
VOLTAGE REFERENCE					
Reference Output Voltage	V_{REFOUT}	4.97	5.00	5.03	V
Temperature Coefficient			±15	±25	ppm/°C
Reference Output Current[3]		3.0	5.0		mA
Reference Input Voltage	V_{REFIN}	4.5	5.0	5.5	V
Reference Input Current @ 5.0 V	I_{REFIN}			3.0	mA
POWER SUPPLY GAIN SENSITIVITY					
$\Delta Gain/\Delta V_{DD}$, V_{DD} = +10.8 to +13.2 V dc[1]			±15	±25	ppm of FSR/%
$\Delta Gain/\Delta V_{SS}$, V_{SS} = −10.8 to −13.2 V dc[1]			±15	±25	ppm of FSR/%
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{SS}	±10.8	±12	±13.2	V
Supply Currents	I_{DD}, I_{SS}		±25	±30	mA
TEMPERATURE RANGE					
Specification	T_{MIN}, T_{MAX}	0		+70	°C
Storage		−65		+150	°C

NOTES

[1]Gain and bipolar zero errors are measured using internal voltage reference and include its errors.

[2]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from $V_{OUT,MIN}$ to $V_{OUT,MAX}$ into a 2 kΩ ‖ 500 pF load by means of varying the digital input code.

[3]The internal voltage reference is intended to drive on-chip only; buffer it if using it externally.

[4]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.