National Semiconductor

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74ABT16501
18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

To ensure the high-impedance state during power up or power down, OE inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

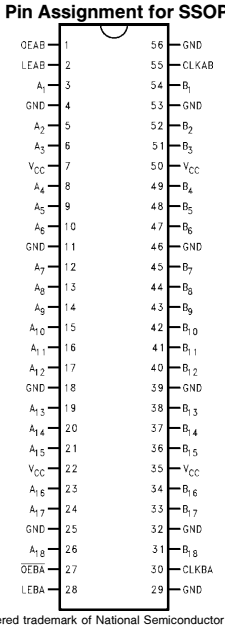
Commercial	Package Number	Package Description
74ABT16501CSSC (Note 1)	MS56A	56-Lead (0.300″ Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT16501CMTD (Notes 1, 2)	MTD56	56-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13″ reel. Use suffix = SSCX and MTDX.

Note 2: Contact factory for package availability.

Connection Diagram

Pin Assignment for SSOP



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Function Table†

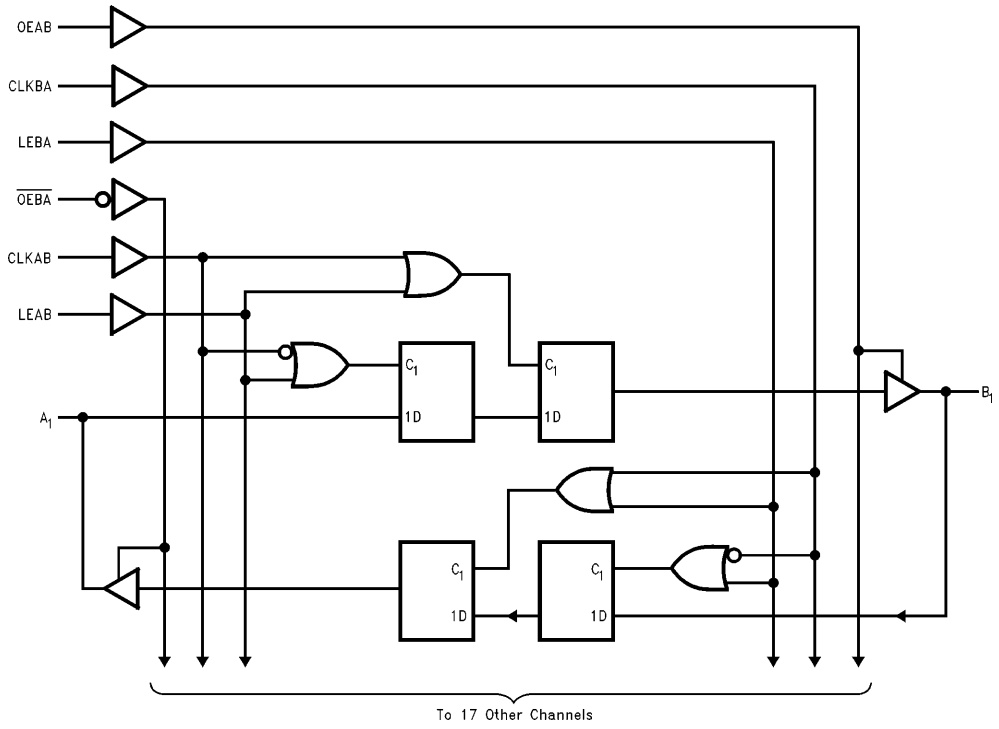
Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Logic Diagram



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16501 Min	ABT16501 Typ	ABT16501 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74ABT	2.5			V	Min	I_{OH} = −3 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	74ABT			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V (Note 1) V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V (Note 1) V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$, OE = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$, OE = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				68	mA	Max	An or Bn Outputs Low
I_{CCZ}	Power Supply Current				1.0	mA	Max	$\overline{OE}_n$ = V_{CC}, All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.23	mA/MHz	Max	Outputs Open Transparent Mode One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF; $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.2	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.5	−1.0		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	150	200		150		MHz
t_{PLH}	Propagation Delay A or B to B or A	1.0	2.7	4.6	1.0	4.6	ns
t_{PHL}		1.0	3.2	4.6	1.0	4.6	
t_{PLH}	Propagation Delay LEAB or LEBA to B or A	1.0	3.1	5.0	1.0	5.0	ns
t_{PHL}		1.0	3.6	5.5	1.0	5.5	
t_{PLH}	Propagation Delay CLKAB or CLKBA to B or A	1.0	3.4	5.3	1.0	5.3	ns
t_{PHL}		1.0	3.7	5.3	1.0	5.3	
t_{PZH}	Propagation Delay OEAB or $\overline{OEBA}$ to B or A	1.5	2.7	5.6	1.5	5.6	ns
t_{PZL}		1.5	3.0	5.6	1.5	5.6	
t_{PHZ}	Propagation Delay OEAB or $\overline{OEBA}$ to B or A	1.5	3.7	6.0	1.5	6.0	ns
t_{PLZ}		1.5	3.2	6.0	1.5	6.0	

AC Operating Requirements

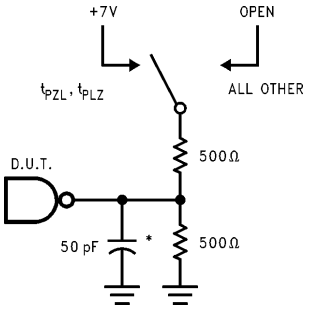
Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, A to CLKAB, B to CLKBA	4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, A to CLKAB, B to CLKBA	0 0		0 0		ns
$t_s(H)$ $t_s(L)$	Setup Time, A to LEAB or B to LEBA, $\overline{CLK}$ High	4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, A to LEAB or B to LEBA, $\overline{CLK}$ High	1.5 1.5		1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup Time, A to LEAB or B to LEBA, $\overline{CLK}$ Low	1.5 1.5		1.5 1.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, A to LEAB or B to LEBA, $\overline{CLK}$ Low	1.5 1.5		1.5 1.5		ns
$t_w(H)$ $t_w(L)$	Pulse Width, LEAB or LEBA, High	3.3 3.3		3.3 3.3		ns
$t_w(H)$ $t_w(L)$	Pulse Width, CLKAB or CLKBA, High or Low	3.3 3.3		3.3 3.3		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
$C_{I/O}$ (Note 1)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

AC Loading



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*Includes jig and probe capacitance.

FIGURE 1. Standard AC Test Load

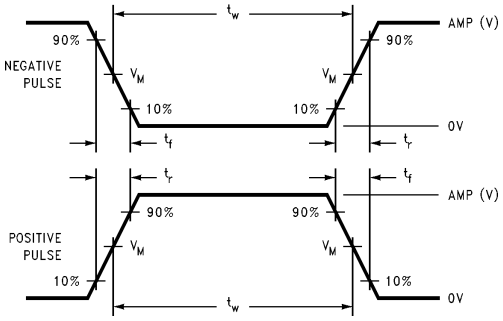

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FIGURE 2a. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements

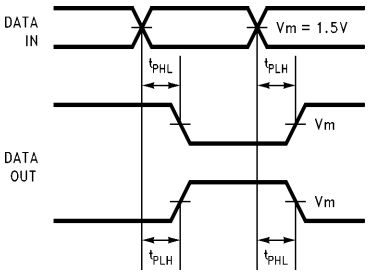

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

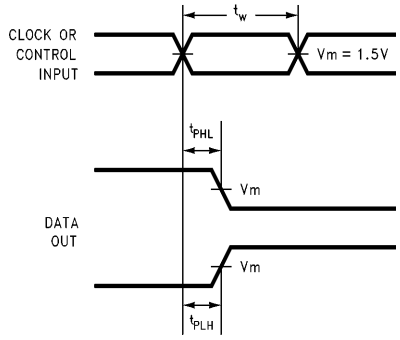

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

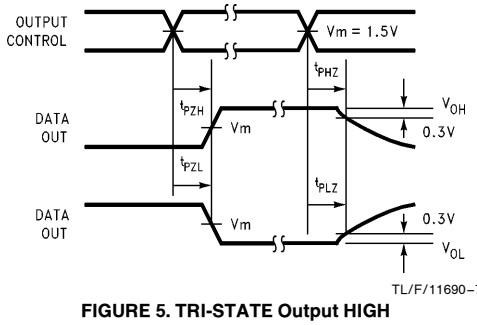

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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

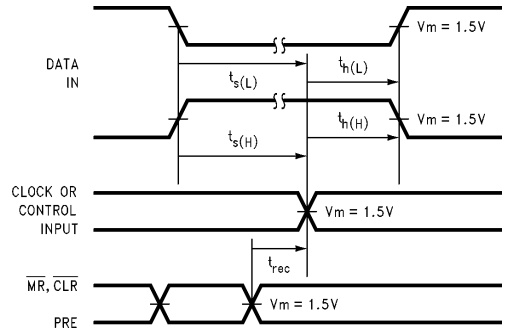

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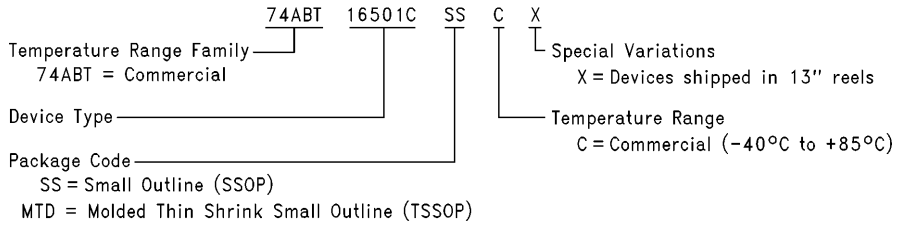
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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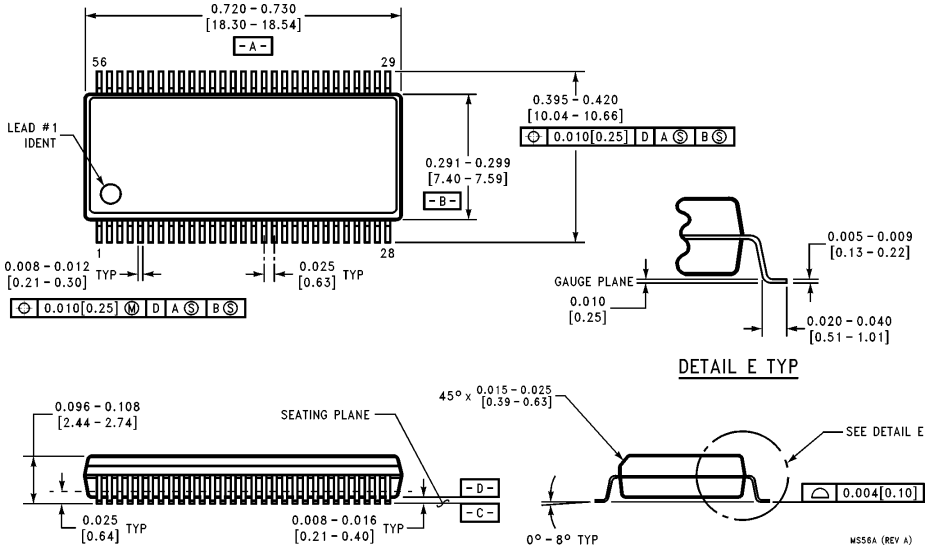
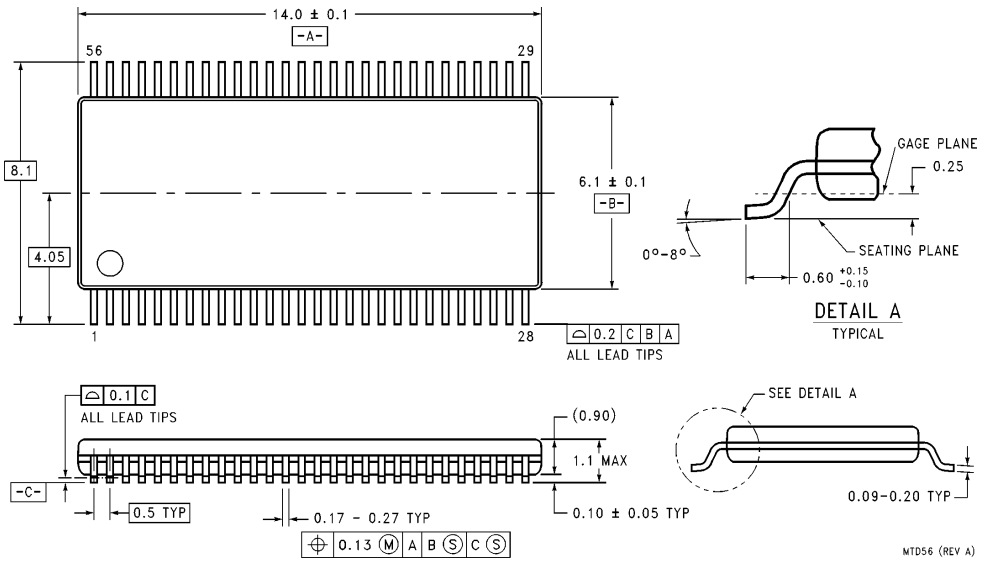
Physical Dimensions inches (millimeters)



56-Lead SSOP (0.300″ Wide) (SS)
NS Package Number MS56A

Physical Dimensions millimeters (Continued)



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56

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