LMX5251 Bluetooth™ CMOS Radio

Check for Samples: LMX5251

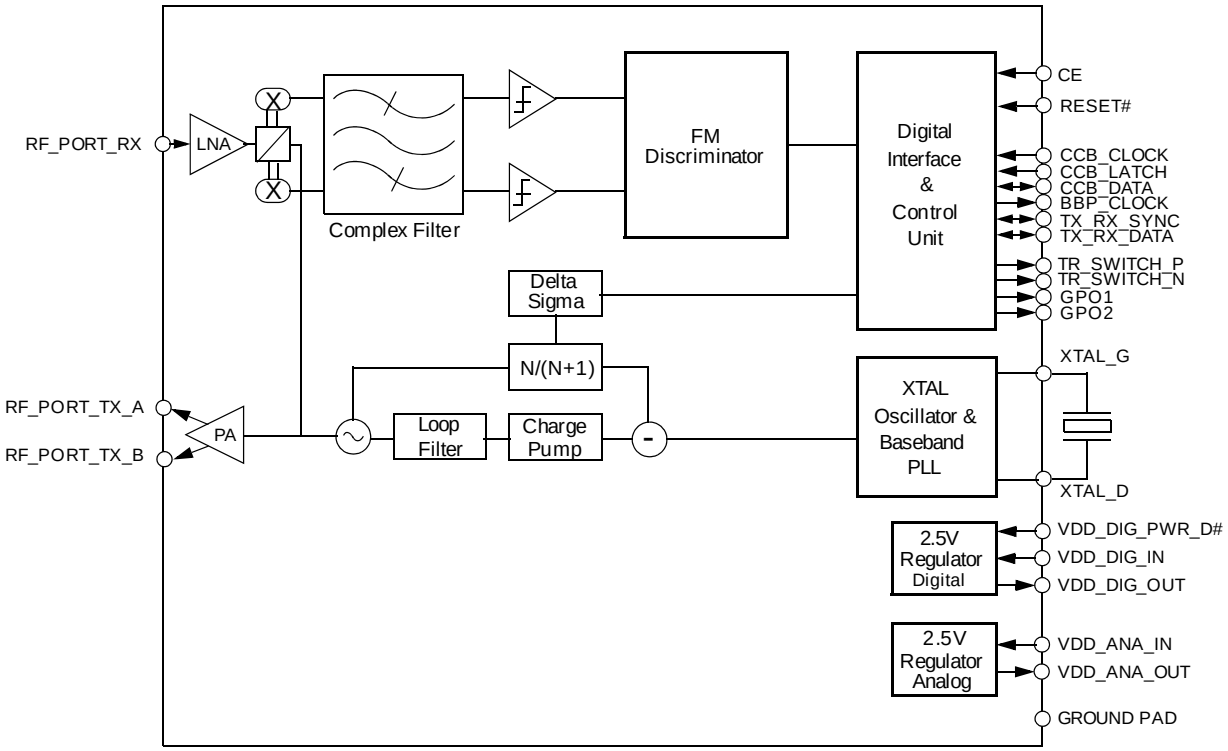
FEATURES

- **Bluetooth Version 1.1 Qualified**
- **Flexible Radio Frequency (RF) to Baseband (BB) Interface**
- **LOW POWER**
  - **Low Current Consumption**
  - **Power Management Control Functions**
- **HIGH PERFORMANCE**
  - **< -82 dBm Sensitivity**
  - **Class 2/3 Operation**
  - **± 1/12 Bit Sampling Resolution**
  - **Closed LoopM ΔΣ Modulation**
- **HIGH INTEGRATION**
  - **Low IF (Intermediate Frequency) Architecture with Digital Demodulation**
  - **Integrated Radio Frequency Voltage Controlled Oscillator (RFVCO)**
  - **Dual on-chip Voltage Regulators:)**
    - **Input Voltages 2.85V–3.6V**
    - **Output Nominally 2.5VM**
  - **48-pin WQFN (Thin Quad Flatpack No lead) Package**
  - **No Pb Leadframe – LMX5251SQ NOPB**

APPLICATIONS

- **Bluetooth Compatible Interface Devices**
- **Cellular and Cordless Phones, PDAs**
- **Desktop and Laptop PCs, Printers, Scanners**
- **Other Wireless-Interfaced Appliances**

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a trademark of Bluetooth Sig, Inc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The LMX5251 is a high performance, monolithic, radio transceiver optimized for Bluetooth™™ communications systems. When used in conjunction with a Bluetooth baseband controller, a complete Bluetooth node with a Host Control Interface (HCI) can be implemented.

The LMX5251 radio architecture allows for minimal external components. The highly integrated design includes the Low Noise Amplifier (LNA), mixer, on-chip filters, 2.5 GHz delta-sigma phase-lock loop (ΔΣ PLL), voltage controlled oscillator, modem functions, and dual power supply regulators. Digital modulation and demodulation techniques are utilized for a robust manufacturable design. Power management includes control over individual chip functions and internal voltage regulation for optimum performance.

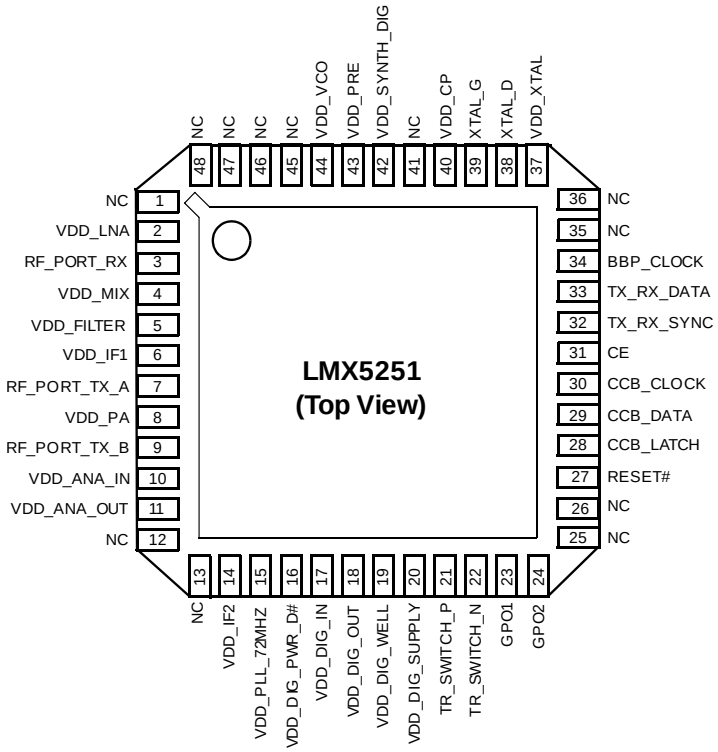
The LMX5251 modem circuitry provides the data communication link to the Bluetooth baseband controller. The interface is flexible and works with solutions that require a standalone Bluetooth radio. The LMX5251 can be placed in Sleep mode (reducing system current consumption) and is optimized for low power operation. It operates from a single 2.85V to 3.6V power supply.

The LMX5251 is manufactured using a CMOS process and is available in a 48-pin WQFN (Thin Quad Flatpack, No lead) package. Die processing is also available through Texas Instruments Die Products Group.

The LMX5251 is the most recent revision of the LMX5250 and is completely interoperable with the LMX5100 Bluetooth Baseband Controller.

CONTENTS

CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Ground pad layout under ground slug of LMX5251 is required. These are connected by vias through all layers to ground plane. No pins on device are ground pins so center slug must be grounded. See detail in Figure 27 "Component Placement Layer 1 Ground Pad Detail".

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1, 12, 13, 25, 26, 35, 36, 41, 45–48	–	**No Connect.** Place pin but do not connect to VCC or Ground.
VDD_LNA	2	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
RF_PORT_RX	3	I	**RF Input to Receiver.**
VDD_MIX	4	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_FILTER	5	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_IF1	6	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
RF_PORT_TX_A	7	O	**Transmit Positive Differential Output.** Typically connected along with RF_PORT_TX_B to a balun and fed to the antenna.
VDD_PA	8	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RF_PORT_TX_B	9	O	**Transmit Inverted Differential Output.** Typically connected along with RF_PORT_TX_A to a balun and fed to the antenna.
VDD_ANA_IN	10	PWR	**2.85V to 3.6V Input for the Internal Power Supply Regulator for the RF Circuitry.** Powered down when CE (pin 31) is held low.
VDD_ANA_OUT	11	PWR	**Voltage Regulator Output/Power Supply for Analog Circuitry.** The bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_IF2	14	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_PLL_72MHZ	15	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_DIG_PWR_D#	16	I	**Power Down for the Internal Power Supply Regulator for the Digital Circuitry.** Digital regulator is powered down when low. Default operation is on, internal pull-up.
VDD_DIG_IN	17	PWR	**2.85V to 3.6V Input for the Internal Power Supply Regulator for the Digital Circuitry.**
VDD_DIG_OUT	18	PWR	**Voltage Regulator Output/Power Supply for Digital Circuitry.** A bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_DIG_WELL	19	PWR	**Power Supply for Digital Circuitry.** Must be connected to the VDD_DIG_OUT pin (pin 18) or external supply. A bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_DIG_SUPPLY	20	PWR	**Power Supply for Digital Circuitry.** Must be connected to the VDD_DIG_OUT pin (pin 18) or external supply. A bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
TR_SWITCH_P	21	O	**Output Control for RF T/R Switch.** The complement of TR_SWITCH_N. When the LMX5251 is transmitting, TR_SWITCH_P is high.
TR_SWITCH_N	22	O	**Output Control for RF T/R Switch.** The complement of TR_SWITCH_P. When the LMX5251 is receiving, TR_SWITCH_N is high.
GPO1	23	O	**General Purpose Output 1.** The multifunction output state is programmed by setting an internal register.
GPO2	24	O	**General Purpose Output 2.** The multifunction output state is programmed by setting an internal register.
RESET#	27	I	**Master Power on Inverted Reset Input.** Internal registers revert to default values while RESET# is low. The power control register default state enables only the crystal oscillator and BBP_CLOCK blocks.
CCB_LATCH	28	I	**Load Enable Signal of the Serial Interface.** During write operations (baseband controller writes into LMX5251 registers) the data received by the shift register of the LMX5251 is copied into the address register on the next rising edge of CCB_CLOCK after the CCB_LATCH signal has transitioned to high. During read operations (read from LMX5251 registers) the LMX5251 releases the CCB_DATA line on the next rising edge of CCB_CLOCK after the CCB_LATCH signal has transitioned to high. Reference serial port timing Figure 19 and Figure 20.
CCB_DATA	29	I/O	**Multiplexed Serial Data Receive and Transmit Signal Path.** For a write operation, data is clocked into the LMX5251 shift register in the direction from the most significant bit (MSB) to the least significant bit (LSB). The data is shifted out of the baseband controller on the falling edge of CCB_CLOCK, and sampled by the LMX5251 (CCB_DATA) on the rising edge of CCB_CLOCK. For a read operation, data is clocked out of the LMX5251 shift register in the direction from MSB to LSB. The data is shifted out of the LMX5251 (CCB_DATA) on the rising edge of CCB_CLOCK, and sampled by the baseband controller on the falling edge of CCB_CLOCK. Reference serial port timing Figure 19 and Figure 20.
CCB_CLOCK	30	I	**Serial Interface Shift Clock Signal.** The baseband controller always acts as the master of the serial interface and therefore always provides the shift clock. This clock can be asynchronous with the BBP_CLOCK and is assumed to be gated by the baseband controller. Reference serial port timing Figure 19 and Figure 20.
CE	31	I	**Chip Enable Input.** All analog blocks and the analog regulator are off and there is no BBP_CLOCK signal. All digital blocks and the digital regulator are on.
TX_RX_SYNC	32	I/O	**Transmit and Receive Slot Timing Synchronization.**

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TX_RX_DATA	33	I/O	**Multiplexed Transmit and Receive Bluetooth Data.** In receive mode (Bluetooth data direction from LMX5251 to baseband controller), this signal is provided by the LMX5251 demodulator (RX_DATA) to the baseband coNtroller data receiver oversampled at a 12x multiple of the 1.0 Mbit/s rate. In transmit mode, (Bluetooth data direction from baseband controller to LMX5251) this signal is provided by the baseband controller packet generator to the LMX5251 modulator (TX_DATA) at a 1.0 Mb/s rate. A pulse on this bus provided by the baseband controller prior to the beginning of data transmission is used to synchronize the LMX5251 to the baseband controller to an internal 1.0 MHz transmit clock timing.
BBP_CLOCK	34	O	**Buffered 12.000 MHz Clock.** This 12 MHz clock is provided by the LMX5251 and is used by the baseband controller as the fast system clock (main clock). The 12 MHz clock is also used in the LMX5251 demodulator and baseband controller data receiver as the sampling clock (12 times over-sampling) for the Bluetooth data. During Bluetooth low power modes, the XTAL oscillator and BBP_CLOCK output of the LMX5251 can be disabled. Upon RESET# being low, this pin is in TRI-STATE mode.
VDD_XTAL	37	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
XTAL_D	38	I	**Crystal Drain Oscillator or Positive Clock Input.** Typically connected along with XTAL_G to an external surface mount AT cut crystal. Can also be configured as a frequency input when using an external crystal oscillator. When configured as a frequency input, it is typically connected to Ground with a 100 pF capacitor.
XTAL_G	39	I	**Crystal Gate Oscillator or Negative Clock Input.** Typically connected along with XTAL_D to an external surface mount AT cut crystal. Can also be configured as a frequency input when using an external crystal oscillator. When configured as a frequency input, is typically connected to an external Temperature Compensated Crystal Oscillator (TCXO) through an Alternating Current (AC) coupling capacitor.
VDD_CP	40	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_SYNTH_DIG	42	PWR	**Power Supply for Digital Circuitry.** Must be connected to the VDD_DIG_OUT pin (pin 18) or external supply. A bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_PRE	43	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.
VDD_VCO	44	PWR	**Power Supply for Analog Circuitry.** Must be connected to the VDD_ANA_OUT pin (pin 11) or external supply. An RF bypass capacitor should be placed as close as possible to this pin and be connected to Ground.

ELECTRICAL SPECIFICATIONS

GENERAL SPECIFICATIONS

The ABSOLUTE MAXIMUM RATINGS table indicate limits beyond which damage to the device may occur. The RECOMMENDED OPERATING CONDITIONS table indicate conditions for which the device is intended to be functional, but do not specify specific performance limits.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

The following conditions are true unless otherwise stated in the tables below:

- T_A = –40°C to +85°C
- VDD_ANA_IN and VDD_DIG_IN = 3.3V
- RF system performance specifications are specified on Texas Instruments Dallas Board rev 2.0a reference design platform.
- Reference Dallas Board rev 2.0a schematic for test point references.

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
VDD_ANA_IN	Analog LDO voltage input	–0.2	3.6	V
VDD_DIG_IN	Digital LDO voltage input	–0.2	3.6	V
VDD_XXXXX	All other power supply voltage inputs	–0.2	2.75	V
V_I	Voltage on any pin with GND = 0V	–0.2	VDD + 0.2	V
PinRF	RF Input power		+15	dBm
T_S	Storage temperature range	–65	+150	°C
T_L	Lead temperature (solder 4 sec)		+235	°C
T_{NOPBL}	No Pb lead temperature (solder 4 sec)		+260	°C
ESD-HBM	ESD – Human Body Model		2000 (1)	V
ESD-MM	ESD – Machine Model		200	V

(1) A 2000V ESD rating applies to all pins except VDD_IF1(pin 6) = 1500V.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP(1)	MAX	UNIT
VDD_ANA_IN	Analog power supply voltage(2)	2.85	3.3	3.6	V
VDD_LNA		2.25	2.5	2.75	V
VDD_FILTER					
VDD_IF1					
VDD_PA					
VDD_IF2					
VDD_PLL					
VDD_MIX					
VDD_XTAL					
VDD_CP					
VDD_PRE					
VDD_VCO					
VDD_DIG_IN	Digital power supply voltage(2)	2.85	3.3	3.6	V
VDD_DIG_WELL		2.25	2.5	2.75	V
VDD_DIG_SUPPLY					
VDD_SYNTH_D					
T_S	Operating temperature range	–40		85	°C

(1) Typical operating conditions are at 3.3V operating voltage and 25°C ambient temperature.
(2) Maximum voltage difference between input voltage for analog VDD and digital VDD is 500 mV.

POWER SUPPLY REQUIREMENTS(1)

PARAMETER		MIN	TYP(2)	MAX	UNIT
I_{CC}-RX	Receive power supply current (receive in Continuous mode)		62	78	mA
I_{CC}-TX	Transmit power supply current (transmit in Continuous mode)		56	68	mA
I_{CC}-PWDN(3)	Power-down current		24	200	µA

(1) Power supply requirements based on Class II output power.
(2) Typical operating conditions are at 2.85V operating voltage and 25°C ambient temperature.
(3) CE and V_{DD}_DIG_PWR_D# low.

POWER SUPPLY ELECTRICAL SPECIFICATIONS

PARAMETER		MIN	TYP(1)	MAX	UNIT
ANALOG AND DIGITAL LDOS					
VDD_ANA_IN VDD_DIG_IN	Analog and digital voltage input range(2)(3)	2.85	3.3	3.6	V
VDD_ANA_OUT VDD_DIG_OUT	Analog and digital voltage output range(4)	2.41	2.54	2.69	V

(1) Typical operating conditions are at 3.3V operating voltage and 25°C ambient temperature.
(2) Maximum voltage difference between input voltage for analog VDD and digital VDD is 500 mV.
(3) Maximum allowed input voltage supply ripple is 100mVp-p.
(4) Set in factory at 2.5V nominal output.

DC CHARACTERISTICS DIGITAL I/O

PARAMETER		CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	VDD_DIG_IO = 2.85V	0.8_{IOVCC}		V
V_{IL}	Low-level input voltage			0.2_{IOVCC}	V
I_{IH}	High-level input current	V_{IH} = VDD_DIG_IO = 2.85V	–1	1	µA
I_{IL}(1)	Low-level input current	V_{IL} = 0	–1	1	µA
V_{OL}	Low-level output voltage	I_{OL} = 100 µA		0.2	V
V_{OH}	High-level output voltage	I_{OH} = 100 µA	V_{DD} –0.2		V

(1) Limit for I_{IL} for the pins Reset, CE and VDD_DIG_PWR_D# is ±3uA.

RF PERFORMANCE CHARACTERISTICS

In the performance characteristics tables the following applies:

1. All tests performed based on Bluetooth Test Specification rev 0.91.
2. All tests at antenna port unless otherwise specified.
3. VDD = 3.3V unless otherwise specified.
4. T_A = –40°C to +85°C
5. RF system performance specifications are specified on Texas Instruments Dallas Board rev 2.0a reference design platform.
6. Reference Dallas Board rev 2.0a schematic for test point references.

RECEIVER PERFORMANCE CHARACTERISTICS

PARAMETER		CONDITION		MIN	TYP(1)	MAX	UNIT
RX_{sense}(2)	Receive sensitivity	BER < 0.001	2.402 GHz		–79	–72	dBm
			2.441 GHz		–79	–72	dBm
			2.480 GHz		–79	–72	dBm
PinRF	Maximum input level			–20	0		dBm
C/I_{CCI}	Carrier to interferer ratio in the presence of co-channel interferer	$P_{in}RF$ = –60 dBm, BER < 0.001			9	11	dB
C/I_{ACI}	Carrier to interferer ratio in the presence of adjacent channel interferer	ΔF_{ACI} = ± 1 MHz, $P_{in}RF$ = –60 dBm, BER < 0.001			-3	0	dB
		ΔF_{ACI} = + 2 MHz, $_{Pin}RF$ = –60 dBm, BER < 0.001			–42	–30	dB
		ΔF_{ACI} = + 3 MHz, $P_{in}RF$ = –67 dBm, BER < 0.001			–46	–40	dB
C/I_{IMAGE}	Carrier to interferer ratio in the presence of image interferer	ΔF= –2 MHz, $P_{in}RF$ = –67 dBm, BER < 0.001			–20	–9	dB
C/I_{IMAGE} 1MHz	Carrier to interferer ratio in the presence of image-1mHz interferer	Δf = –3 MHz, $P_{in}RF$ = –67 dBm, BER < 0.001			–32	–20	dB
IMP(3)	Intermodulation performance	F_1 = + 3 MHz, F_2 = + 6 MHz, $P_{in}RF$ = –64 dBm		–39	–31		dBm
Z_{RFIN}(4)	Input impedance of RF port (RF_inout)	Single input impedance, F_{in} = 2.5 GHz			50		Ω
Return Loss(5)	Return Loss					–8	dB
OOB	Out Of Band Blocking Performance	$P_{in}RF$ = -10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001		–10			dBm
		$P_{in}RF$ = -27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001		–27			dBm
		$P_{in}RF$ = -27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001		–27			dBm
		$P_{in}RF$ = -10 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001		–10			dBm

(1) Typical operating conditions are at 3.3V operating voltage and 25°C ambient temperature.
(2) The receiver sensitivity is measure at the device interface.
(3) The f_0 = –64 dBm Bluetooth modulated signal, f_1 = –39dbm sine wave, f_2 = –39 dBm Bluetooth modulated signal, $f_0 = 2f_1 – f_2$, and $|f_2 – f_1| = n \times 1MHz$, where n is 3, 4, or 5. For the typical case, n = 3.
(4) Reference Smith chart Figure 4.
(5) Reference chart Figure 5.

TRANSMITTER PERFORMANCE CHARACTERISTICS

PARAMETER		CONDITION	MIN	TYP(1)	MAX	UNIT
$P_{OUT}RF$(2)	Transmit output power	2.402 GHz	–1	3	7	dBm
		2.441 GHz	–1	3	7	dBm
		2.480 GHz	–1	3	7	dBm
Power Density	Power density		–4	1	2	dBm

(1) Typical operating conditions are at 3.3V operating voltage and 25°C ambient temperature.
(2) The output power is measure at the device interface.

TRANSMITTER PERFORMANCE CHARACTERISTICS (continued)

PARAMETER		CONDITION	MIN	TYP(1)	MAX	UNIT
MOD $\Delta F1_{AVG}$	Modulation characteristics	Data = 00001111	140	165	175	kHz
MOD $\Delta F2_{MAX}$(3)		Data = 10101010	115	125		kHz
$\Delta F2_{AVG}/\Delta F1_{AVG}$(4)	Modulation characteristics		0.8			
ACP(5)	Adjacent channel power (In-band spurious)	+ 500 kHz			–20	dBc
		| M N | = 2	–50	–48	–20	dBm
		| M N | > 3	–53	–51	–40	dBm
$P_{OUT}2\times fo$(6)	PA 2nd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz		–77		dB
$P_{OUT}3*fo$(3)	PA 3rd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 7206 MHz		–98		dB
Z_{RFOUT}(7)	RF Output Impedance/Input Impedance of RF Port (RF_inout)	P_{out} at 2.5 GHz		50		Ω
Return Loss(8)	Return Loss				–14	dB

(3) ΔF2max > 115 kHz for at least 99.9% of all Δf2max.
(4) Modulation index set between 0.28 and 0.35.
(5) Not tested in production.
(6) Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel. Performance of the radio is significantly better than BT 1.1 specification.
(7) Reference Smith chart Figure 4.
(8) Reference chart Figure 6.

SYNTHESIZER PERFORMANCE CHARACTERISTICS(1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
f_{VCO}	VCO Frequency range		2402		2480	MHz
t_{LOCK}	Lock time	f_0 ± 20 kHz		120		µs
Δf_0offset	Initial carrier frequency tolerance	During preamble	–75	0	75	kHz
Δf_0drift	Initial carrier frequency drift	DH1 data packet	–25	0	25	kHz
		DH3 data packet	–40	0	40	kHz
		DH5 data packet	–40	0	40	kHz
		Drift Rate	–20	0	20	kHz/50µs
t_D-Tx	Transmitter delay time	From Tx data to antenna		4		µs

(1) Frequency accuracy dependent on crystal or oscillator chosen. Crystal/oscillator must have cumulative accuracy specifications of not more than ±20 ppm to meet the Bluetooth specification.

CRYSTAL/OSCILLATOR PERFORMANCE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Crystal oscillator frequency		10	12	26	MHz
f_{ACC}(1)	Frequency accuracy	Cumulative over operating temperature range	–20		20	ppm
t_{OSC-ON}	Oscillator turn-on time	VCC applied, f_{OSC} = 12 MHz, C_{ext} = 0.1 µF, Settled to within f_{ACC}		4		ms
V_{OSC}	Oscillator input voltage	External XO input	0.6		2	Vpp
ESR	Equivalent series resistance			50	100	Ω
D_{CYCLE}	Duty cycle		49%		51%	
P_{NOISE}	Phase noise	100Hz			–105	dBc/Hz
		1000Hz			–125	dBc/Hz
B_{BCLK}	Baseband clock output frequency			12		MHz

(1) Frequency accuracy dependent on crystal or oscillator chosen. Crystal/oscillator must have cumulative accuracy specifications of ±15 ppm to provide margin for frequency drift with aging and temperature.

AC CHARACTERISTICS SERIAL INTERFACE TIMING

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_{CS}	Data to clock setup time	See Serial Port Timing Diagrams	10			ns
t_{CH}	Data to clock hold time		5			ns
t_{CWH}	Clock pulse width high		20			ns
t_{CWL}	Clock pulse width low		20			ns
t_{ES}	Clock to enable setup time		10			ns
t_{CES}	Enable to clock setup time		20			ns
t_{EWH}	Enable pulse width high		20			ns
t_{EWL}	Enable pulse width low		200			ns
t_{MS}	Master to slave transfer time			70		ns
t_{MTRI}	Master to TRI-STATE setup time		–5		10	ns
t_{SCTL}	Slave control setup time		0		10	ns
t_{SM}	Slave to master return time			60		ns
t_{STRI}	Slave to TRI-STATE setup time		0		10	ns
t_{MCTL}	Master control setup time		–-5		10	ns

PERFORMANCE PARAMETERS (TYPICAL)

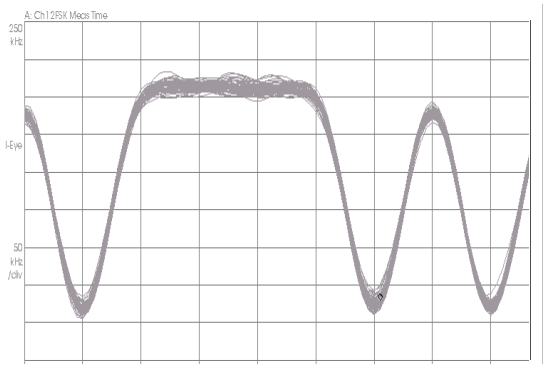


Figure 1. Modulation

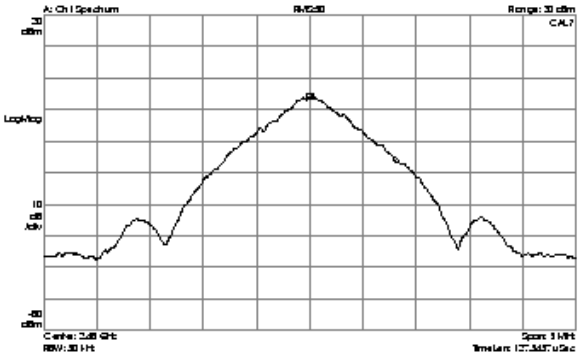


Figure 2. Transmit Spectrum

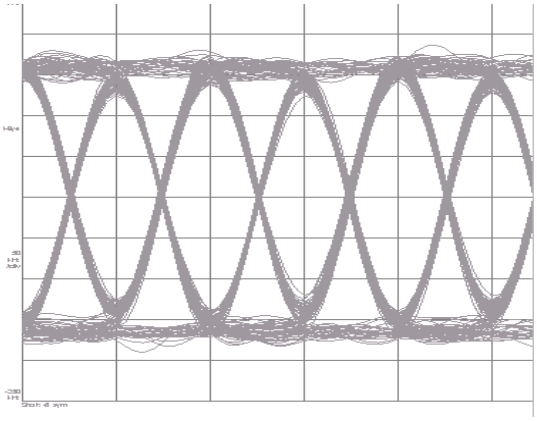


Figure 3. Corresponding Eye Diagram

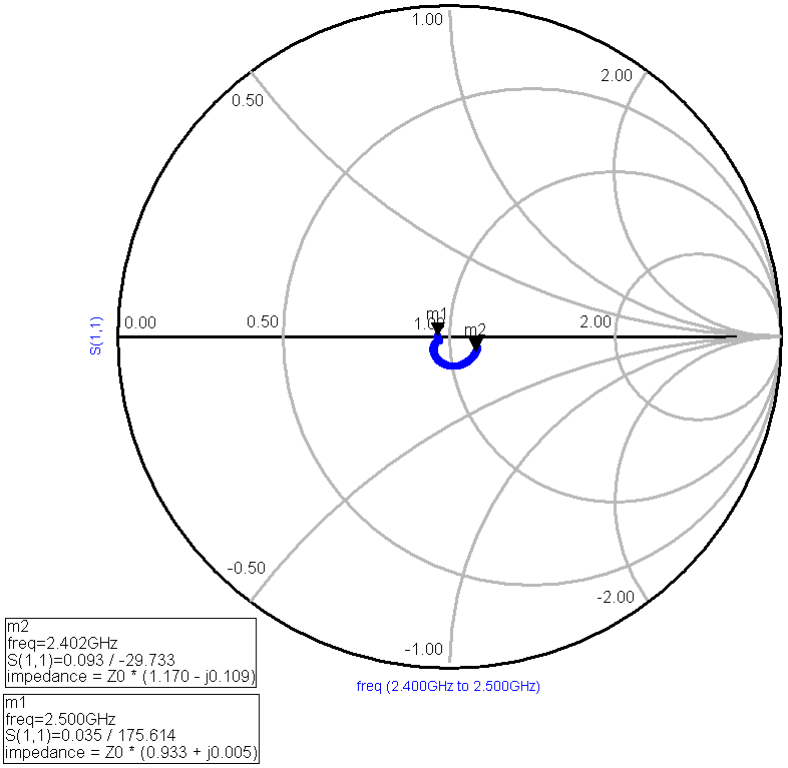


Figure 4. TX and RX Pin 50Ω Impedance Characteristics

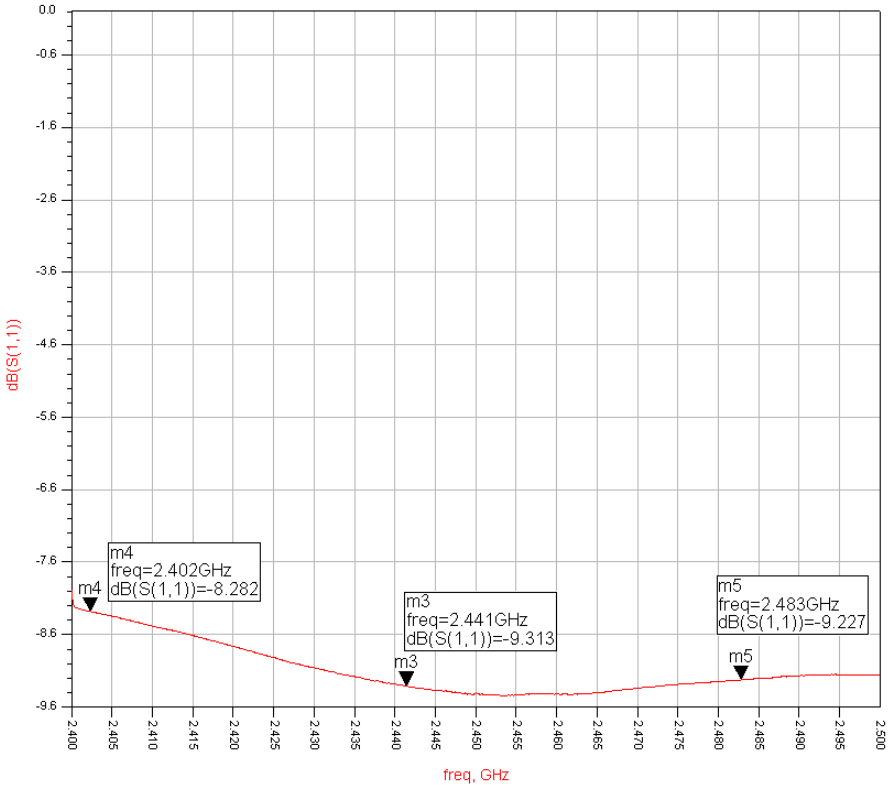


Figure 5. Receiver Return Loss

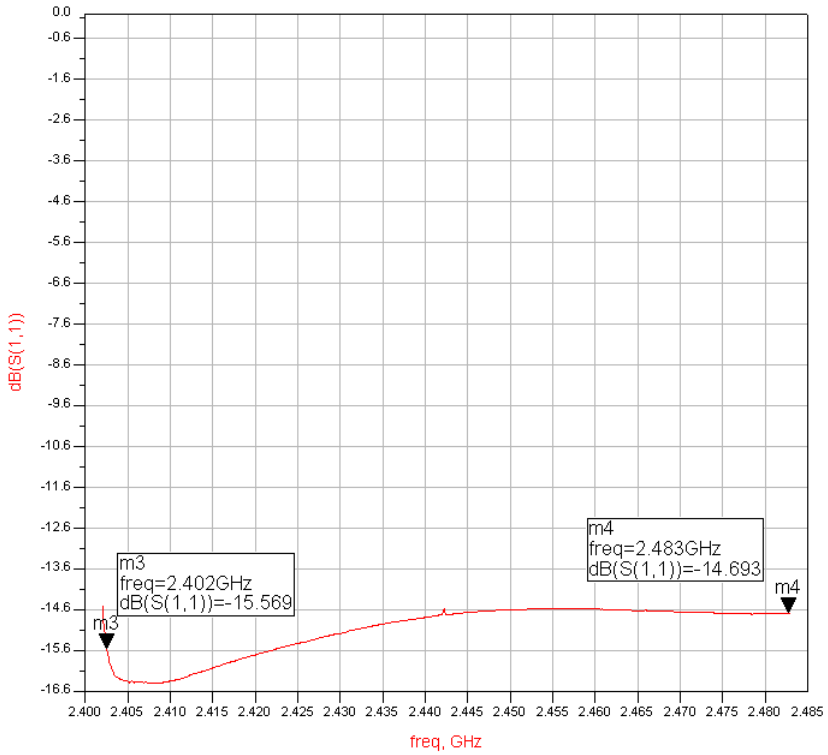


Figure 6. Transmitter Return Loss

FUNCTIONAL DESCRIPTION

The LMX5251 is a high performance, monolithic, radio transceiver optimized for Bluetooth communications systems. When used in conjunction with a Bluetooth baseband controller (e.g., LMX5100), a complete Bluetooth node with a Host Control Interface (HCI) can be implemented.

The LMX5251 radio architecture allows for minimal external components. The highly integrated design includes the low noise amplifier (LNA), mixer, on-chip filters, 2.5 GHz ΔΣ PLL, voltage controlled oscillator (VCO), power amplifier (PA) driver, and modem functions. Digital modulation and demodulation techniques are utilized for a robust manufacturable design. Power management includes control over individual chip functions and internal voltage regulation for optimum performance.

The LMX5251 is optimized for low power operation, while maintaining sensitivity performance. The main external components required consist of a crystal (or other clock source) and assorted de-coupling capacitors to form a complete Class 2 Bluetooth radio transceiver. Optional components, based on the requirements of a particular application may include a band select filter, T/R switch, and a differential to single ended balun (discrete or microstrip). The T/R switch and balun are required only if one antenna is used instead of two antennas.

Radio Receiver

The signal path of the RX architecture contains an internal LNA and quadrature RF downconverting mixer at 2.5 GHz. A low intermediate frequency (IF) receiver provides high performance at low cost and low current consumption. The IF demodulator is implemented digitally in combination with a limiting amplifier.

Low Noise Amplifier

The on-board low noise amplifier (LNA) is a single-ended structure designed with a 50Ω input impedance for simple capacitive matching. The LNA is closely integrated with the mixer providing low noise and good immunity from blocking signals.

RX Mixer

The receive mixer is an image reject ring diode type mixer. An internal low noise gain block is incorporated prior to the mixer to achieve extremely low noise performance. A differential IF output improves noise immunity while maintaining a high intercept point.

Channel Select Filter

The IF circuitry is followed by an integrated complex active bandpass filter that provides the required channel selectivity and image rejection. The I and Q outputs of the filter are then converted to the digital domain using a limiter, discriminator, and A/D converter.

Limiter

The limiter circuit consists of I and Q limiting amplifiers that provide the remaining gain in the receiver such that an acceptable signal level exists at the frequency modulation (FM) discriminator. Limiting amplification of the downconverted wanted signal minimizes the input range requirements of the A/D converter.

FM Discriminator

The limited signal is translated to digital format using an analog frequency shift keying (FSK) demodulator and A/D converter. The A/D extracts the RX signal at a sample rate of 72.0 MHz.

Receive Signal Strength Indicator

The receive signal strength indicator (RSSI) signal is derived from the input level to the limiter and covers a range low detector level = -59dBm and high detector level = -38dBm. The information is typically fed back to the baseband controller via the serial interface.

Radio Transmitter

The signal path of the TX architecture contains an internal modulator for 1 Mb/s GFSK (Gaussian Frequency Shift Keying) modulation of the 2.5 GHz VCO. Closed loop ΔΣ modulation is chosen, since it is the most low power solution. The integrated pre-amplifier provides output levels sufficient for Class 2 Bluetooth operation.

Modulator

The encrypted, whitened, transmit data stream is supplied by the baseband controller to the LMX5251 via the TX_RX_DATA pin (pin 33). An internal digital Gaussian filter provides the FSK modulation waveform. A modulation input to the completely integrated 2.5 GHz ΔΣ PLL provides a consistent modulation deviation. This eliminates the risks of open loop modulation such as frequency drift and frequency offset.

Transmit Frequency Output

The transmit RF output is differential, and typically connected to the antenna through a passive balun.

Frequency Synthesizers

The 2.4 to 2.5 GHz RF range is provided by an on-chip voltage controlled oscillator (VCO). A programmable 2.5 GHz ΔΣ PLL selects the channel frequency. An internal crystal oscillator can be configured with a 10 to 26 MHz crystal, or for TCXO frequency input. Internal dividers provide internal clocks and clock outputs to the baseband controller.

Voltage Controlled Oscillator

The transmit VCO is configured differentially, with an internal tank circuit, and tuning varactor. The input modulated signal is supplied from the internal ΔΣ PLL.

Crystal Circuit

Due to the need for clock accuracy, the LMX5251 has a dedicated crystal oscillator. The LMX5251 uses the crystal to supply a 12 MHz clock source to the baseband controller. The 12 MHz is buffered, providing a receive data clock to the baseband controller. It is also possible to configure the crystal oscillator for input only when another high quality crystal oscillator is available in the system. The LMX5251 can accommodate crystals from 10 to 26 MHz in increments of 10 kHz.

External Crystal Oscillators

The LMX5251 each contain a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. (See Figure 7 and Figure 23). The LMX5251 also can operate with an external TCXO (Temperature Compensated Crystal Oscillator).

Crystal

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

1. Load Capacitance

   For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in Figure 8 is composed of:

   – C1 (motional capacitance)
   – R1 (motional resistance)
   – L1 (motional inductance)
   – C0 (static or shunt capacitance)

   The LMX5251 provide some of the load with internal capacitors C_{int}. The remainder must come from the external capacitors labeled Ct1 and Ct2 as shown in Figure 7. Ct1 and Ct2 should have the same the value for best noise performance. Crystal load capacitance (C_L) is calculated as the following:

   $$C_L = C_{int} + Ct1//Ct2$$

   The C_L above does not include the crystal internal selfcapacitance C0 as shown in Figure 8, so the total capacitance is:

   $$C_{total} = C_L + C0$$

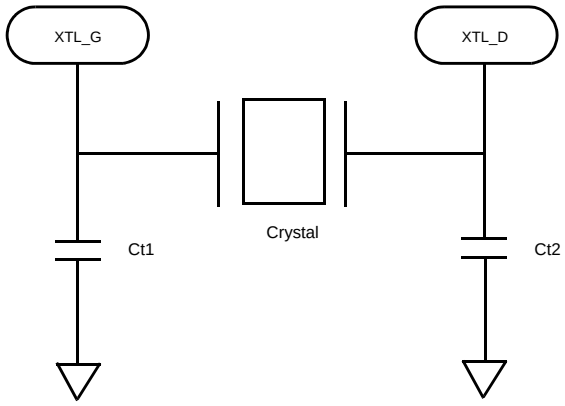


Figure 7. LMX5251 Crystal Recommended Circuit

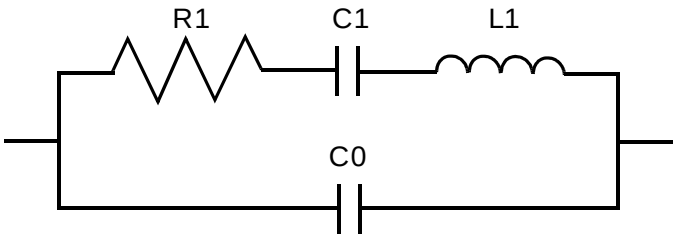


Figure 8. Crystal Equivalent Circuit

2. Crystal Pullability

   Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

3. Frequency Tuning

   Frequency Tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within ±20 ppm. Crystal/oscillator must have cumulative accuracy specifications of ±15 ppm to provide margin for frequency drift with ageing and temperature.

4. Vite Crystal

   The VXE4-1055 is a 12 MHz SMT crystal from Vite. Texas Instruments is using this crystal with the LMX5251. Table 1 shows the specification of VXE4-1055.

   Since the internal capacitance of the crystal circuit is 4-5 pF and the load capacitance is 9 pF, 10 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 9 shows the RF frequency offset test results.

   Figure 9 shows the results are 100 kHz off the center frequency, which is –4 ppm. The pullability of the crystal is 24 ppm/pF, so the load capacitance must be decreased by about 0.2 pF. By changing Ct1 or Ct2 to 9 pF, the total load capacitance is increased by 0.26 pF. Figure 10 shows the frequency offset test results. The frequency offset is now zero with Ct1 = 9 pF, Ct2 = 10 pF.

5. Kineski KSS CX-4025S

   The LMX5251 has also been tested with the Kineski KSS CX-4025S. See Table 2.

Table 1. VXE4-1055-12M000

SPECIFICATION	VALUE
Package	6.0x3.5x1.1 mm 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	±18 ppm at –20 to +70°C (inclusive of all conditions)
Load Capacitance	9 pF
ESR	40 Ω max, 20 Ω typ
Shunt Capacitance	7 pF max
Drive Level	10 to 100 µW
Pullability	24 ppm/pF min
Storage Temperature	–40 to +85°C

Table 2. KSS CX-4025S

SPECIFICATION	VALUE
Package	4.0x2.5x0.75 mm 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	±20 ppm at –30 to +80°C (inclusive of all conditions)
Load Capacitance	12pF
ESR	80 Ω max, 20 Ω typ
Shunt Capacitance	3 pF max
Drive Level	100 µW max
Storage Temperature	–40 to +85°C

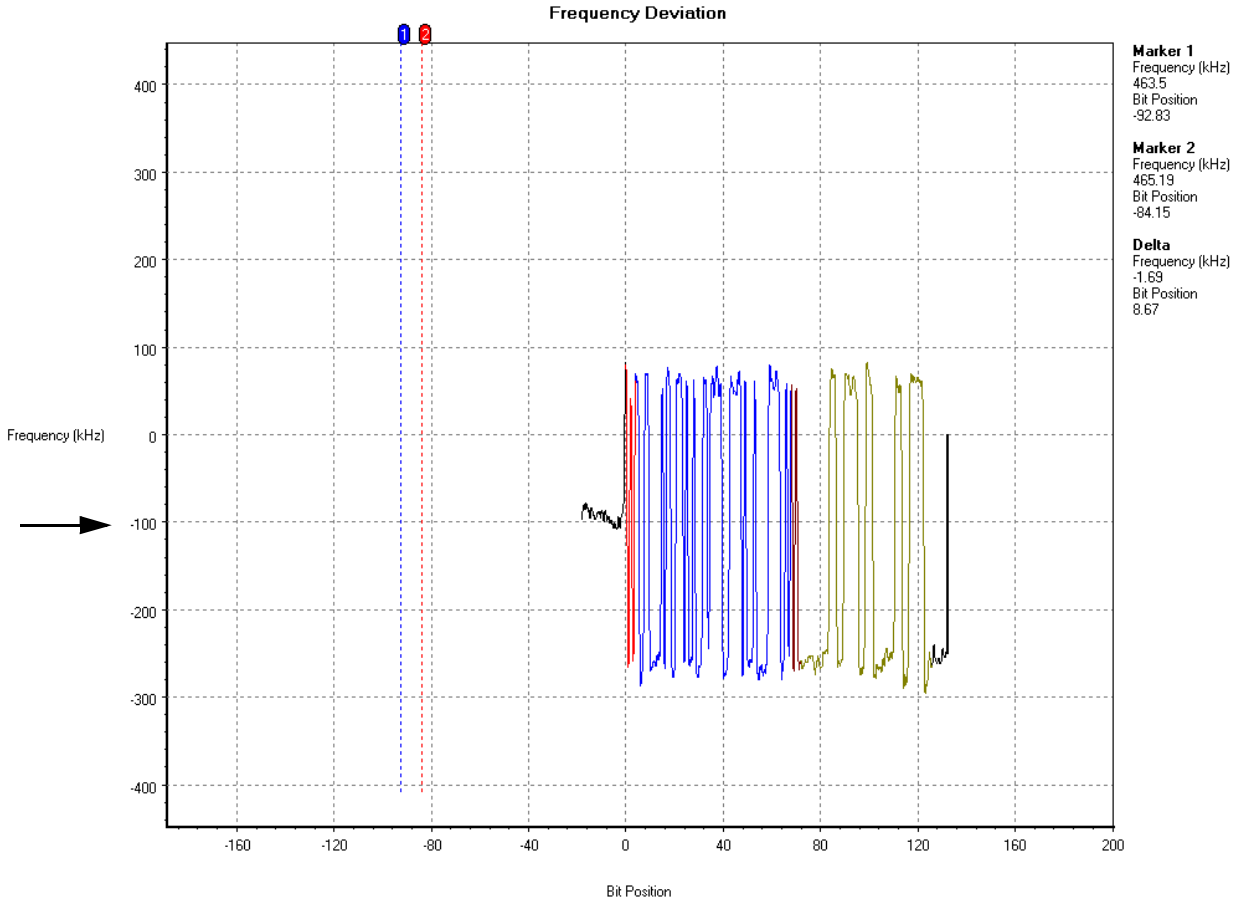


Figure 9. Frequency Offset with 10 pF Capacitors

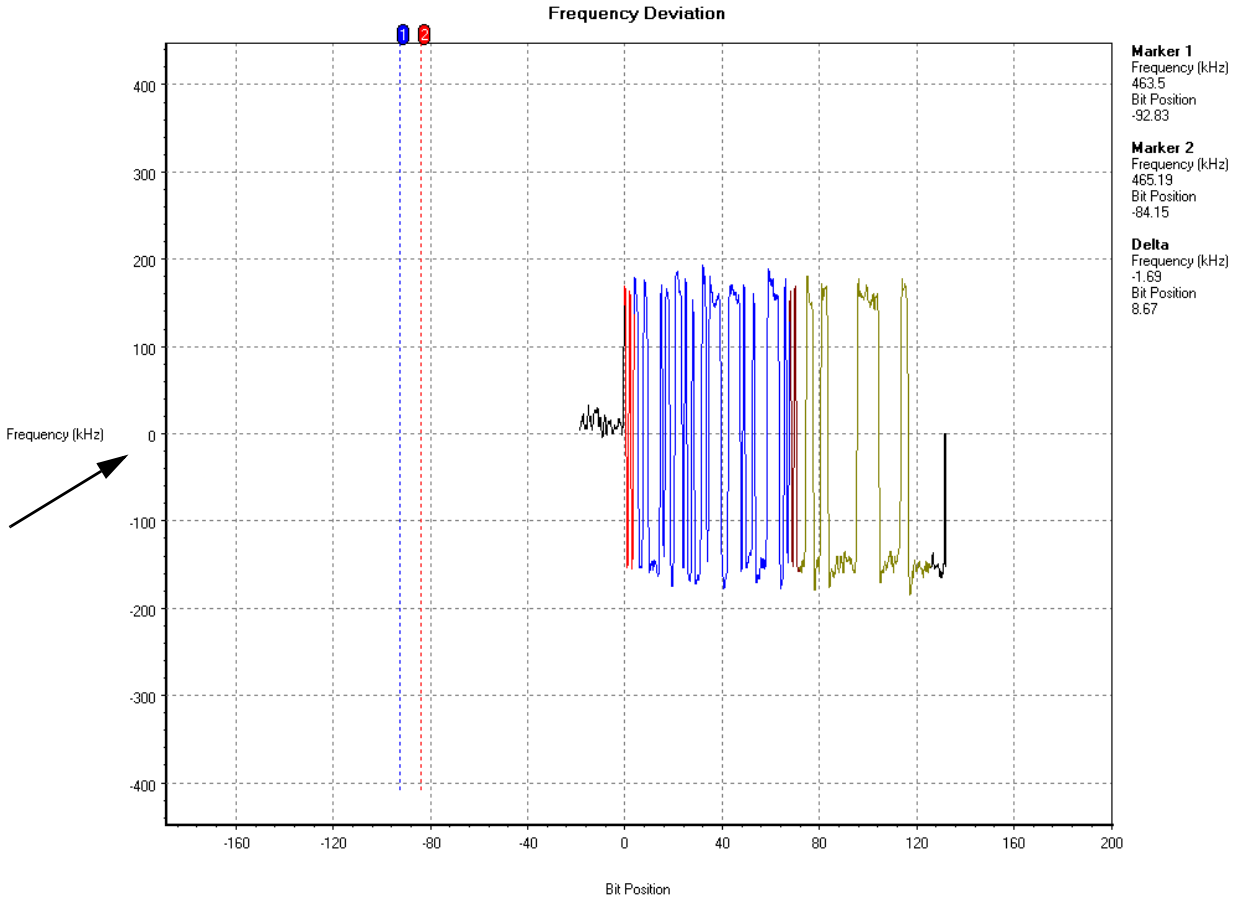


Figure 10. Frequency Offset with 9 pF//10 pF Capacitors

TCXO (Temperature Compensated Crystal Oscillator)

The LMX5251 also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the XTL_G, shown in Figure 24.

1. Input Impedance

   The LMX5251 XTL_G pin has in input impedance of 2pF capacitance in parallel with >400kΩ resistance.

2. NKG3184A TCXO

   The LMX5251 has also been tested with the NKG3184A TCXO. See Table 3.

Table 3. TCXO NKG3184A

SPECIFICATION	VALUE
Package	5.0x3.2x1.4 mm 4 pads
Frequency	12.000 MHz
Stability	±18 ppm at –30 to +85°C (inclusive of all conditions)
Output Load	10kΩ // 13pF
Current Consumption	2.0mA
Output Level	0.3Vp-p to 2.0Vp-p
Storage Temperature	-40 to +85°C
DC Cut Capacitor	Included in VC-TCXO

Multiple Crystal Support

The LMX5251 Bluetooth Radio IC can operate using a large range of crystal frequencies. The on-chip ΔΣ PLL can accommodate crystal frequencies or clock sources from 10 to 26 MHz. In addition, the LMX5251 can generate a 12 MHz Baseband Controller Clock (BBP_CLOCK) using its on-board ΔΣ PLL. For baseband controllers requiring a frequency clock other than 12 MHz, the BBP_CLOCK can be switched to generate a digital signal at the crystal frequency.

Theory of Operation

For 10 to 20 MHz crystals, the LMX5251 doubles the crystal frequency for use on the chip. It generates an internal 12 MHz clock with 24-bit accuracy for its internal processing using one PLL. In addition, it must generate an RF signal for transmit and receive using another PLL with 24-bit accuracy. For 20 to 26 MHz crystals, the LMX5251 does not double the crystal frequency, but still generates the 12 MHz internal clock and RF signal with 24-bit accuracy. The baseband controller must supply the LMX5251 with two correct 24-bit codes so the LMX5251 will generate the 12 MHz internal clock as well as the RF signal correctly:

- Clock_Code_12MHz_PLL = 72 x (10^6) x (2^{16}) / crystal
- Clock_Code_RF_PLL = (2^{16}) x crystal / (10^6)

Serial Interface

The serial interface for the LMX5251 is a 3-wire data clock latch in slave configuration. The interface can also support bidirectional data transfer mode. An option to provide fast write-only programmability is also included. The serial interface is used to program all of the various control registers and state machines in the LMX5251. The read back mode is enabled through a control bit provided by the baseband controller.

Power Control

The power control information for the LMX5251 is stored in dedicated power control registers, which configure the state for the various circuit blocks as long as VDD_ANA_IN is applied. In addition, a hardwire control pin, CE, is available for enabling the entire chip for RX, TX, and Standby modes. While RESET# is low, the LMX5251 registers are reset to the default values. In normal mode, the LMX5251 powers up according to the state of the mode and power control register bits. The default condition powers down all circuit blocks except for the crystal oscillator, crystal oscillator voltage regulator, and baseband controller interface. The RX or TX mode configuration is then programmed via the serial interface.

Voltage Reulation

Voltage is regulated using two 100 mA linear voltage regulators producing the following voltages:

- Input Range: 2.85V to 3.6V
- Output: 2.5V

The LMX5251 crystal oscillator is forced on by the use of the TX_RX_DATA pin. When RESET# is brought high, the TX_RX_DATA pin is also held high by the baseband controller. This allows for a baseband controller bootup sequence. The default state of the crystal oscillator will start up and provide an output to the BBP_CLOCK pin once the level has surpassed a minimum threshold. Once the baseband controller is stable, the TX_RX_DATA pin reverts to normal operation.

Internal Pull-Ups/Downs

LMX5251 has four pads that have either pull-ups or pull downs. Reference Table 4 for details.

Table 4. Internal Pull-Ups/Downs

NAME	DIRECTION	DESCRIPTION
CE	Pull-up	Upon power-up, the LMX5251 generates a 12 MHz baseband clock in default configuration.
RESET#	Pull-up	Upon power-up, RESET# is low, and the LMX5251 registers are reset to the default values. When RESET# transitions low to high, the LMX5251 starts normal operation.
VDD_DIG_PWR_DWN#	Pull-up	Upon power-up, held high to enable digital LDO regulator.
BBP_CLOCK	Pull-down	Upon power-up, a 12 MHz clock is provided by the LMX5251 to the baseband controller. In low power modes, the BBP_CLOCK output of the LMX5251 can be disabled.

APPLICATION INFORMATION

Typical Application Block Diagrams

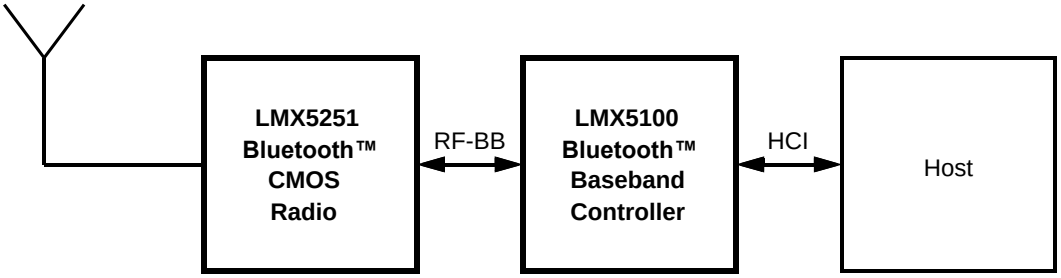


Figure 11. System Application Diagram

LMX5100/LMX5251 Interface

This section describes the interface signals between the LMX5251 and the LMX5100. The LMX5251 interfaces to the LMX5100 via an 8-pin interface, called the RF interface. Figure 12shows how the LMX5100 interfaces to the LMX5251 Bluetooth CMOS Radio chip.

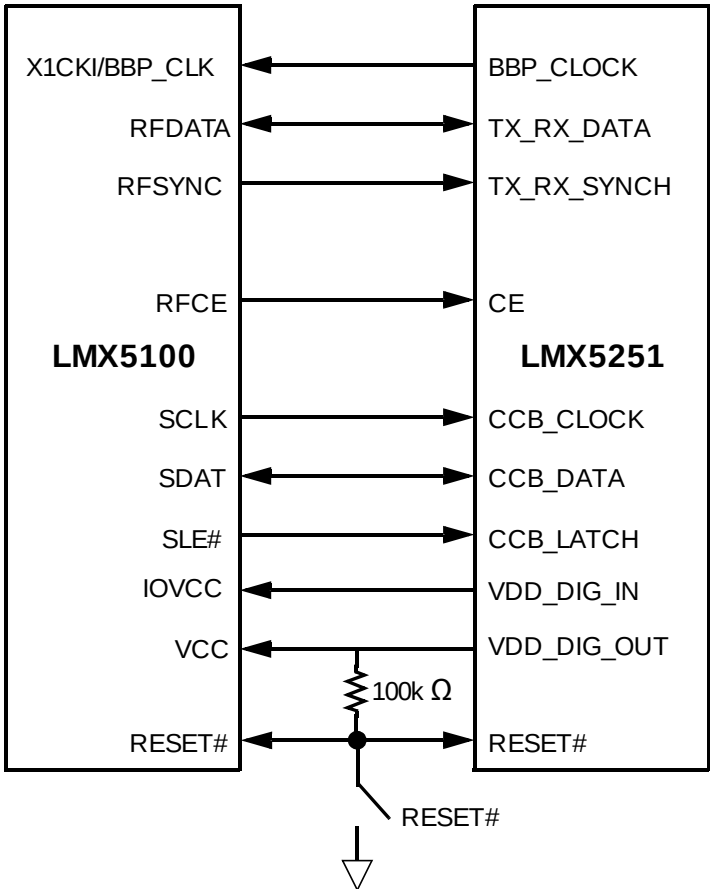


Figure 12. LMX5100/LMX5251 Interface

RF Interface

The LMX5251 and the LMX5100 communicate with each other via an 8-pin digital interface. The RF interface signals can be grouped as:

- Modem Signals (BBP_CLOCK, TX_RX_DATA, and TX_RX_SYNC)
- Chip Enable Control Signal (CE)
- Serial Interface Signals (CCB_CLOCK, CCB_DATA and CCB_LATCH)

BBP_CLOCK (Pin 34): The BBP_CLOCK pin is the output pin for the 12 MHz clock signal to the LMX5100. This 12 MHz clock is provided by the LMX5251 and is used by the LMX5100 as the fast system clock (main clock) as well as the sampling clock (12 times over sampling) for the Bluetooth data, transferred via the TX_RX_DATA pin. During Bluetooth power-down phases, the clock output of the LMX5251 can be disabled by driving the CE pin of the RF interface with a logic low level. However, the RF interface is only allowed to control the clock while the power management module of the LMX5100 has granted “Hardware Clock Control” to the Bluetooth LLC.

TX_RX_DATA (Pin 33): The TX_RX_DATA pin is the multiplexed Bluetooth data receive and transmit pin. The data is provided at a bit rate of 1 Mbit/s and 12 times over sampled corresponding to the 12 MHz BBP_CLOCK. The TX_RX_DATA pin is a dedicated RF interface pin. This pin is driven to a logic high level after reset.

TX_RX_SYNC (Pin 32): In receive mode (data direction from LMX5251 to LMX5100), this pin acts as the frequency correction/DC compensation circuit control output to the LMX5251. The TX_RX_SYNC pin is driven low throughout the correlation phase, and brought high when synchronization to the received access code is achieved.

In transmit mode (data direction from LMX5100 to LMX5251) this pin is used to enable the RF output of the LMX5251. When the TX_RX_SYNC pin is driven high, the RF transmitter circuit of the LMX5251 is enabled, corresponding to the settings of the power control register in the LMX5251.

CE (Pin 31): The CE pin is the chip enable input from the LMX5100 to LMX5251. When the CE pin is driven high, the LMX5251 is powered-up according to the settings of its power control registers. When the CE pin is low, the LMX5251 is powered-down. However, the serial interface is still operational and the LMX5100 can still access the LMX5251 internal control registers.

CCB_CLOCK (Pin 30): The CCB_CLOCK pin is the serial interface shift clock output. The LMX5100 always acts as the master of the serial interface and therefore always provides the shift clock to the LMX5251.

CCB_DATA (Pin 29): The CCB_DATA pin is the multiplexed serial data receive and transmit path from/to the LMX5100.

CCB_LATCH(Pin 28): The CCB_LATCH pin is the serial load enable input of the serial interface of the LMX5251.

During write operations (write to LMX5251 registers), the data received by the shift register of the LMX5251 is latched into the address register on the next rising edge of CCB_CLOCK after the CCB_LATCH signal is driven high.

During read operations (read from LMX5251 registers), the LMX5251 releases the CCB_DATA line on the next rising edge of CCB_CLOCK after the CCB_LATCH signal is driven high.

Receive and Transmit Data Timing

All timing for receive and transmit data exchange is derived from the 12 MHz BBP_CLOCK (pin 34) output of the LMX5251. The LMX5251 always uses the negative edge, and the baseband controller always uses the positive edge of the BBP_CLOCK signal. For receive mode, the LMX5251 controls the TX_RX_DATA bus, and asserts the data from the incoming Bluetooth RF packet onto the TX_RX_DATA pin (pin 33) at the falling edge of the BBP_CLOCK. The baseband controller samples the TX_RX_DATA at the rising edge of BBP_CLOCK to allow for bus transition time and clock skew. The timing diagram for TX_RX_DATA is shown in Figure 13 and Figure 14.

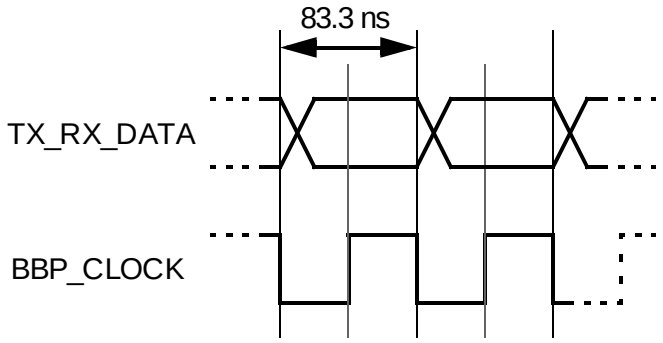


Figure 13. Bluetooth Receive Data Timing

During transmit mode, the baseband controller controls the TX_RX_DATA line, and asserts the data from the outgoing Bluetooth RF packet onto TX_RX_DATA at the rising edge of the BBP_CLOCK. The LMX5251 samples the RX_DATA at the falling edge of BBP_CLOCK after a six BBP_CLOCK period delay, corresponding to a half symbol time delay to allow for sampling at the middle of the data bit.

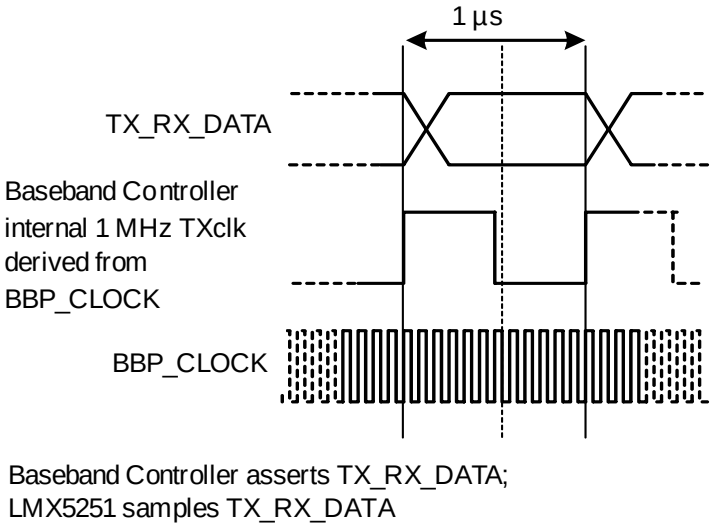


Figure 14. Bluetooth Transmit Data Timing

Receive Mode Slot Timing

Prior to initiating the receive mode, the crystal oscillator must be turned on and settled such that the BBP_CLOCK output is present. The baseband controller programs the LMX5251 receiver (RX) mode and frequency information via the serial interface, at which point the LMX5251 PLL begins acquiring the correct RX frequency channel. After ~100 µs, the receive chain powers up. RX data is then clocked to the baseband controller. The serial port is used to program the LMX5251 out of receive mode.

The LMX5251 has built in flexibility for adjusting the TX_RX_SYNC timing. The default is for the TX_RX_SYNC to go high at the middle of the third trailer bit, T2. The LMX5251 TX_RX_SYNC_del[1:0] programming bits adjust for position of TX_RX_SYNC pulse with respect to center of the trailer bits ±0.5 µs (see Figure 15). When the TX_RX_SYNC pulse goes high at T0, T1, T2, or T3, TX_RX_SYNC_del is set to 0, 1, 2, or 3 respectively. The TX_RX_SYNC_del is set to the delay in usec of the TX_RX_SYNC rising edge relative to the leading edge of the first trailer bit, T0. An example of the TX_RX_SYNC timing for the case when the trailer is 1010 is shown in Figure 15.

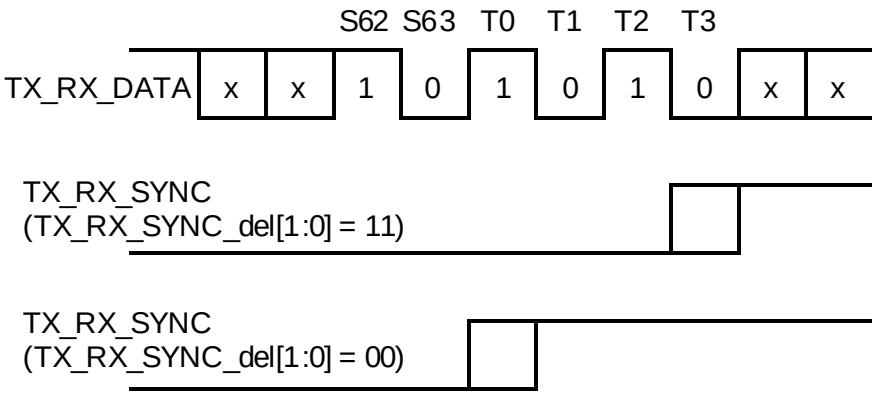


Figure 15. TX_RX_SYNC Timing

Transmit Mode Slot Timing

Prior to initiating the transmit mode, the crystal oscillator must be turned on and settled such that the BBP_CLOCK output is present. The baseband controller programs the LMX5251 transmit mode and frequency information via the serial interface, at which point the LMX5251 PLL begins acquiring the correct TX frequency channel. After ~120 µs, the transmit chain powers up. A TX data synch pulse is provided by the baseband controller to the LMX5251 at least 1 µs before data transmission begins. This allows the LMX5251 to derive a synchronous internal 1 MHz transmit clock. TX data is then clocked into the LMX5251 as shown in Figure 14. The serial port is used to program the LMX5251 out of transmit.

RXMODE 2 Receive Command Sequence

Reset only needs to happen once after power-up. For receive mode, the receive channel frequency is the channel frequency -1 (example: to receive on channel 0 (2402 - 1 = 2401 MHz). RXMODE 2 register values are shown in Table 5.

Table 5. RXMODE 2 Register Values

CCB ADDRESS REGISTER	CCB DATA REGISTER	COMMENT
0x01	0x0181	Receive Channel (2401) and Start RX2 Sequence
0x01	0x0081	Return to Idle

Steps to Receive

1. The LMX5100 programs the Control Registers (CCB registers) with the sequence in Table 5, using the three serial interface pins.
2. The LMX5251 scans the channel until the LMX5100 Idles the chip.
3. The propagation delay between the RF_PORT_RX and the TX_RX_DATA is 4 µs.
4. First the Bluetooth RF Preamble bit exits the TX_RX_DATA pin.
5. When the access code is detected, the LMX5100 brings TX_RX_SYNC high during the trailer. No rigorous timing is required at this time.

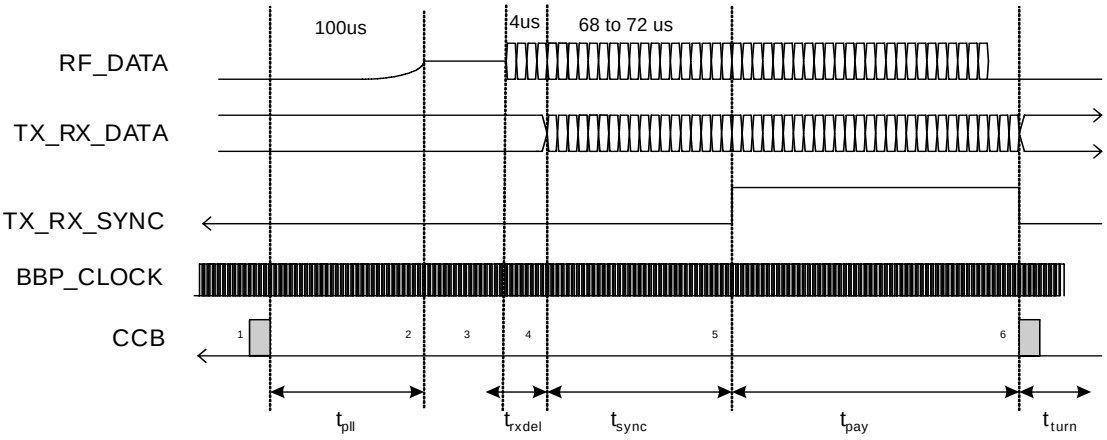


Figure 16. RXMODE 2 Receive Timing

TXMODE 2 Transmit Command Sequence

In TXMODE 2, the baseband controller sends transmit data (and access code) at 1 Mbps to the LMX5251. The base- band controller sends a synchronization pulse 2 µs before the actual data. This pulse is 1 µs in duration. The transmit data is latched into the LMX5251 by an internally gener- ated 1 MHz clock synchronous to the 12 MHz BBP_CLOCK output. TXMODE 2 register values are shown in Table 6.

Table 6. TXMODE 2 Register Values

CCBREGISTER ADDRESS	CCB DATA REGISTER	COMMENT
0x01	0x0101	Transmit Channel (2401) and Start TX2 Sequence
0x01	0x0001	Return to Idle

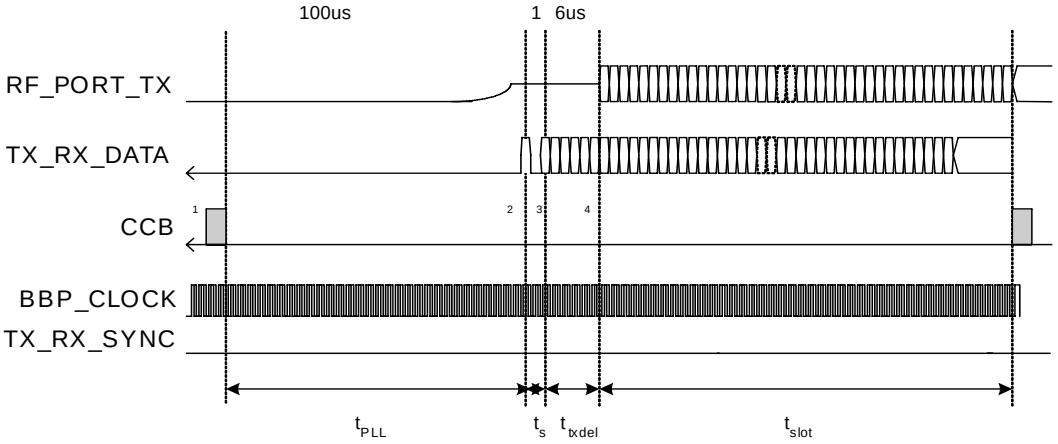


Figure 17. TXMODE 2 Transmit Timing

SYSTEM POWER-UP SEQUENCE

In order to correctly power-up the Bluetooth system (LMX5251 and LMX5100) the following sequence must be performed:

1. Apply VDD to the LMX5251.
2. Apply IOVCC and VCC to the LMX5100.
3. The RESET# pin of the LMX5251 should be driven high minimum of 2ms after the LMX5251 and LMX5100 volt- age rails are high. The LMX5251 and LMX5100 are properly reset.
4. After internal Power-On Reset (POR) of the LMX5100 the TX_RX_DATA pin of the LMX5100 is driven high. The CE, TX_RX_SYNC, and CCB_DATA pins of the LMX5251 are in TRISTATE mode. However, there are pull-up/pull-down resistors built into the CCB_CLOCK, CCB_DATA, CCB_LATCH, and TX_RX_SYNC pins of the LMX5251 to specify the correct initial voltage levels for a proper power-up sequence.
5. The TX_RX_DATA pin driven to logic high level causes the LMX5251 to enable its oscillator. After an oscillator start-up delay, the LMX5251 drives a stable 12 MHz clock (BBP_CLOCK) to the LMX5100.
6. The Bluetooth LLC can now directly control the RF interface pins and set the pins to the logic high levels required during the power-up phase. The CE pin, driven high, forces the LMX5251 to switch from “power-up” to “normal” mode and to disable its internal pull-up/pull-down resistors on the RF interface.
7. In the “normal” mode, the oscillator of the LMX5251 is controlled via the CE pin. Driving the CE pin high enables the oscillator, and the LMX5251 drives the BBP_CLOCK.

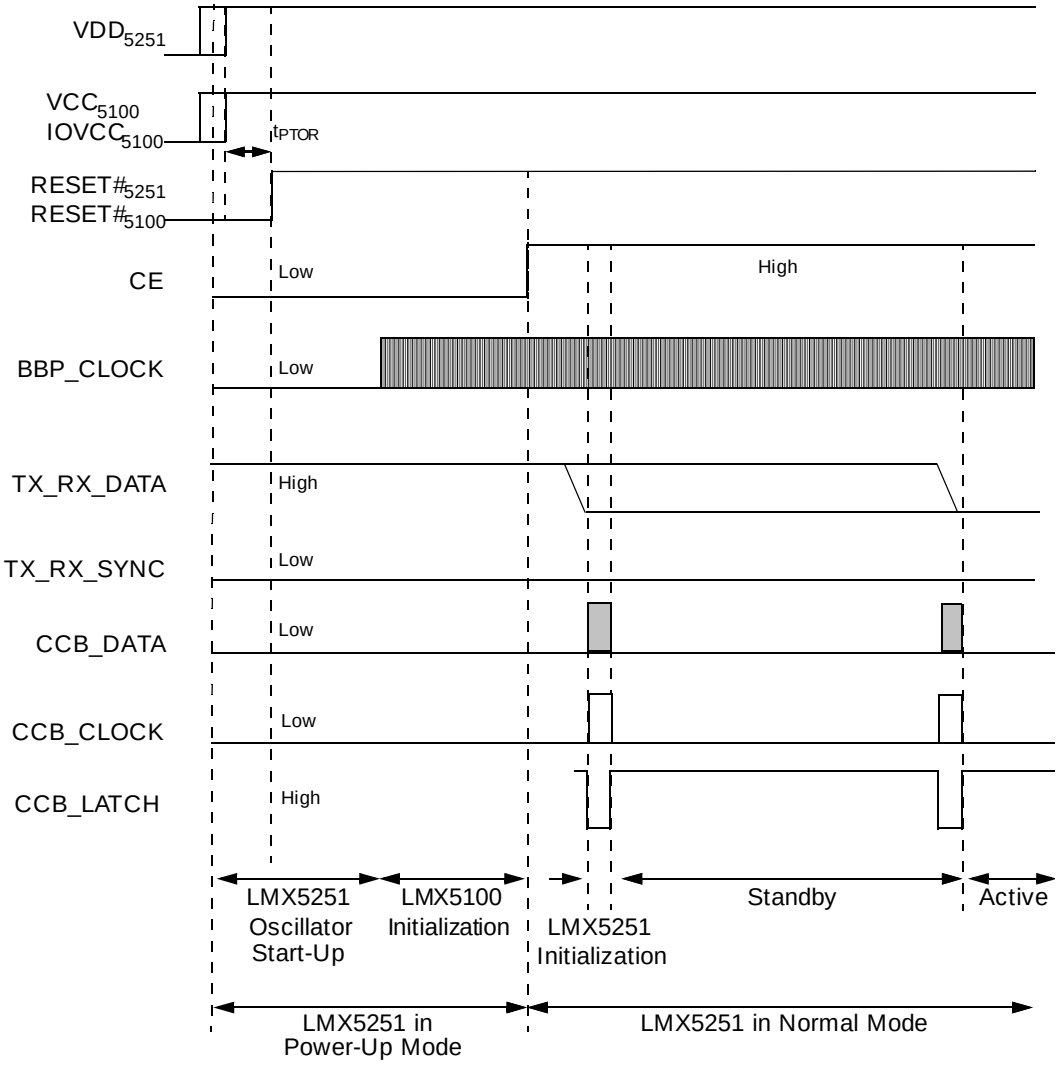


Figure 18. LMX5251/LMX5100 System Power-Up Sequence Timing

LMX5251/LMX5100 System Power-up Sequence Timing

Table 7. LMX5251/LMX5100 System Power-up Sequence Timing

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_{PTOR}	Power to Reset	$VDD_{5251}/VCC_{5100}/IO_{VCC}$ at operating voltage level to valid reset	2			ms

PROGRAMMING DESCRIPTION

The LMX5251 register set can be accessed through the serial interface. The LMX5251 serial interface operates in slave mode to a serial port master contained in a Bluetooth baseband controller such as the baseband controller. A 25-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a Data field, Address field, R/W bit, and Header. The three MSBs of the data loaded into the shift register is the Header 101 (data is programmed MSB first). The Header is immediately followed by the R/W control bit. When R/W = 0, data is clocked into the LMX5251 shift register in the direction from MSB to LSB, when the CCB_CLOCK signal goes high. Shift register bits 20 to 16 are used to decode the internal register address. After the rising edge of the Load Enable (CCB_LATCH) signal, the next rising edge of CCB_CLOCK loads data stored in the shift register into the addressed on-chip register. The serial interface memory map is comprised of four pages for configuring the smart radio functionality. Each page consists of 32 addressable data registers, 16 bits in length. The serial interface format is shown in Table 8.

Write Operation

Serial port write operation timing is shown in Figure 19. When R/W = 0, data is clocked from the base- band controller into the LMX5251 16-bit shift register in the direction from MSB to LSB. The data is shifted out of the baseband controller on the falling edge of CCB_CLOCK, and sampled by the LMX5251 (CCB_DATA) on the rising edge of CCB_CLOCK. When Load Enable (CCB_LATCH) transitions high, data is transferred from the 16-bit shift register into a control register on the rising edge of the next CCB_CLOCK. The data is directed to the appropriate control register depending on the state of the address bits (Address[4:0]), and the active page (Register 0x00, data [11:8]). A multiplexing circuit in the LMX5251 decodes these address bits and writes the data field to the corresponding internal register. In a write operation, the data from the slave (LMX5251) shift register is transferred to the data register on the first clock rising edge after CCB_LATCH goes high.

Read Operation

Serial port read operation timing is shown in Figure 20 on page 26. When R/W = 1, no data field is sent to the LMX5251 from the baseband controller, and the LMX5251 transmits the current value of the addressed register to the baseband controller. Upon receiving the read command (R/W = 1), the LMX5251 takes control of the serial interface data bus. Data is clocked out of the LMX5251 shift register in the direction from MSB to LSB when the CCB_CLOCK signal goes high, and is read into the baseband controller on the falling edge of CCB_CLOCK. When Load Enable (CCB_LATCH) transitions high, the LMX5251 returns control to the baseband controller. The CCB_DATA field assignment for the registers is shown in Table 8. Sixteen bits are always clocked out on a read operation regardless of the register size, with the undefined bits as “don’t care”.

Read Operation Timing

Data is clocked out of the LMX5251 shift register when the CCB_CLOCK signal goes high, and read into the base- band controller on the falling edge of CCB_CLOCK. At 12 MHz a 1/2 clock cycle is 41.7 ns. The steps needed for a read operation are:

1. Baseband controller asserts CCB_CLOCK rising edge.
2. LMX5251 receives CCB_CLOCK rising edge, changes CCB_DATA.
3. LMX5251 asserts new data on CCB_DATA.
4. Baseband controller receives CCB_DATA.
5. Baseband controller asserts CCB_CLOCK falling edge.

Step 4 must occur before step 5. Any additional pad delays also must be taken into account.

Master Slave Data Bus Transfer

Serial port master to slave transfer timing is shown in Figure 21. Upon receiving the read command (R/W = 1), the LMX5251 takes control of the serial interface data bus after the address bits of the register to be read back are received. The baseband controller stops driving CCB_DATA on the falling edge of CCB_CLOCK immediately after the rising edge used by the LMX5251 to clock in the LSB of the address. The LMX5251 then starts driving the data bus at the next rising edge of CCB_CLOCK. The LMX5251 holds the last data value until returning the bus to master control.

Slave to Master Data Bus Return

Serial port master to slave return timing is shown in Figure 22. In a read operation the master requests that the slave stops transmitting data by driving Load Enable (CCB_LATCH) high. When CCB_LATCH transitions high, the LMX5251 releases CCB_DATA at the next rising edge of CCB_CLOCK. The baseband controller takes control of CCB_DATA at the successive falling edge of CCB_CLOCK.

Table 8. Serial Interface Read/Write Register Format

MSB																							LSB
24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header[2:0]			R/W	Address[4:0]					Data[15:0]															

Serial Port Timing Diagrams

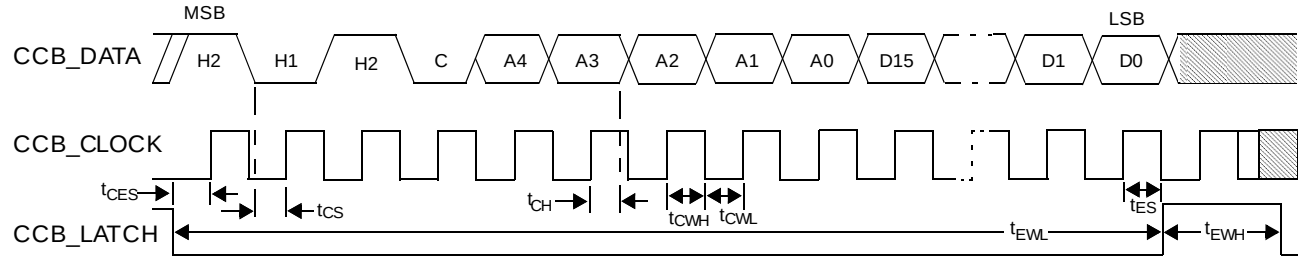


Figure 19. Serial Port Write Timing Diagram

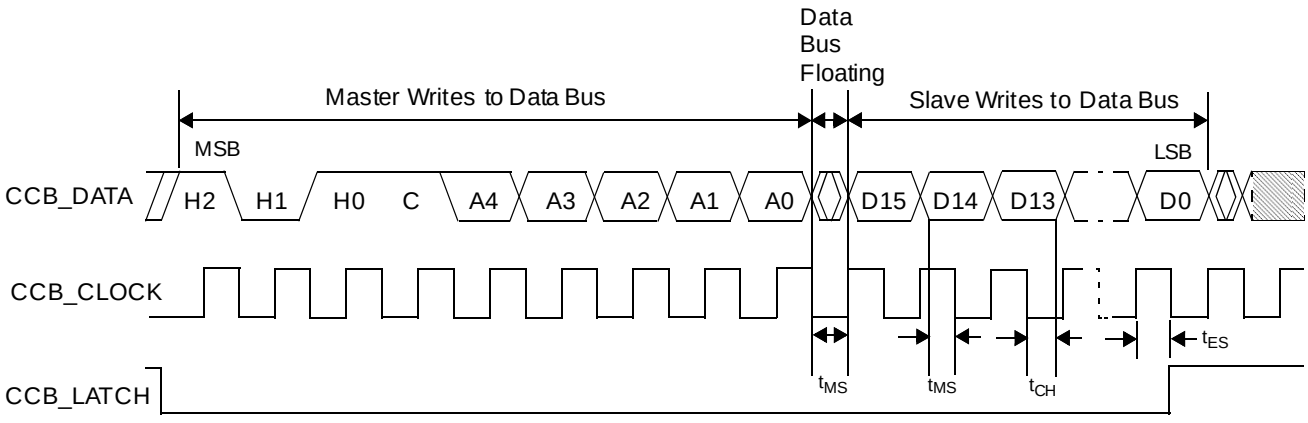


Figure 20. Serial Port Read-Back Timing Diagram

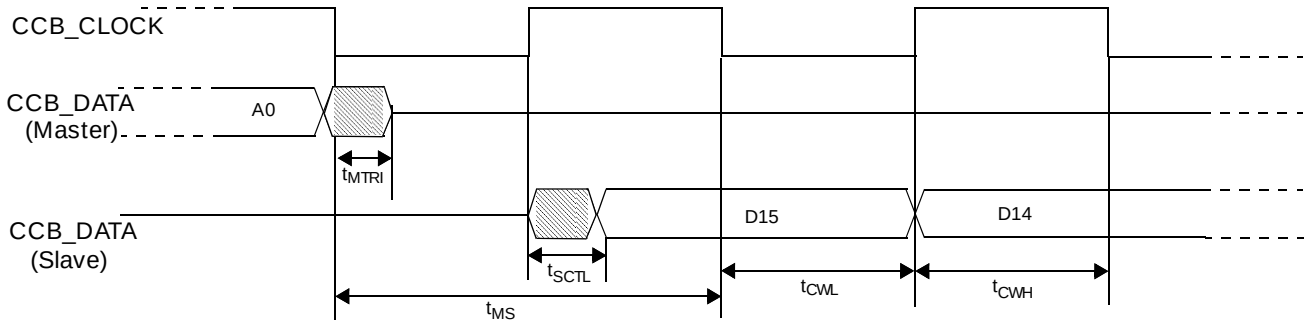


Figure 21. Master to Slave Transfer Timing

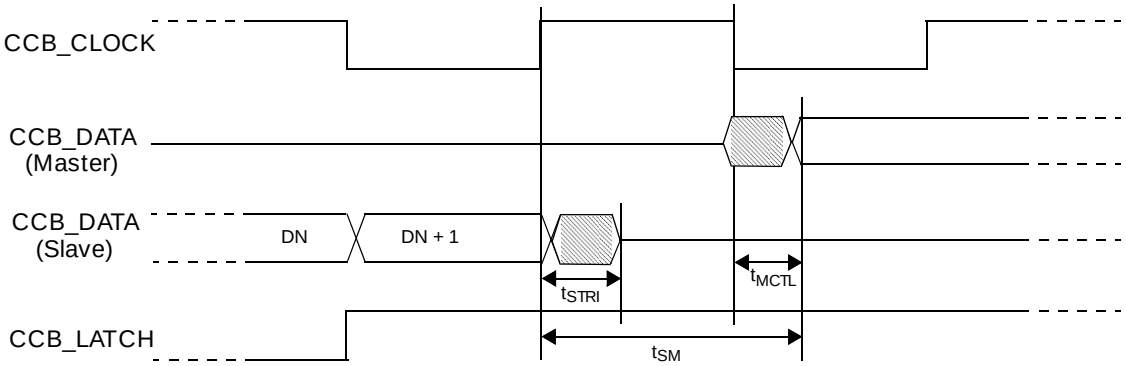
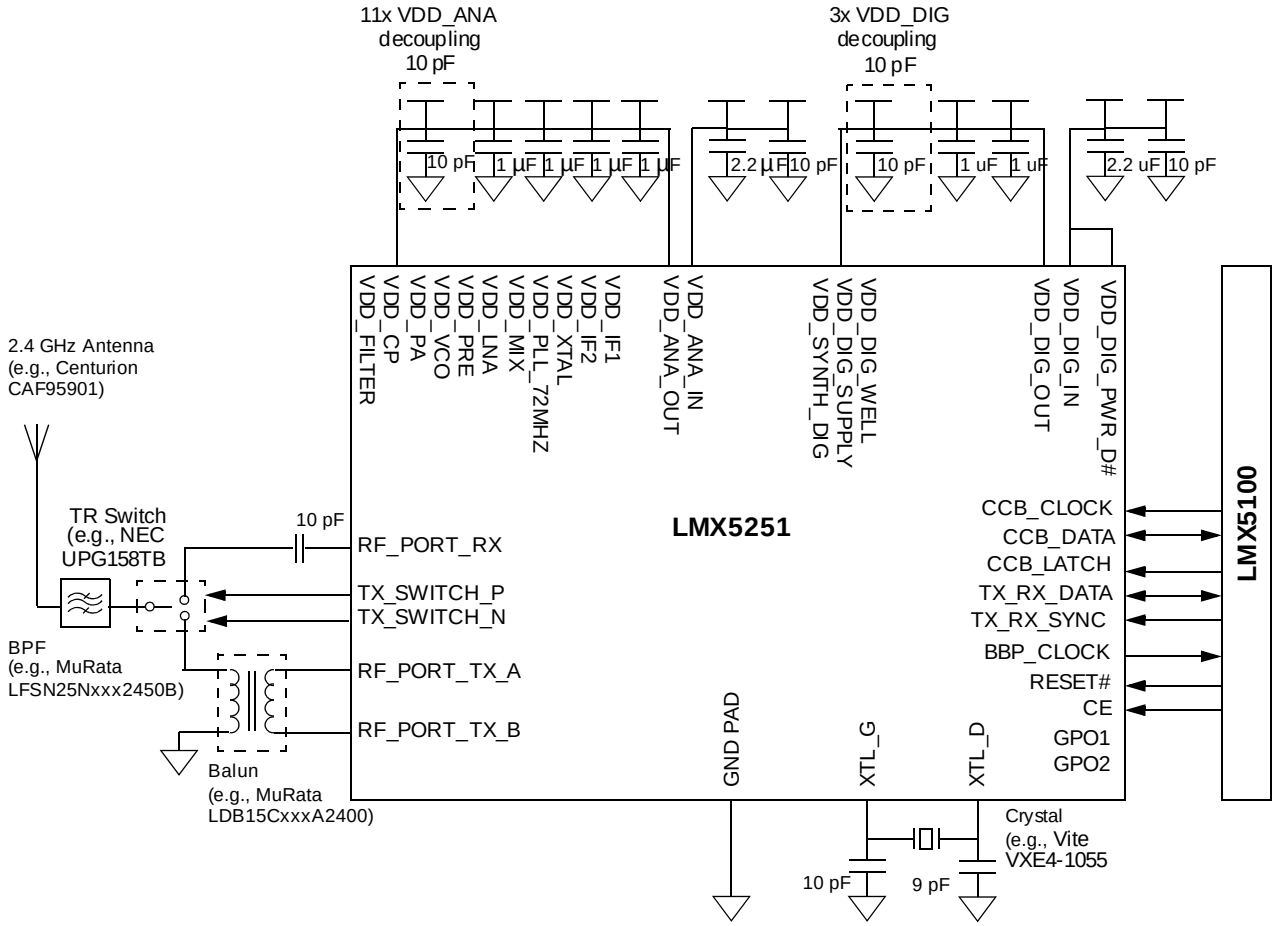


Figure 22. Slave To Master Return Timing

Schematic and Layout Examples

Reference Dallas Board rev 2.0a schematic and layout for details.



NOTE: Tuning capacitors on a crystal can vary depending on design. Refer to the crystal manufacturer's specification to properly tune to board design.

Figure 23. RF Application Diagram

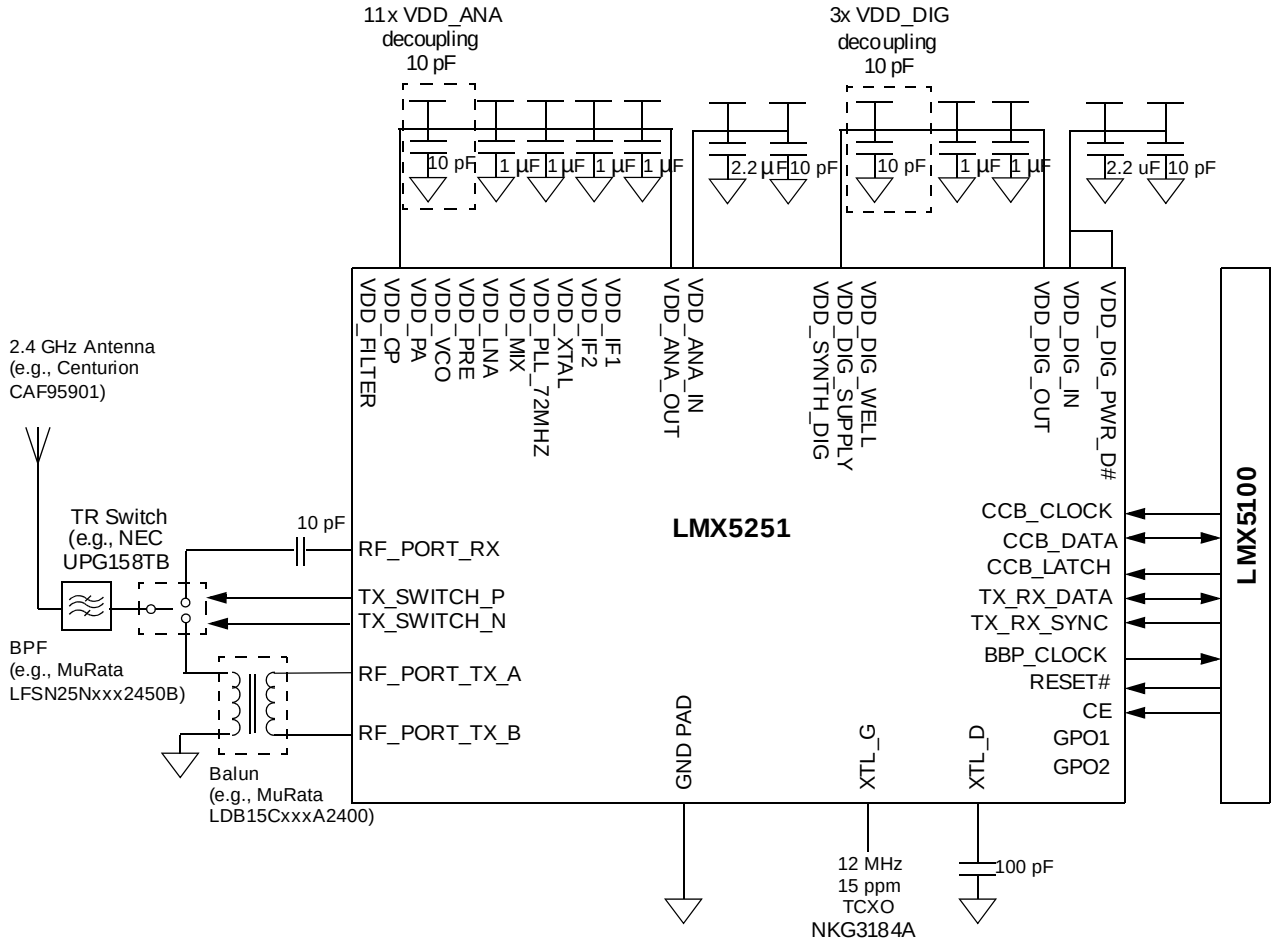


Figure 24. External TCXO

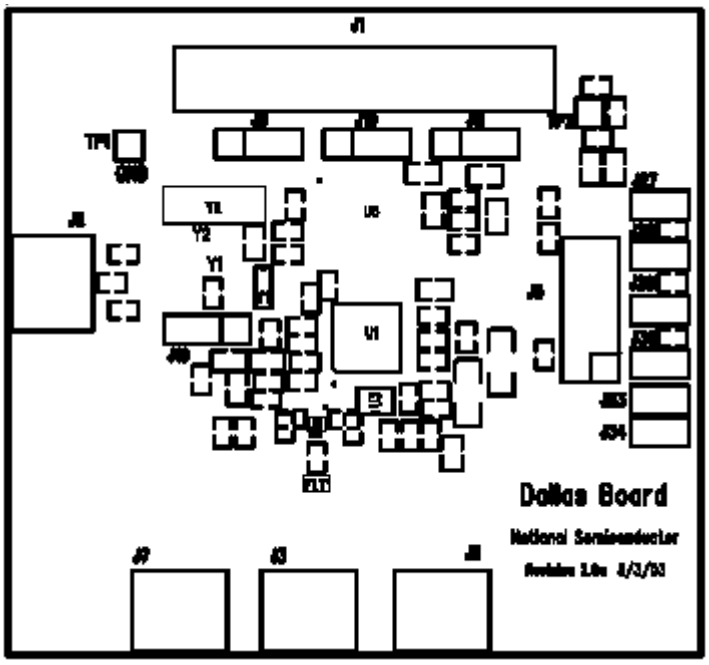
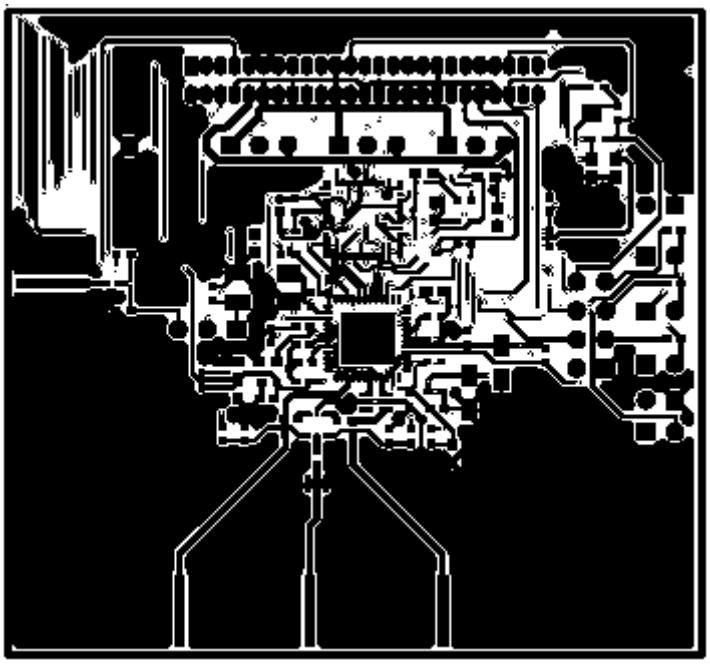
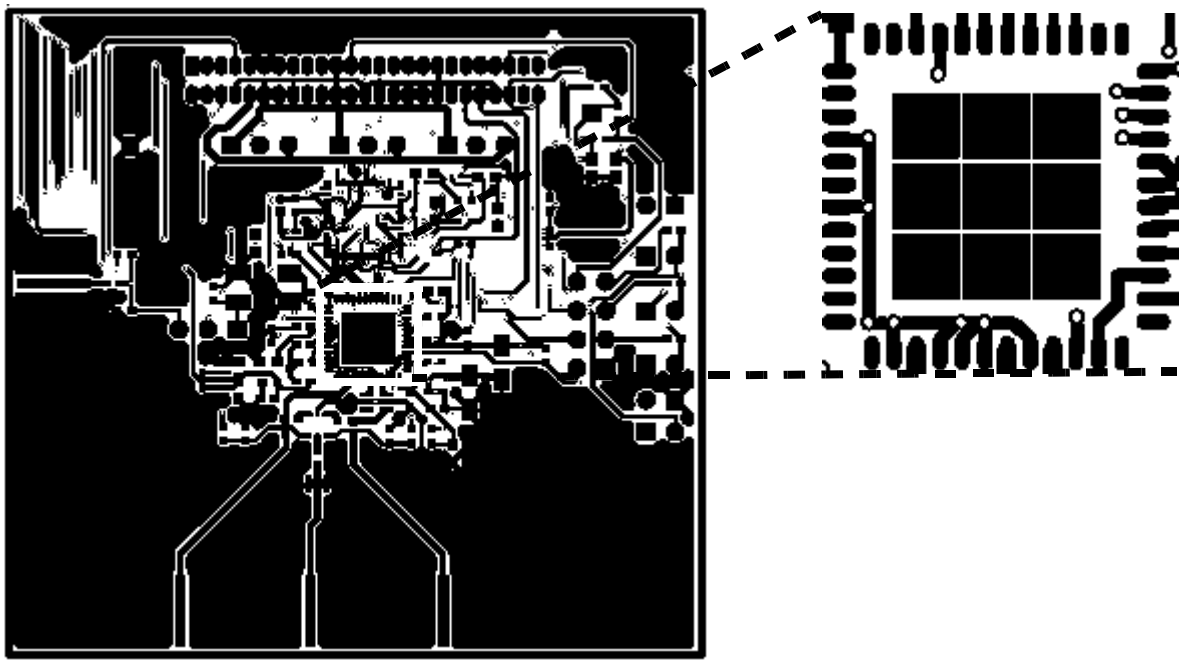


Figure 25. Component Layout Silkscreen - Layer 1



NOTE: Ground pad layout under ground slug of LMX5251 is required. These are connected by vias through all layers to ground plane. No pins on device are ground pins so center slug must be grounded. See detail in Figure 27 "Component Placement - Layer 1 Ground Pad Detail" .

Figure 26. Component Placement - Layer 1



NOTE: Ground pad layout under ground slug of LMX5251 is required. These are connected by vias through all layers to ground plane. No pins on device are ground pins so center slug must be grounded.

Figure 27. Component Placement - Layer 1 Ground Pad Detail

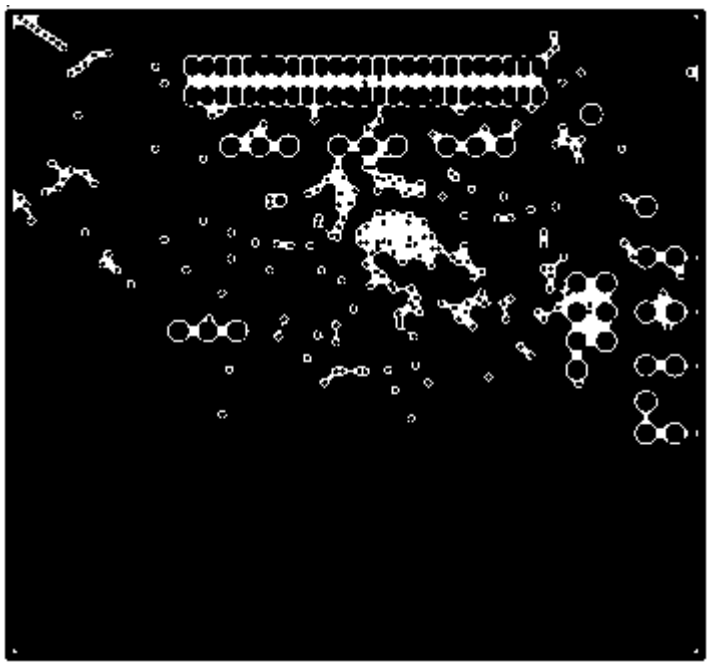


Figure 28. Solid Ground Plane - Layer 2

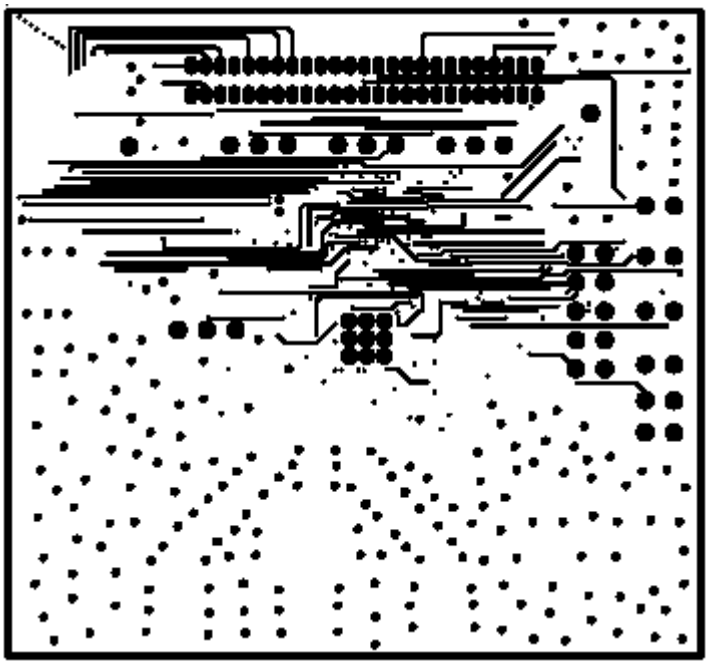


Figure 29. Signal Plane - Layer 3

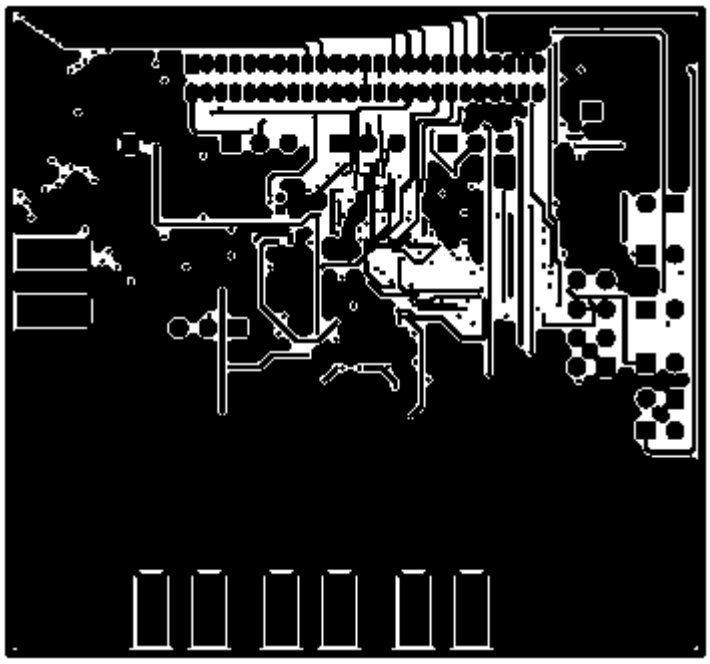


Figure 30. Bottom - Layer 4

REVISION HISTORY

Changes from Original (February 2004) to Revision A **Page**

- Changed - converted this data sheet from National's PDF to Xmetal-DZ, formatted the revisions in the PDF as revision history. original date on this Data Sheet was February 2004, converted to DocZone April 2013 1
- Changed 48-pin QFN bulleted item to 48-pin WQFN (Thin Quad Flatpack No lead) Package 1
- Changed Block diagram graphic and LMX5100/LMX5251 device interface graphic updated. 1
- Deleted the ORDERING INFORMATION table 2
- Changed - Full Temperature performance specified 6
- Changed - 'Several performance parameters updated based on characterization data: 1) Test specification reference and test point references added, 2) Current consumption numbers and low power states., 3) Analog and Digital LDO output voltage range., 4) Receiver and Transmitter performance, typical and worst case value (min or max depending on parameter), added or updated., 5) Synthesizer performance parameters updated.' 6
- Changed Crystal and Oscillator performance updated for V_{OSC} voltage, ESR, Duty Cycle and Phase Noise added. 9
- Added Power Up Sequence section. 25
- Added Schematic and Layout examples 28
- Added Smith charts added for TX/RX pin impedance and TX/RX return loss. 33
- Added External crystal oscillator section updated with tuning details and existing tested crystal specifications. 33
- Added TCXO section with existing tested crystal specification. 33
- Added Detailed RF interface description. 33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX5251SQX/NOPB	ACTIVE	WQFN	RHS	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X5251SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

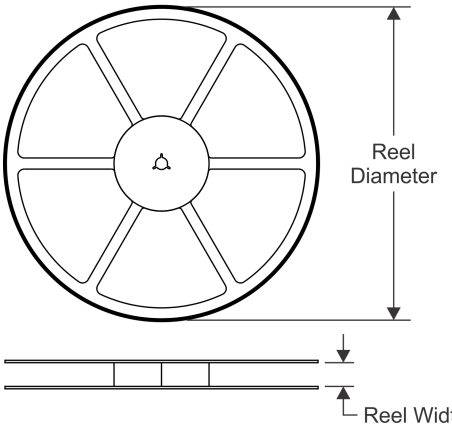
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

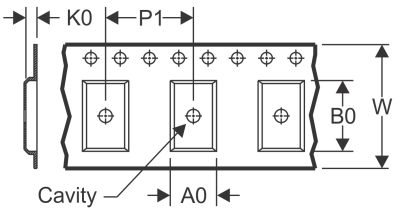
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

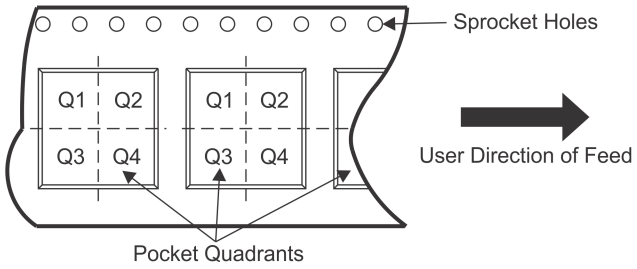


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

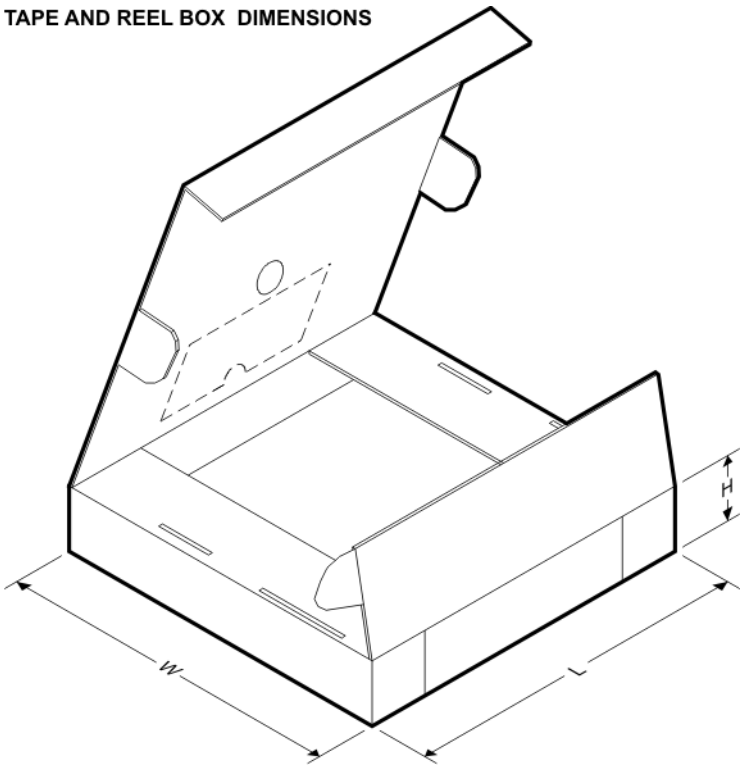
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX5251SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

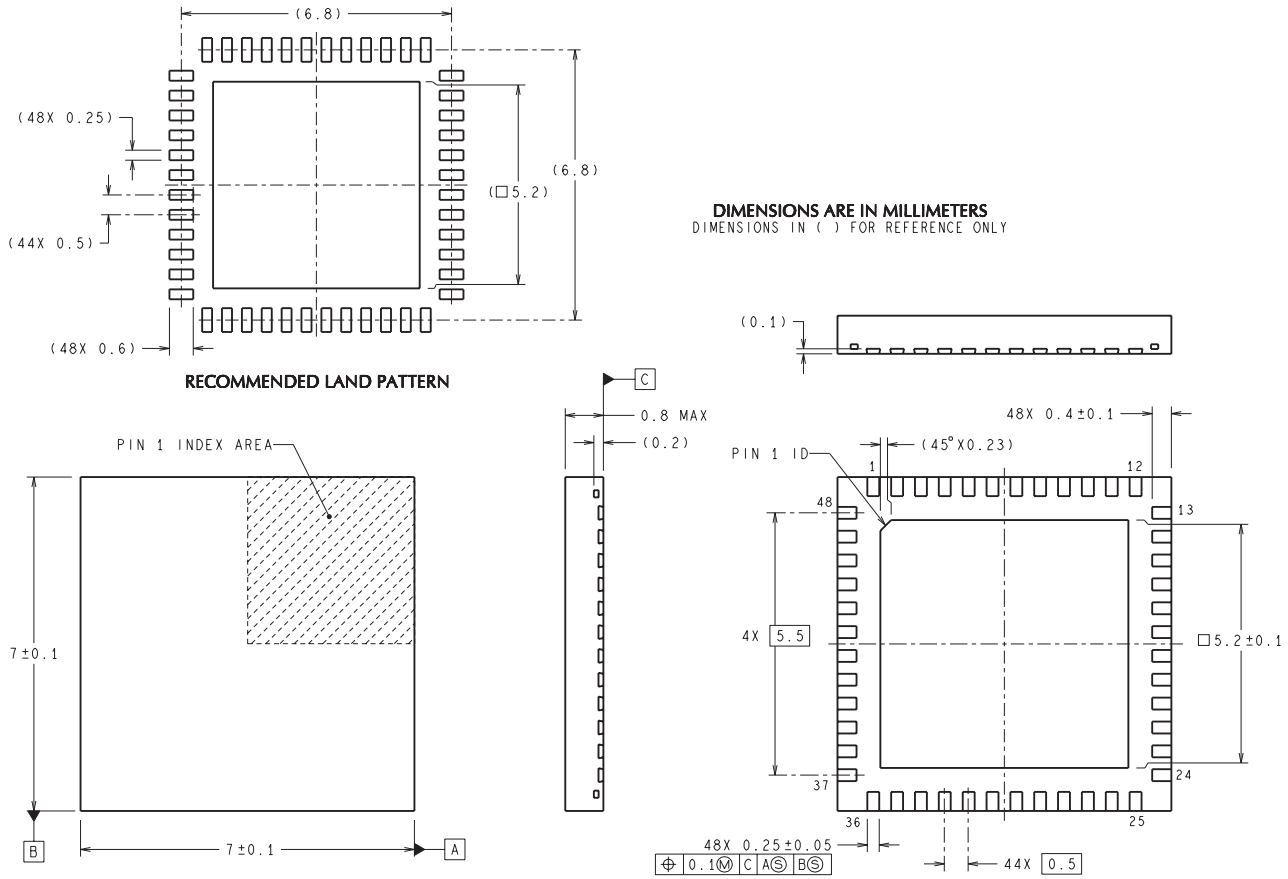
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX5251SQX/NOPB	WQFN	RHS	48	2500	367.0	367.0	38.0

RHS0048B



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