2x16W Stereo Digital Audio Amplifier with Headphone Driver

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 93dB (PSNR), 98dB (DR)
  Headphone: 86dB (PSNR), 96dB (DR)
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz
- System clock = 64x,128x,192x,256x,384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
- Supply voltage
  3.0~12V for loudspeaker driver
  3.0~3.3V for others
- Loudspeaker output power
  2×10W(Full,8Ω) @ 1kHz and 10% THD+N
  2×12.5W(Full,6Ω) @ 1kHz and 10% THD+N
  2×16W(Full,4Ω) @ 1kHz and 10% THD+N
- Headphone power
  34mW into 32Ω@1kHz and 1% THD+N
  65mW into 16Ω@1kHz and 1% THD+N
  110mW into 8Ω@1kHz and 1% THD+N
  200mW into 4Ω@1kHz and 1% THD+N
- Sound processing including：
  Bass (+18dB~-12dB, 3dB frequency is 250Hz),
  Treble (+18dB~-12dB, 3dB frequency is 7kHz),
  5 bands parametric EQ,
  Volume control (+24dB~-103dB, 1dB/step) and Dynamic range control
- Anti-pop design
- Over-temperature protection
- Under-voltage shutdown
- Short-circuit protection
- I^2C control interface

Applications

- CD and DVD
- TV audio
- Car audio
- Boom-box
- MP3 docking systems
- Portable / Handheld
- Powered speaker
- Wireless audio
- USB speaker

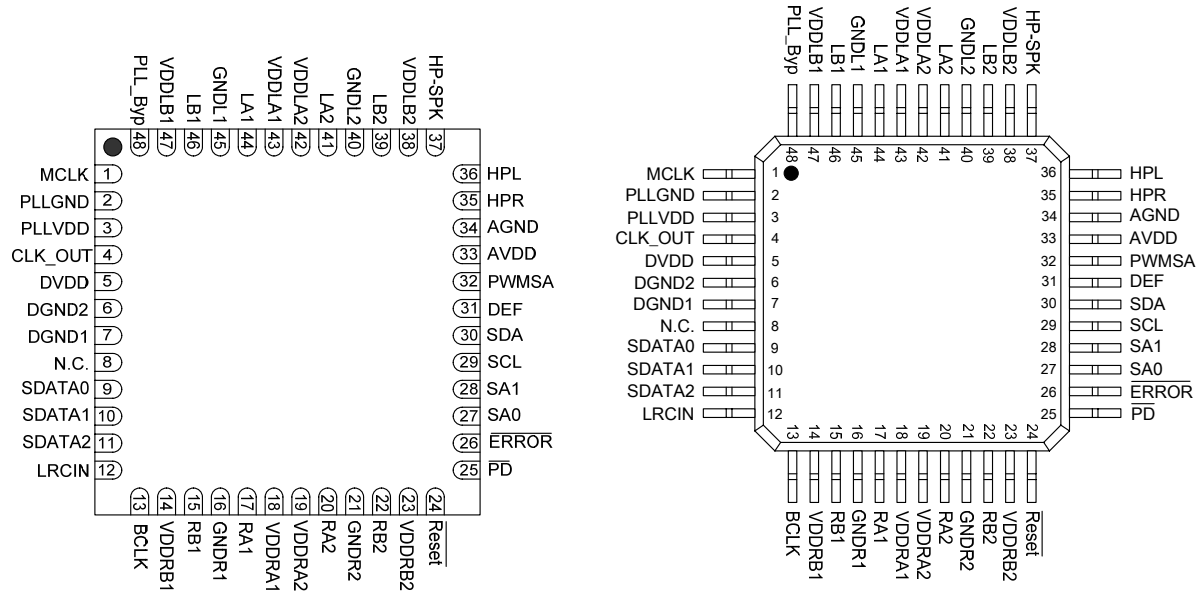
Description

This is a stereo fully digital audio amplifier with output power which can deliver up to 2×16W to 4Ω load with 12V supply voltage. Using I^2C digital control interface, AD8256A provides sound processing functions including Volume, Bass, Treble, EQ, Mixing and Dynamic Range Control (DRC).

ORDERING INFORMATION

Product Number	Package	Comments
AD8256A-KG	7x7 48L QFN	Pb-free
AD8256A-LEG	7x7 48L E-LQFP	Pb-free

Pin Assignment



Pin Description

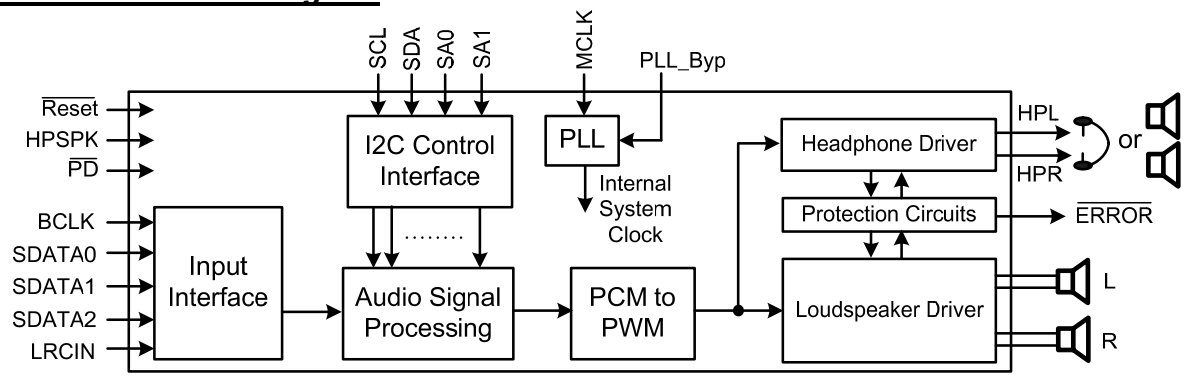
PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
2	PLLGND	P	Ground for PLL	
3	PLLVDD	P	Supply for PLL	(Note1)
4	CLK_OUT	O	PLL output	TTL output buffer
5	DVDD	P	Digital Power	(Note1)
6	DGND2	P	Digital Ground2	
7	DGND1	P	Digital Ground1	
8	N.C.		No Connection	
9	SDATA0	I	Serial audio data input 0	Schmitt trigger TTL input buffer
10	SDATA1	I	Serial audio data input 1	Schmitt trigger TTL input buffer
11	SDATA2	I	Serial audio data input 2	Schmitt trigger TTL input buffer
12	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
13	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
14	VDDRB1	P	Supply1 for right channel B	(Note2)
15	RB1	O	Right channel output1 (-)	
16	GNDR1	P	Ground1 for right channel	
17	RA1	O	Right channel output1 (+)	
18	VDDRA1	P	Supply1 for right channel A	(Note2)
19	VDDRA2	P	Supply2 for right channel A	(Note2)

20	RA2	O	Right channel output2 (+)	
21	GNDR2	P	Ground2 for right channel	
22	RB2	O	Right channel output2 (-)	
23	VDDRB2	P	Supply2 for right channel B	(Note2)
24	$\overline{\text{Reset}}$	I	Reset, low active	Schmitt trigger TTL input buffer
25	$\overline{\text{PD}}$	I	Power down, low active	Schmitt trigger TTL input buffer
26	$\overline{\text{ERROR}}$	O	ERROR output	Open-drain output
27	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
28	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
29	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
30	SDA	I	I^2C serial data input	Schmitt trigger TTL input buffer with open-drain output
31	DEF	I	Default volume, 0=Mute, 1=Un-Mute	Schmitt trigger TTL input buffer
32	PWMSA	O	Half-bridge, sub-woofer channel output	TTL output buffer
33	AVDD	P	Analog supply	(Note1)
34	AGND	P	Analog ground	
35	HPR	O	Headphone right channel output	
36	HPL	O	Headphone left channel output	
37	HP-SPK	I	Headphone detection	
38	VDDLB2	P	Supply2 for left channel B	(Note2)
39	LB2	O	Left channel output2 (-)	
40	GNDL2	P	Ground2 for left channel	
41	LA2	O	Left channel output2 (+)	
42	VDDLA2	P	Supply2 for left channel A	(Note2)
43	VDDLA1	P	Supply1 for left channel A	(Note2)
44	LA1	O	Left channel output1 (+)	
45	GNDL1	P	Ground1 for left channel	
46	LB1	O	Left channel output1 (-)	
47	VDDLB1	P	Supply1 for left channel B	(Note2)
48	PLL_Byp	I	PLL Bypass	Schmitt trigger TTL input buffer

Note1：These pins provide the supply for digital PWM controller, headphone drivers, built-in PLL and protection circuits except for loudspeaker short-circuit protection circuits.

Note2：These pins provide the supply for loudspeaker driver stages, which are known as “PVDD”.

Functional Block Diagram



Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jc}(℃/W)	Exposed Thermal Pad
7x7 48L QFN	AD8256A	23.5	1.6	12.5	Yes (Note3)
7x7 48L E-LQFP		23.8	1.8	15.8	

Note3：The thermal pad is at the bottom of package. To optimize the performance of thermal dissipation, solder the thermal pad to PCB's ground plane is suggested.