rev 0.3

# 18 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs

## Features

- One input to 18 output Buffer/Driver
- Supports up to four SDRAM DIMMs
- Two additional outputs for feedback
- Serial interface for individual output control
- Low skew outputs (< 250 pS)
- Up to 133 MHz operation
- Dedicated OE pin for testing
- Space-saving 48 Pin SSOP package
- 3.3V operation

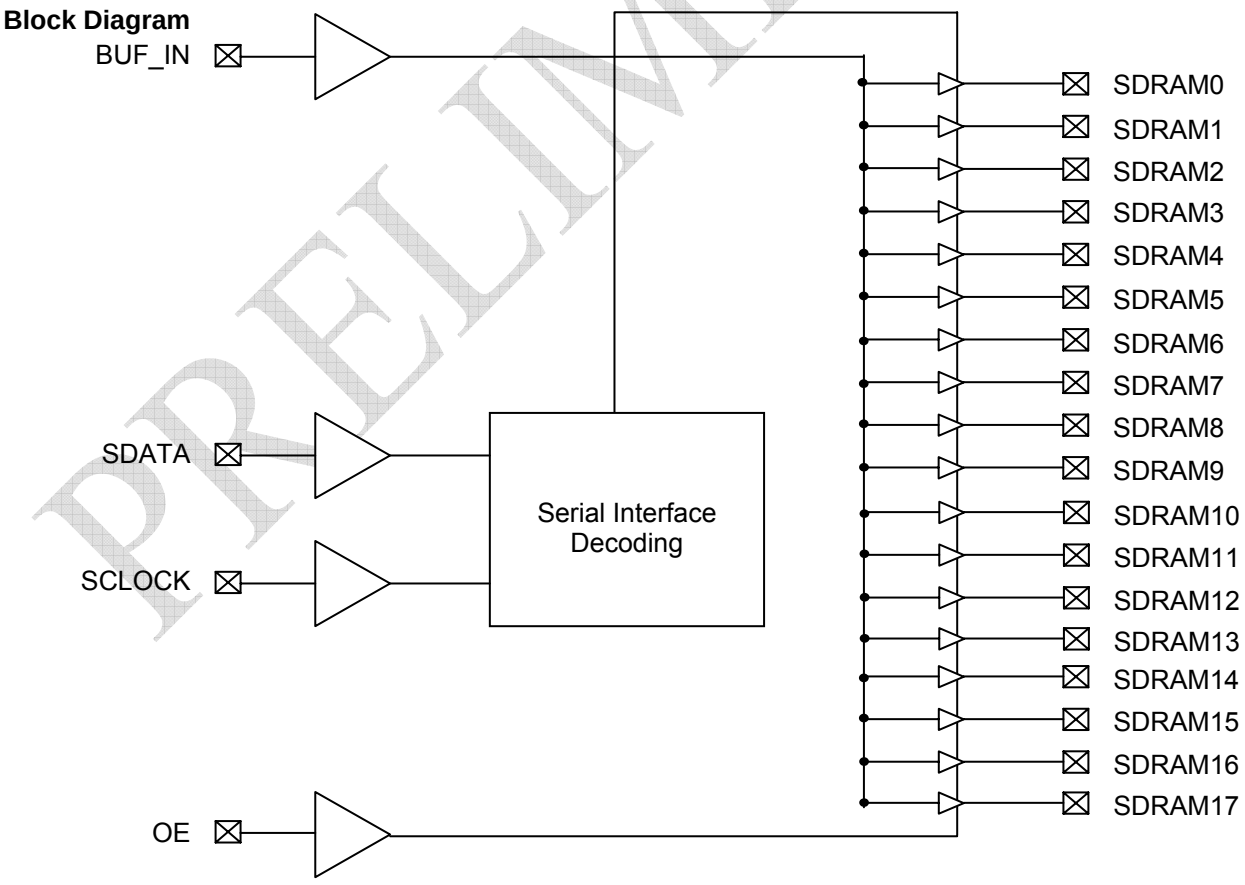
## Functional Description

The ASM2I2318ANZ is a 3.3V buffer designed to distribute high-speed clocks in PC applications. The part has 18 outputs, 16 of which can be used to drive up to four SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133MHz, thus making it compatible with Pentium II®* processors. The ASM2I2318ANZ can be used in conjunction with the clock synthesizer for a complete Pentium II motherboard solution. The ASM2I2318ANZ also includes a serial interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up). A separate Output Enable pin facilitates testing on ATE.

*Pentium is a registered trademark of Intel Corporation.

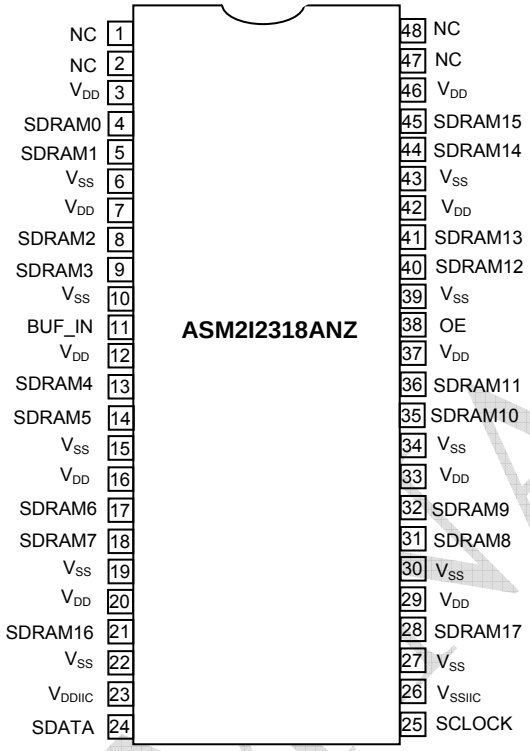


## Block Diagram



## Pin Configuration

**48-Pin SSOP Package -- Top View**




## Pin Description

| Pins | Name | Type | Description |
|---|---|---|---|
| 3, 7, 12, 16, 20, 29, 33, 37, 42, 46 | $V_{DD}$ | P | 3.3V Digital voltage supply |
| 6, 10, 15, 19, 22, 27, 30, 34, 39, 43 | $V_{SS}$ | P | Ground |
| 23 | $V_{DDIIC}$ | P | Serial interface voltage supply |
| 26 | $V_{SSIIC}$ | P | Ground for serial interface |
| 11 | BUF_IN | I | Input clock. 5V tolerant |
| 38 | OE | I | Output Enable (active HIGH), Three-state outputs when low[1] |
| 24 | SDATA | I/O | Serial data input[1]. 5V tolerant |
| 25 | SCLK | I | Serial clock input[1]. 5V tolerant |
| 4, 5, 8, 9 | SDRAM [0–3] | O | SDRAM byte 0 clock outputs |
| 13, 14, 17, 18 | SDRAM [4–7] | O | SDRAM byte 1 clock outputs |
| 31, 32, 35, 36 | SDRAM [8–11] | O | SDRAM byte 2 clock outputs |
| 40, 41, 44, 45 | SDRAM [12–15] | O | SDRAM byte 3 clock outputs |
| 21, 28 | SDRAM [16–17] | O | SDRAM clock outputs usable for feedback |
| NC | 1, 2, 47, 48 | - | Reserved for future modifications, do not connect in system |

Note: 1. Internal pull-up resistor to $V_{DD}$ (value > 100 KOhms)

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### Device Functionality

| OE | SDRAM [0-17] |
|---|---|
| 0 | Hi-Z |
| 1 | 1 x BUF_IN |

### Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved bits should be programmed to “0” or ”1”.
- Serial interface address for the ASM2I2318ANZ is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | ---- |

### Byte 0:SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enable

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 18 | SDRAM7 (Active/Inactive) |
| Bit 6 | 17 | SDRAM6 (Active/Inactive) |
| Bit 5 | 14 | SDRAM5 (Active/Inactive) |
| Bit 4 | 13 | SDRAM4 (Active/Inactive) |
| Bit 3 | 9 | SDRAM3 (Active/Inactive) |
| Bit 2 | 8 | SDRAM2 (Active/Inactive) |
| Bit 1 | 5 | SDRAM1 (Active/Inactive) |
| Bit 0 | 4 | SDRAM0 (Active/Inactive) |

### Byte 1: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enable

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 45 | SDRAM15 (Active/Inactive) |
| Bit 6 | 44 | SDRAM14 (Active/Inactive) |
| Bit 5 | 41 | SDRAM13 (Active/Inactive) |
| Bit 4 | 40 | SDRAM12 (Active/Inactive) |
| Bit 3 | 36 | SDRAM11 (Active/Inactive) |
| Bit 2 | 35 | SDRAM10 (Active/Inactive) |
| Bit 1 | 32 | SDRAM9 (Active/Inactive) |
| Bit 0 | 31 | SDRAM8 (Active/Inactive) |

### Byte 2: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enable

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 28 | SDRAM17 (Active/Inactive) |
| Bit 6 | 21 | SDRAM16 (Active/Inactive) |
| Bit 5 | -- | Reserved |
| Bit 4 | -- | Reserved |
| Bit 3 | -- | Reserved |
| Bit 2 | -- | Reserved |
| Bit 1 | -- | Reserved |
| Bit 0 | -- | Reserved |

Note 1 : When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

### IIC Byte Flow

| Byte | Description |
|---|---|
| 1 | IIC Address |
| 2 | Command (dummy value, ignored) |
| 3 | Byte Count (dummy value, ignored) |
| 4 | IIC Data Byte 0 |
| 5 | IIC Data Byte 1 |
| 6 | IIC Data Byte 2 |

### Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage to Ground Potential | –0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Except BUF_IN) | –0.5 to $V_{DD}$ + 0.5 | V |
| $V_{BUFIN}$ | DC Input Voltage (BUF_IN) | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_J$ | Junction Temperature | 150 | °C |
| $T_{DV}$ | Static Discharge Voltage (As per JEDEC STD 22- A114-B) | 2 | KV |

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

### Operating Conditions[1]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ $V_{DDIIC}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_L$ | Load Capacitance | 20 | 30 | pF |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all $V_{DD}$'s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | mS |

Note: 1. Electrical parameters are guaranteed under the operating conditions specified.

## Electrical Characteristics

(Test condition: All parameters values are valid within the Operating range, unless otherwise stated)

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | For all pins except serial interface pins | | | 0.8 | V |
| $V_{ILiic}$ | Input LOW Voltage | For serial pins only | | | 0.7 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{OL}$ | Output LOW Voltage[1] | $I_{OL}$= 25 mA | | | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage[1] | $I_{OH}$ = –36 mA | 2.4 | | | V |
| $I_{CC}$ | Quiescent Supply Current | $V_{DD}$= 3.465V, $V_i$ = $V_{DD}$ or GND, $I_O$ =0 | | 50 | 100 | µA |
| $I_{OZ}$ | High Impedance Output Current | $V_{DD}$= 3.465V, $V_i$ = $V_{DD}$ or GND | | | ±10 | µA |
| $I_{OFF}$ | Off-State Current (for SCL ,SDATA) | $V_{DD}$= 0V, $V_i$ = 0V or 5.5V | | | 50 | µA |
| $\Delta I_{CC}$ | Change in Supply Current | $V_{DD}$= 3.135V to 3.465V One Input at $V_{DD}$-0.6, All other Inputs at $V_{DD}$ or GND | | | 500 | µA |
| $I_i$ | Input Leakage | $V_{DD}$= 3.465V or GND (Applicable to all Input Pins) | -5 | | +5 | µA |
| $I_{DD}$ | Supply Current[1] | Unloaded outputs, 133 MHz | | | 150 | mA |
| $I_{DD}$ | Supply Current[1] | Loaded outputs, 30pF,133 MHz | | | 400 | mA |
| $I_{DD}$ | Supply Current[1] | Unloaded outputs, 100 MHz | | | 110 | mA |
| $I_{DD}$ | Supply Current[1] | Loaded outputs, 30pF, 100 MHz | | | 300 | mA |
| $I_{DD}$ | Supply Current[1] | Unloaded outputs, 66.67 MHz | | | 80 | mA |
| $I_{DD}$ | Supply Current[1] | Loaded outputs, 30pF, 66.67 MHz | | | 200 | mA |
| $I_{DDS}$ | Supply Current | BUF_IN=$V_{DD}$ or $V_{SS}$, all other inputs at $V_{DD}$ | | | 500 | µA |

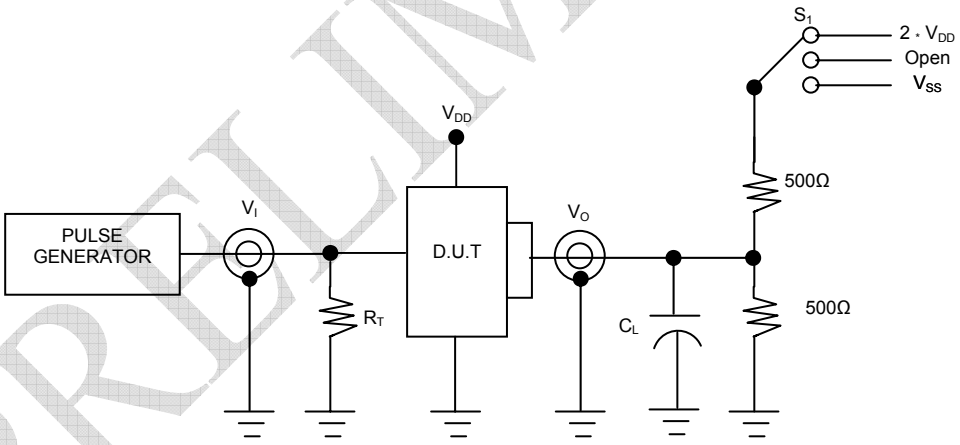
Note: 1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics[1]

| Parameter | Name | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{in}$ | Maximum Operating Frequency | | - | - | 133 | MHz |
| $t_D$ | Duty cycle [2,3] = $t_2 \div t_1$ | Measured at 1.5V | 45.0 | 50.0 | 55.0 | % |
| $t_3$ | Rising Edge Rate[3] | Measured between 0.4V and 2.4V | 1 | 2 | 4 | V/nS |
| $t_4$ | Falling Edge Rate[3] | Measured between 2.4V and 0.4V | 1 | 2 | 4 | V/nS |
| $t_5$ | Output to Output Skew[3] | All outputs equally loaded | | 150 | 225 | pS |
| $t_6$ | SDRAM Buffer LH Prop. Delay[3] | Input edge greater than 1 V/nS | 1 | 2.7 | 3.5 | nS |
| $t_7$ | SDRAM Buffer HL Prop. Delay[3] | Input edge greater than 1 V/nS | 1 | 2.7 | 3.5 | nS |
| $t_{PLZ}$, $t_{PHZ}$ | SDRAM Buffer Enable Delay[3] | Input edge greater than 1 V/nS | 1 | 3 | 5 | nS |
| $t_{PZL}$, $t_{PZH}$ | SDRAM Buffer Disable Delay[3] | Input edge greater than 1 V/nS | 1 | 3 | 5 | nS |
| $t_r$ | Rise Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3 | $C_L$ = 10pF | 6 | | | nS |
| | | $C_L$ = 400pF | | | 250 | |
| $t_f$ | Fall Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3 | $C_L$ = 10pF | 20 | | | nS |
| | | $C_L$ = 400pF | | | 250 | |

Note: 1. All parameters specified with loaded outputs.
2. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/nS
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Test Circuit for SDRAM Enable and Disable Times




| TEST | $S_1$ |
|---|---|
| $t_6/t_7$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2· $V_{DD}$<br>$V_{SS}$ |

**Figure 1. Load circuit for Switching times**

### SDRAM Enable and Disable Times

$V_M$ = 1.5V
$V_X$ = $V_{OL}$ +0.3V
$V_Y$ = $V_{OH}$ -0.3V
$V_{OH}$ and $V_{OL}$ are the typical Output Voltage drop that occur with the output load

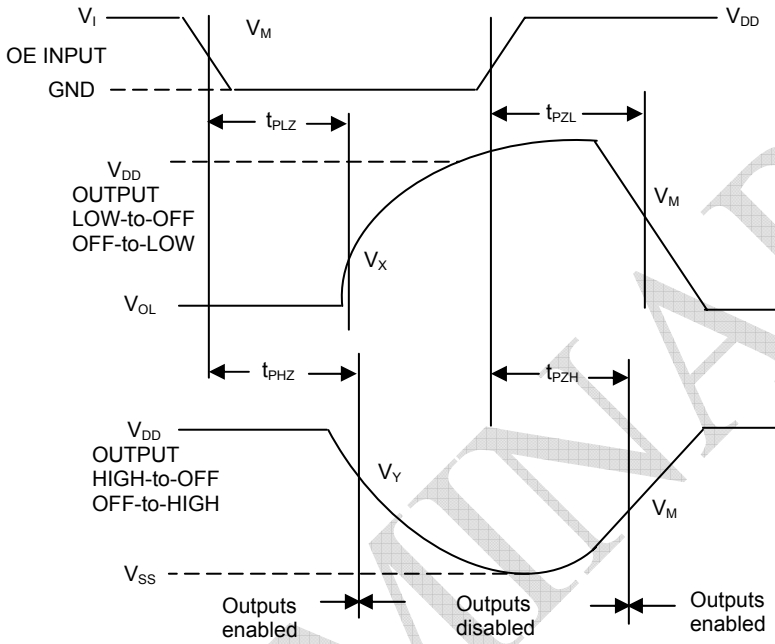



**Figure 2. 3-State Enable and Disable times**

### Test Circuit for IIC Rise and Fall Times

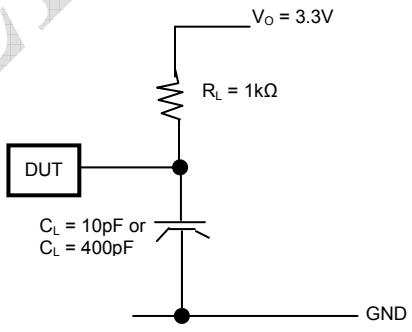
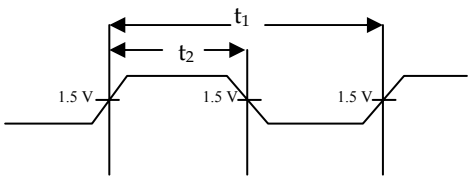


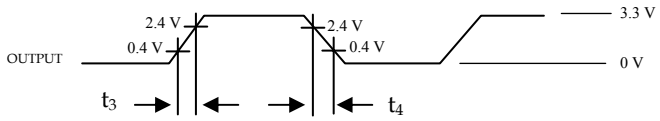

**Figure 3. Test Circuit for IIC**

## Switching Waveforms

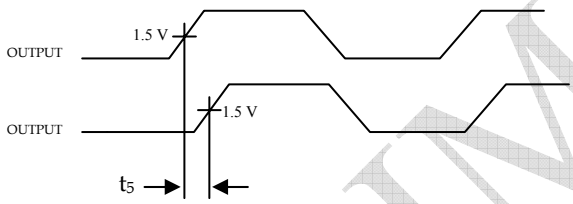
### Duty Cycle Timing



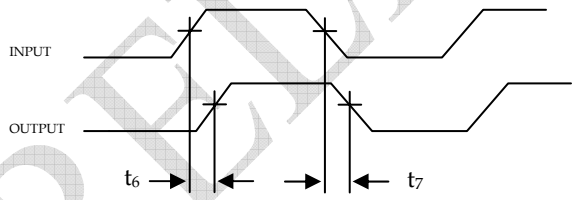

### All Outputs Rise/Fall Time



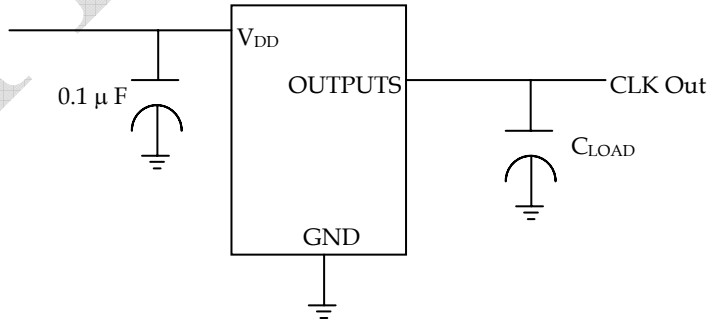

### Output - Output Skew




### SDRAM Buffer LH and HL Propagation Delay




### Test Circuit



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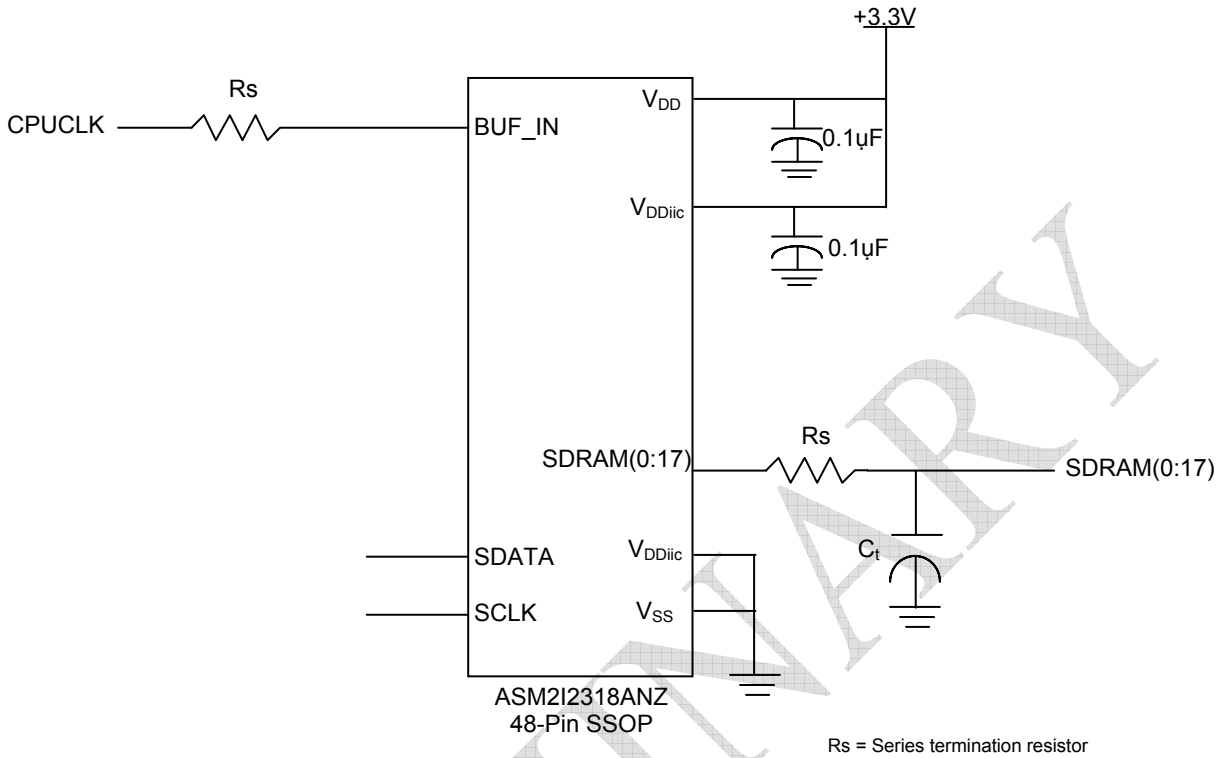
## Application Circuit




## Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25Ω), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7pF to 22pF.
- A Ferrite Bead may be used to isolate the Board $V_{DD}$ from the clock generator $V_{DD}$ island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a 10µF–22µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

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### IIC Serial Interface Information

The information in this section assumes familiarity with IIC programming.

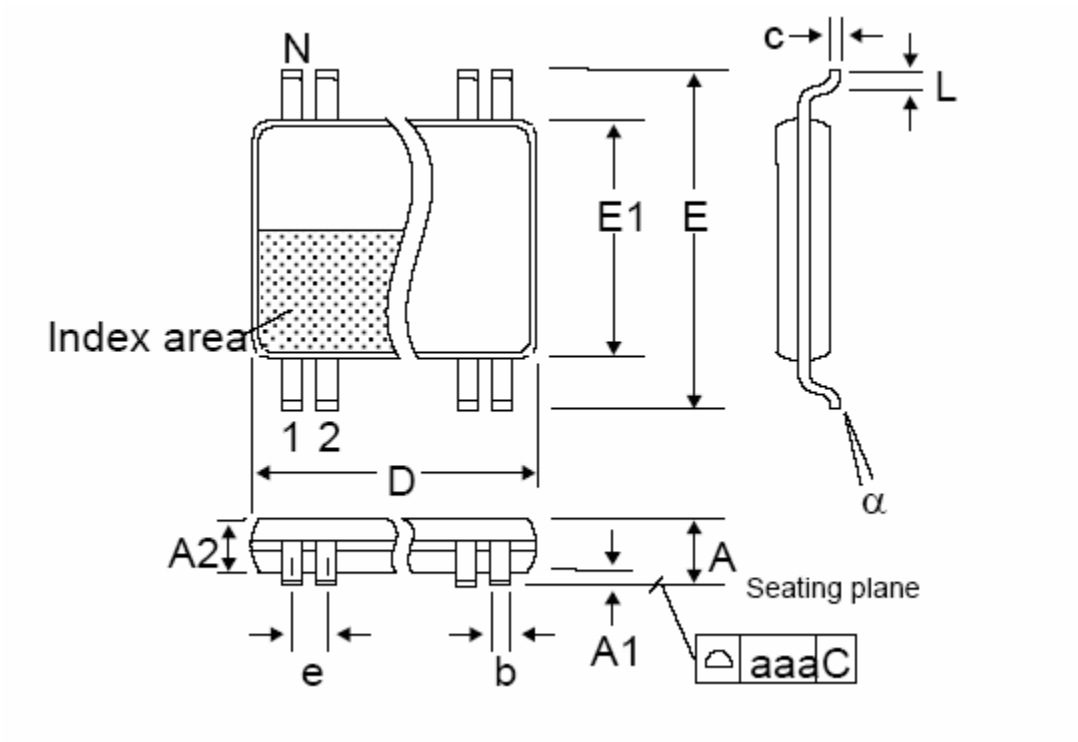
### How to program ASM2I2318ANZ through IIC:

- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- ASM2I2318ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- ASM2I2318ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count
- ASM2I2318ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0
- ASM2I2318ANZ device will acknowledge Byte 0
- Master (host) sends the Byte 1
- ASM2I2318ANZ device will acknowledge Byte 1
- Master (host) sends the Byte 2
- ASM2I2318ANZ device will acknowledge Byte 2
- Master (host) sends a Stop bit.

| Controller (Host) | ASM2I2318ANZ (slave/receiver) |
|---|---|
| Start Bit | |
| Slave Address D3(H) | |
| | ACK |
| Command Byte | |
| | ACK |
| Byte count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Stop Bit | |

**Package Information**

**48L SSOP Package (300 mil)**




| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | 0.095 | 0.110 | 2.413 | 2.794 |
| A1 | 0.008 | 0.016 | 0.203 | 0.406 |
| B | 0.008 | 0.012 | 0.203 | 0.305 |
| C | 0.005 | 0.009 | 0.127 | 0.228 |
| D | 0.620 | 0.630 | 15.75 | 16.002 |
| E | 0.291 | 0.299 | 7.39 | 7.59 |
| H | 0.395 | 0.420 | 10.033 | 10.67 |
| L | 0.020 | 0.040 | 0.508 | 1.016 |
| e | 0.025 BSC | | 0.635 BSC | |
| α | 0° | 8° | 0° | 8° |

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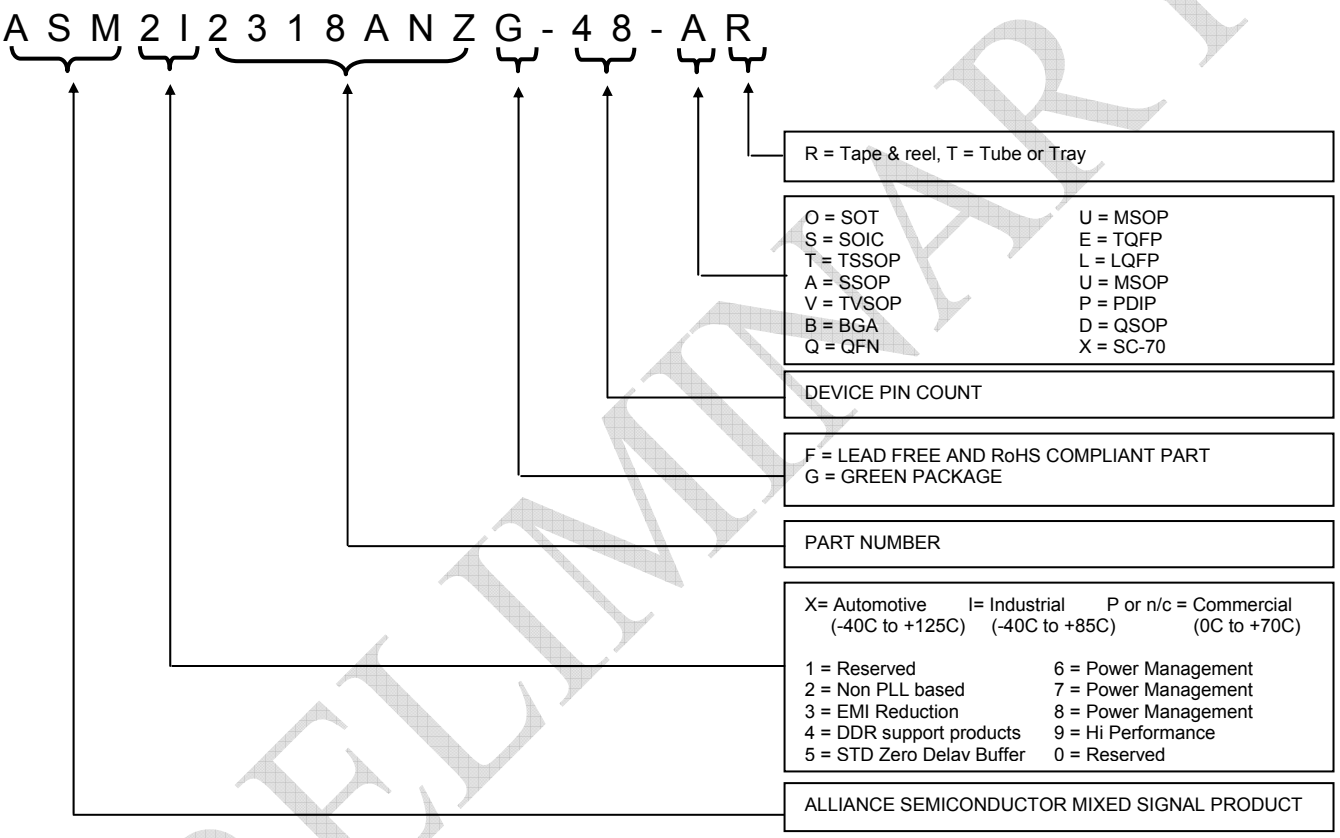
## Ordering Information

| Ordering Code | Marking | Package Type | Operating Range |
|---|---|---|---|
| ASM2I2318ANZ-48-AT | 2I2318ANZ | 48 Pin SSOP, Tube | Industrial |
| ASM2I2318ANZ-48-AR | 2I2318ANZ | 48 Pin SSOP, Tape and Reel | Industrial |
| ASM2I2318AGNZ-48-AT | 2I2318AGNZ | 48 Pin SSOP, Tube, Green | Industrial |
| ASM2I2318AGNZ-48-AR | 2I2318AGNZ | 48 Pin SSOP, Tape and Reel, Green | Industrial |

## Device Ordering Information



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Part Number: ASM2I2318ANZ
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003