



DRAM

1 MEG x 16 DRAM

3.3V, EDO PAGE MODE,
OPTIONAL EXTENDED REFRESH

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD 883
- SMD Planned

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR), HIDDEN
- BYTE WRITE access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 180mW active, typical
- Extended Data-Out (EDO) PAGE access cycle
- 5V-tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS

- Timing
 - 60ns access (Contact Factory)
 - 70ns access
 - 80ns access

MARKING

- 6
- 7
- 8

- Refresh Rate
 - Standard 16ms period

None

- Packages

Ceramic SOJ	ECJ	No. 506
Ceramic Gull Wing	ECG	No. 604
Ceramic LCC	EC	No. 213

KEY TIMING PARAMETERS

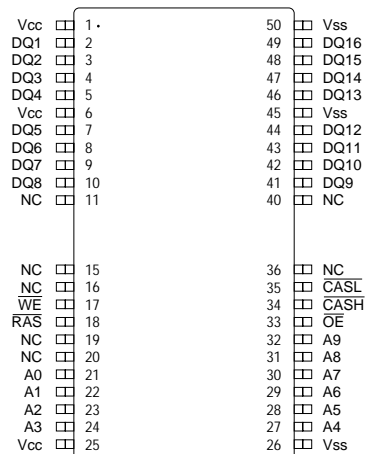
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns
-8	150ns	80ns	40ns	40ns	20ns	20ns

GENERAL DESCRIPTION

The AS4LC1M16 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The AS4LC1M16 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins ($\overline{\text{CASL}}$ and $\overline{\text{CASH}}$). These function in a similar manner to a single $\overline{\text{CAS}}$ of other DRAMs in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate

PIN ASSIGNMENT (Top View)

44/50-Pin SOJ/LCC/Gull Wing
450mil



an internal $\overline{\text{CAS}}$.

The AS4LC1M16 $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and the last $\overline{\text{CAS}}$ to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. The $\overline{\text{CAS}}$ function also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{\text{RAS}}$ goes LOW.



GENERAL DESCRIPTION (continued)

The CASL and CASH inputs internally generate a \overline{CAS} signal functioning in a similar manner to the single \overline{CAS} input of other DRAMs. The key difference is each \overline{CAS} input (\overline{CASL} and \overline{CASH}) controls its corresponding 8 DQ inputs during WRITE accesses. \overline{CASL} controls DQ1 through DQ8 and \overline{CASH} controls DQ9 through DQ16. The two \overline{CAS} controls give the MT4LC1M16E5(S) both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or \overline{CAS} (\overline{CASL} or \overline{CASH}), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either \overline{CAS} falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after \overline{CAS} (\overline{CASL} or \overline{CASH}) was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of \overline{OE} . During LATE WRITE or READ-MODIFY-WRITE cycles, \overline{OE} must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping \overline{OE} LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by \overline{RAS} followed by a column-address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding RAS LOW and strobing in different column-addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the PAGE MODE of operation.

EDO PAGE MODE

The AS4LC1M16 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after \overline{CAS} returns HIGH. EDO provides for \overline{CAS} precharge time (t_{CP}) to occur without the output data going invalid. This elimination of \overline{CAS} output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of \overline{CAS} . EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after \overline{CAS} goes HIGH during READs, provided \overline{RAS} and \overline{OE} are held LOW. If \overline{OE} is pulsed while \overline{RAS} and \overline{CAS} are LOW, data will toggle from valid data to High-Z and back to the same valid data. If \overline{OE} is toggled or pulsed after \overline{CAS} goes HIGH while \overline{RAS} remains LOW, data will transition to and remain High-Z (refer to Figure 1).

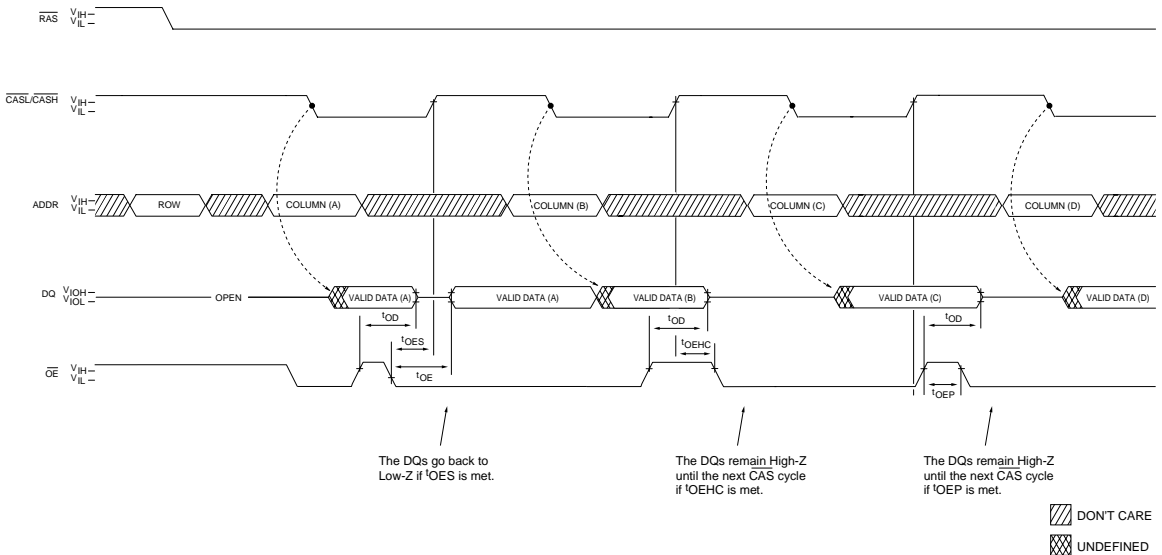


Figure 1
OUTPUT ENABLE AND DISABLE



EDO PAGE MODE (continued)

WE can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternately,

pulsing WE to the idle banks during CAS HIGH time will also High-Z the outputs. Independent of OE control, the outputs will disable after t'OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last.

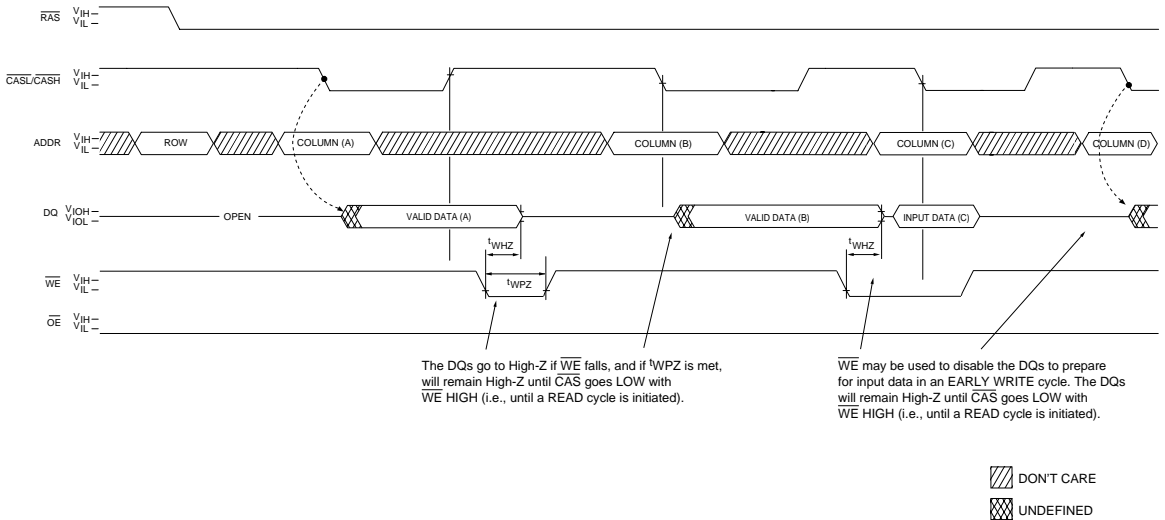


Figure 2
WE CONTROL OF DQs



BYTE ACCESS CYCLE

The BYTE WRITES and BYTE READs are determined by the use of $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$. Enabling $\overline{\text{CASL}}$ will select a lower BYTE access (DQ1-DQ8). Enabling $\overline{\text{CASH}}$ will select an upper BYTE access (DQ9-DQ16). Enabling both $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ selects a WORD WRITE cycle.

The AS4LC1M16 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{\text{CAS}}$ inputs. Figure 3 illustrates the BYTE WRITE and WORD WRITE cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A $\overline{\text{CAS}}$ precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY

WRITE on one byte and a LATE WRITE on the other byte is not allowed during the same cycle. However, an EARLY WRITE on one byte and, after a $\overline{\text{CAS}}$ precharge has been satisfied, a LATE WRITE on the other byte is permissible.

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{\text{RAS}}$ addressing.

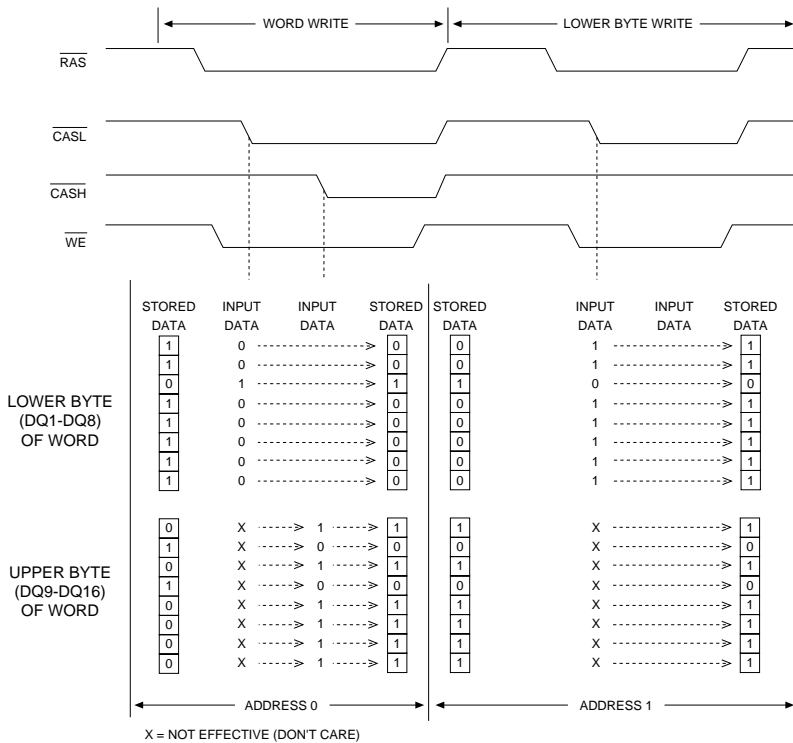
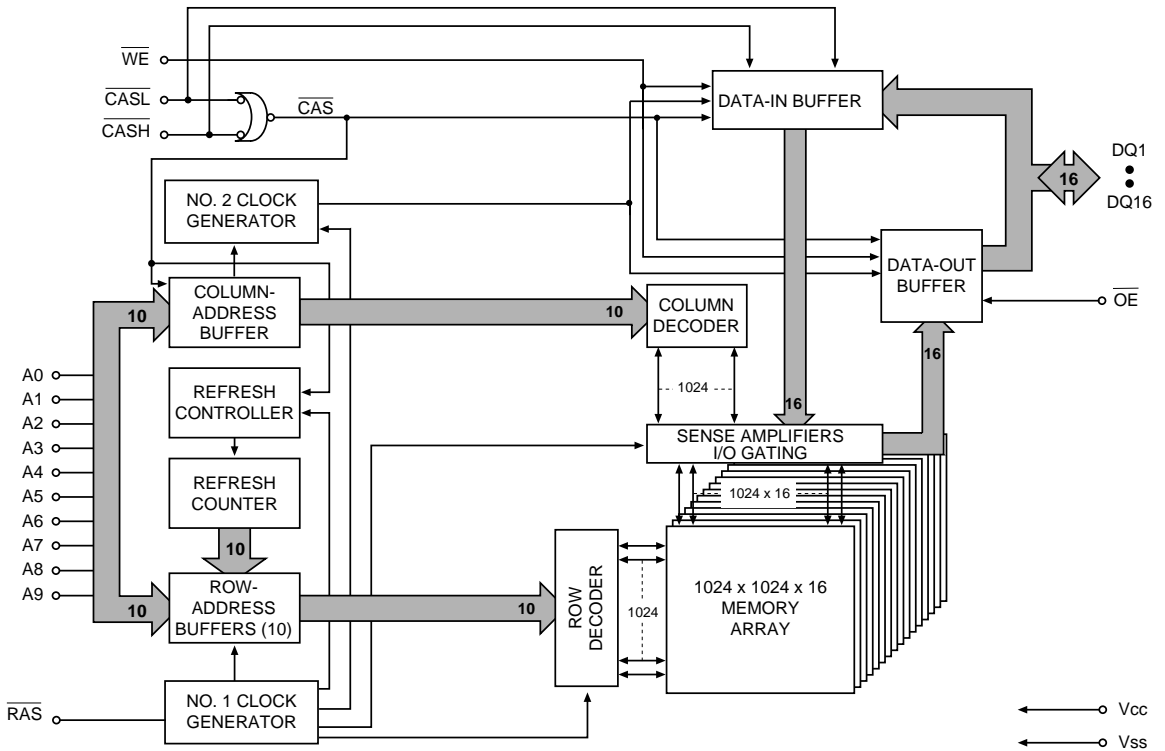


Figure 3
WORD AND BYTE WRITE EXAMPLE



FUNCTIONAL BLOCK DIAGRAM





TRUTH TABLE

FUNCTION	\overline{RAS}	\overline{CASL}	\overline{CASH}	\overline{WE}	\overline{OE}	ADDRESSES		DOs	NOTES	
						'R	'C			
Standby	H	H→X	H→X	X	X	X	X	High-Z		
READ: WORD	L	L	L	H	L	ROW	COL	Data-Out		
READ: LOWER BYTE	L	L	H	H	L	ROW	COL	Lower Byte, Upper Byte, Data-Out		
READ: UPPER BYTE	L	H	L	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte		
WRITE: WORD (EARLY WRITE)	L	L	L	L	X	ROW	COL	Data-In		
WRITE: LOWER BYTE (EARLY)	L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z		
WRITE: UPPER BYTE (EARLY)	L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In		
READ WRITE	L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2	
EDO-PAGE-MODE READ										
	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L	n/a	n/a	Data-Out	2
EDO-PAGE-MODE WRITE										
	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE										
	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH										
	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
\overline{RAS} -ONLY REFRESH	L	H	H	X	X	ROW	n/a	High-Z		
CBR REFRESH	H→L	L	L	H	X	X	X	High-Z	4	

- NOTE:**
1. These WRITE cycles may also be BYTE WRITE cycles (either \overline{CASL} or \overline{CASH} active).
 2. These READ cycles may also be BYTE READ cycles (either \overline{CASL} or \overline{CASH} active).
 3. EARLY WRITE only.
 4. Only one \overline{CAS} must be active (\overline{CASL} or \overline{CASH}).



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc pin Relative to Vss -1.0V to +4.6V
 Voltage on NC, Inputs or I/O pins
 Relative to Vss -1.0V to +5.5V
 Operating Temperature, T_A (ambient) T_A(MIN)=-55°C
 T_C(MAX)=125°C
 Storage Temperature -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V _{IH}	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V Vcc = 3.6V (All other pins not under test = 0V)	I _I	-2	2	μA	4
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V) Vcc=3.6V	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -2.0mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 2.0mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS} = \overline{CAS} = \text{other inputs} = V_{cc} - 0.2V$)	I _{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}, \overline{CAS}$ address cycling: $t_{RC} = t_{RC}$ [MIN])	I _{CC3}	170	155	140	mA	5, 6
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS} = V_{IL}, \overline{CAS}$, address cycling: $t_{PC} = t_{PC}$ [MIN])	I _{CC4}	130	120	110	mA	5, 6
REFRESH CURRENT: \overline{RAS} ONLY Average power supply current (\overline{RAS} cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ [MIN])	I _{CC5}	160	145	130	mA	5, 6
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}, \overline{CAS}$ address cycling: $t_{RC} = t_{RC}$ [MIN])	I _{CC6}	150	140	130	mA	5, 7



CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C _{I1}	7	pF	8
Input Capacitance: RAS, CAS, CASH, WE, OE	C _{I2}	7	pF	8
Input/Output Capacitance: DQ	C _{I0}	8	pF	8

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 2, 3, 6, 9, 10, 11, 12,) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Access time from column-address	^t AA		30		35		40	ns	
Column-address set-up to CAS precharge	^t ACH	15		15		25		ns	
Column-address hold time (referenced to RAS)	^t AR	45		50		60		ns	
Column-address setup time	^t ASC	0		0		0		ns	25
Row-address setup time	^t ASR	0		0		0		ns	25
Column-address to WE delay time	^t AWD	55		60		65		ns	13
Access time from CAS	^t CAC		15		20		20	ns	14, 26
Column-address hold time	^t CAH	10		12		15		ns	25
CAS pulse width	^t CAS	12	10,000	13	10,000	15	10,000	ns	27
CAS hold time (CBR REFRESH)	^t CHR	10		12		15		ns	7, 28
Last CAS going LOW to first CAS to return HIGH	^t CLCH	10		10		15		ns	29
CAS to output in Low-Z	^t CLZ	0		0		0		ns	26
Data output hold after next CAS LOW	^t COH	3		3		3		ns	
CAS precharge time	^t CP	10		10		10		ns	15, 30
Access time from CAS precharge	^t CPA		35		40		40	ns	26
CAS to RAS precharge time	^t CRP	5		5		5		ns	28
CAS hold time	^t CSH	50		55		60		ns	28
CAS setup time (CBR REFRESH)	^t CSR	5		5		10		ns	7, 25
CAS to WE delay time	^t CWD	35		40		45		ns	13, 25
Write command to CAS lead time	^t CWL	15		15		20		ns	28
Data-in hold time	^t DH	10		12		15		ns	16, 26
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Data-in setup time	^t DS	0		0		0		ns	16, 26
Output disable	^t OD	0	15	0	15	0	15	ns	
Output Enable	^t OE		15		20		20	ns	17, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	12		12		15		ns	18
OE HIGH hold from CAS HIGH	^t OEHC	10		10		10		ns	18
OE HIGH pulse width	^t OEP	10		10		10		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 2, 3, 6, 9, 10, 11, 12, 20) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
OE LOW to CAS HIGH setup time	^t OES	5		5		10		ns	
Output buffer turn-off delay	^t OFF	0	15	0	15	0	20	ns	20, 26
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^t PC	30		35		40		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	^t PRWC	75		85		90		ns	31
Access time from RAS	^t RAC		60		70		80	ns	19
RAS to column-address delay time	^t RAD	12	30	12	35	15	40	ns	21
Row-address hold time	^t RAH	10		10		10		ns	
Column-address to RAS lead time	^t RAL	30		35		40		ns	
RAS pulse width	^t RAS	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (EDO PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
RAS to CAS delay time	^t RCD	14	45	14	50	16	60	ns	22, 25
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	23, 28
Read command setup time	^t RCS	0		0		0		ns	25
Refresh period (1,024 cycles)	^t REF		16		16		16	ms	
RAS precharge time	^t RP	40		50		60		ns	
RAS to CAS precharge time	^t RPC	5		5		5		ns	
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	23
RAS hold time	^t RSH	13		15		20		ns	32
READ WRITE cycle time	^t RWC	150		180		200		ns	
RAS to WE delay time	^t RWD	80		90		105		ns	13
Write command to RAS lead time	^t RWL	15		18		20		ns	
Transition time (rise or fall)	^t T	2	50	2	50	2	50	ns	
Write command hold time	^t WCH	10		12		15		ns	32
Write command hold time (referenced to RAS)	^t WCR	45		55		60		ns	
WE command setup time	^t WCS	0		0		0		ns	13, 25
Output disable delay from WE	^t WHZ	0	13	0	15	0	20	ns	
Write command pulse width	^t WP	10		12		15		ns	
WE pulse width to disable at CAS HIGH	^t WPZ	10		12		15		ns	
WE hold time (CBR REFRESH)	^t WRH	10		10		10		ns	
WE setup time (CBR REFRESH)	^t WRP	10		10		10		ns	

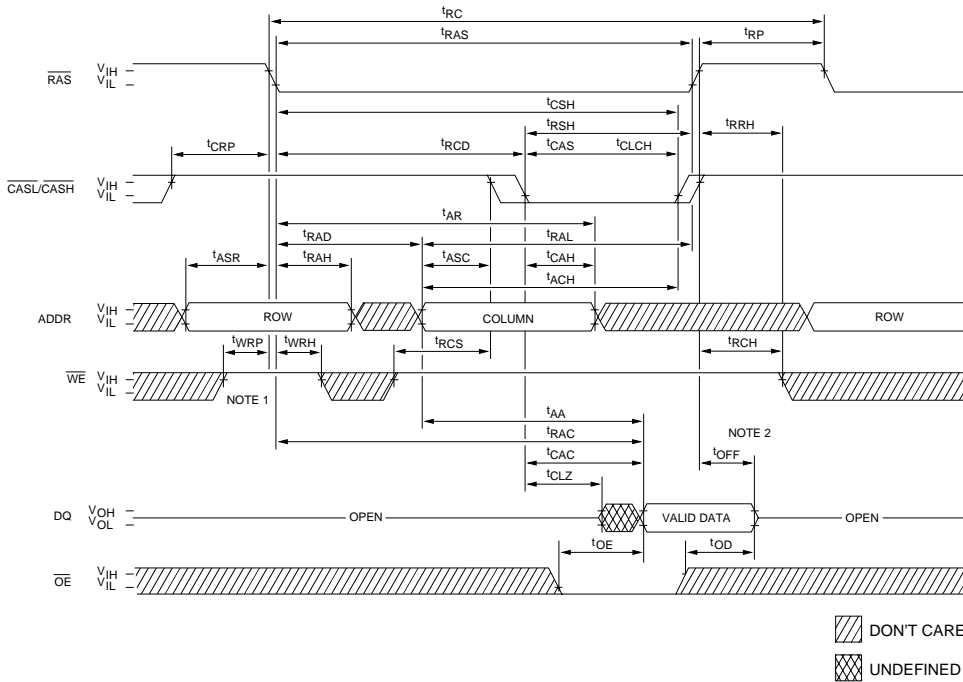


NOTES

1. All voltages referenced to V_{SS} .
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) is assured.
3. An initial pause of $100\mu\text{s}$ is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the $\overline{\text{REF}}$ refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. $V_{CC} = +3.0\text{V}$; $f = 1\text{ MHz}$.
9. AC characteristics assume $t = 2.5\text{ns}$.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates, 100pF and $V_{OL} = 0.8\text{V}$ and $V_{OH} = 2.0\text{V}$.
13. ${}^t\text{WCS}$, ${}^t\text{RWD}$, ${}^t\text{AWD}$ and ${}^t\text{CWD}$ are not restrictive operating parameters. ${}^t\text{WCS}$ applies to EARLY WRITE cycles. ${}^t\text{RWD}$, ${}^t\text{AWD}$ and ${}^t\text{CWD}$ apply to READ-MODIFY-WRITE cycles. If ${}^t\text{WCS} \geq {}^t\text{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^t\text{WCS} < {}^t\text{WCS}$ (MIN) and ${}^t\text{RWD} \geq {}^t\text{RWD}$ (MIN), ${}^t\text{AWD} \geq {}^t\text{AWD}$ (MIN) and ${}^t\text{CWD} \geq {}^t\text{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$ -controlled) cycle. ${}^t\text{WCS}$, ${}^t\text{RWD}$, ${}^t\text{CWD}$ and ${}^t\text{AWD}$ are not applicable in a LATE WRITE cycle.
14. Assumes that ${}^t\text{RCD} \geq {}^t\text{RCD}$ (MAX).
15. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ${}^t\text{CP}$.
16. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{\text{WE}}$ must be pulsed during $\overline{\text{CAS}}$ HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ${}^t\text{OD}$ and ${}^t\text{OE}$ met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after ${}^t\text{OE}$ is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
19. Assumes that ${}^t\text{RCD} < {}^t\text{RCD}$ (MAX). If ${}^t\text{RCD}$ is greater than the maximum recommended value shown in this table, ${}^t\text{RAC}$ will increase by the amount that ${}^t\text{RCD}$ exceeds the value shown.
20. ${}^t\text{OFF}$ (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL} . It is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
21. Operation within the ${}^t\text{RAD}$ (MAX) limit ensures that ${}^t\text{RAC}$ (MIN) and ${}^t\text{CAC}$ (MIN) can be met. ${}^t\text{RAD}$ (MAX) is specified as a reference point only; if ${}^t\text{RAD}$ is greater than the specified ${}^t\text{RAD}$ (MAX) limit, then access time is controlled exclusively by ${}^t\text{AA}$, provided ${}^t\text{RCD}$ is not exceeded.
22. Operation within the ${}^t\text{RCD}$ (MAX) limit ensures that ${}^t\text{RAC}$ (MAX) can be met. ${}^t\text{RCD}$ (MAX) is specified as a reference point only; if ${}^t\text{RCD}$ is greater than the specified ${}^t\text{RCD}$ (MAX) limit, then access time is controlled exclusively by ${}^t\text{CAC}$, provided ${}^t\text{RAD}$ is not exceeded.
23. Either ${}^t\text{RCH}$ or ${}^t\text{RRH}$ must be satisfied for a READ cycle.
24. The first $\overline{\text{CASx}}$ edge to transition LOW.
25. Output parameter (DQx) is referenced to corresponding $\overline{\text{CAS}}$ input; DQ1-DQ8 by $\overline{\text{CASL}}$ and DQ9-DQ16 by $\overline{\text{CASH}}$.
26. Each $\overline{\text{CASx}}$ must meet minimum pulse width.
27. The last $\overline{\text{CASx}}$ edge to transition HIGH.
28. Last falling $\overline{\text{CASx}}$ edge to first rising $\overline{\text{CASx}}$ edge.
29. Last rising $\overline{\text{CASx}}$ edge to first falling $\overline{\text{CASx}}$ edge.
30. Last rising $\overline{\text{CASx}}$ edge to next cycle's last rising $\overline{\text{CASx}}$ edge.
31. Last $\overline{\text{CASx}}$ to go LOW.
32. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}} = \text{LOW}$ and $\overline{\text{OE}} = \text{HIGH}$.



READ CYCLE



- NOTE:**
- Although \overline{WE} is a "don't care" at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.
 - t_{OFF} is referenced from rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

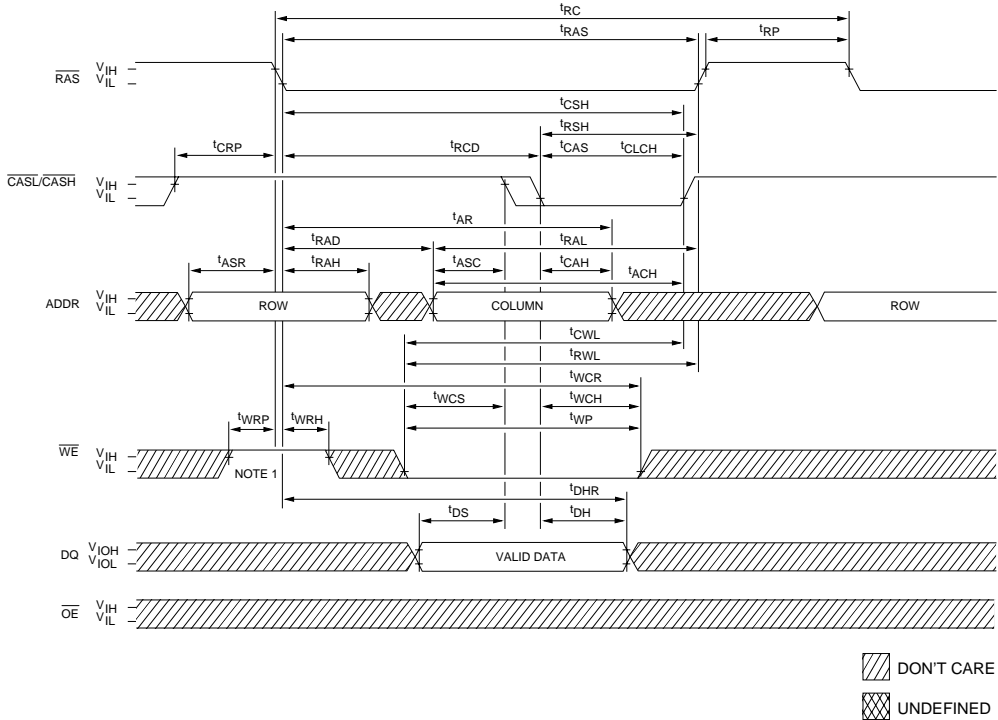
TIMING PARAMETERS

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA}		30		35		40	ns
t _{ACH}	15		15		20		ns
t _{AR}	45		50		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{CAC}		15		20		20	ns
t _{CAH}	10		12		15		ns
t _{CAS}	12	10,000	13	10,000	20	10,000	ns
t _{CLCH}	10		10		10		ns
t _{CLZ}	0		0		0		ns
t _{CRP}	5		5		5		ns
t _{CSH}	50		55		60		ns
t _{OD}	0	15	0	15	0	20	ns
t _{OE}		15		20		20	ns
t _{OFF}	0	15	0	15	0	20	ns

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RAC}		60		70		80	ns
t _{RAD}	12	30	12	35	15	40	ns
t _{RAH}	10		10		10		ns
t _{RAL}	30		35		40		ns
t _{RAS}	60	10,000	70	10,000	80	10,000	ns
t _{RC}	110		130		150		ns
t _{RCD}	14	45	14	50	20	60	ns
t _{RCH}	0		0		0		ns
t _{RCS}	0		0		0		ns
t _{RP}	40		50		60		ns
t _{RRH}	0		0		0		ns
t _{RSH}	13		15		15		ns
t _{WRH}	10		10		10		ns
t _{WRP}	10		10		10		ns



EARLY WRITE CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for t_{WRP} and t_{WRH}. This design implementation will facilitate compatibility with future EDO DRAMs.

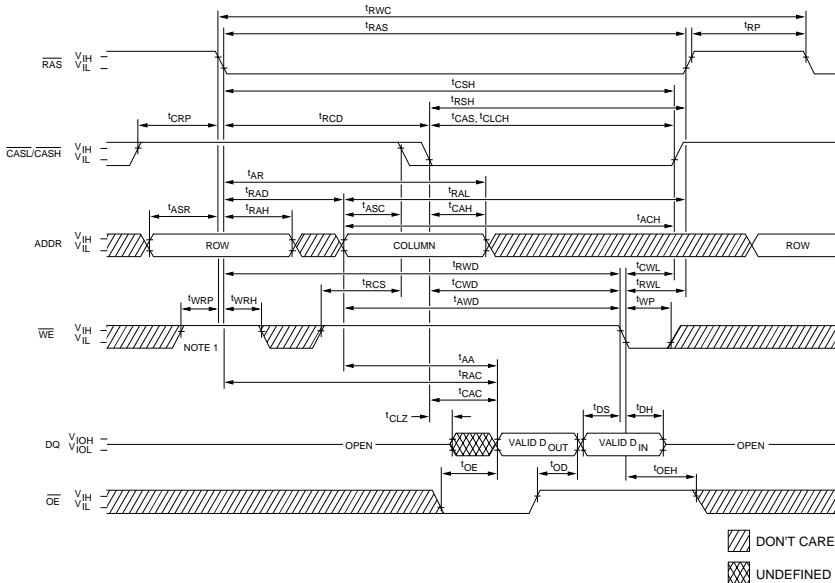
TIMING PARAMETERS

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{ACH}	15		15		20		ns
t _{AR}	45		50		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{CAH}	10		12		15		ns
t _{CAS}	12	10,000	13	10,000	20	10,000	ns
t _{CLCH}	10		10		10		ns
t _{CRP}	5		5		5		ns
t _{CSH}	50		55		60		ns
t _{CWL}	15		15		20		ns
t _{DH}	10		12		15		ns
t _{DHR}	45		55		55		ns
t _{DS}	0		0		0		ns
t _{RAD}	12	30	12	35	15	40	ns

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RAH}	10		10		10		ns
t _{RAL}	30		35		40		ns
t _{RAS}	60	10,000	70	10,000	80	10,000	ns
t _{RC}	110		130		150		ns
t _{RCD}	14	45	14	50	20	60	ns
t _{RP}	40		50		60		ns
t _{RSH}	13		15		0		ns
t _{RWL}	15		15		20		ns
t _{WCH}	10		12		15		ns
t _{WCR}	45		55		60		ns
t _{WCS}	0		0		0		ns
t _{WP}	10		12		15		ns
t _{WRH}	10		10		10		ns
t _{WRP}	10		10		10		ns



READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. Although \overline{WE} is a "don't care" at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH}. This design implementation will facilitate compatibility with future EDO DRAMs.

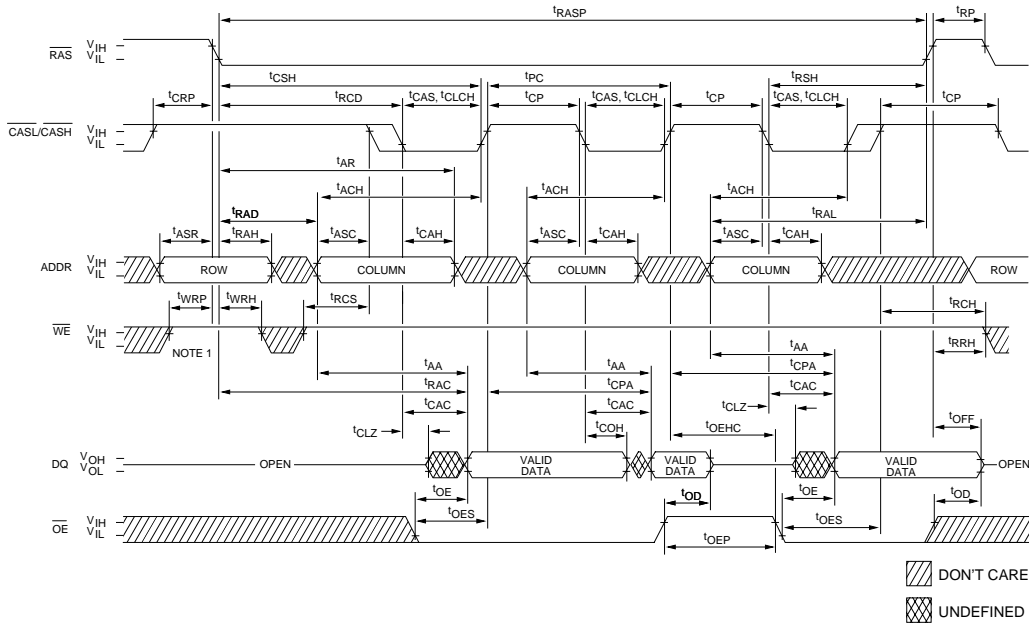
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{ACH}	15		15		20		ns
t _{AR}	45		50		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{AWD}	55		60		65		ns
t _{CAC}		15		20		20	ns
t _{CAH}	10		12		15		ns
t _{CAS}	12	10,000	13	10,000	20	10,000	ns
t _{CLCH}	10		10		10		ns
t _{CLZ}	0		0		0		ns
t _{CRP}	5		5		5		ns
t _{CSH}	50		55		60		ns
t _{CWD}	35		40		45		ns
t _{CWL}	15		15		20		ns
t _{DH}	10		12		15		ns
t _{DS}	0		0		0		ns
t _{OD}	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OE}		15		20		20	ns
t _{OEH}	12		12		15		ns
t _{RAC}		60		70		80	ns
t _{RAS}	12	30	12	35	15	40	ns
t _{RAH}	10		10		10		ns
t _{RAL}	30		35		40		ns
t _{RAS}	60	10,000	70	10,000	80	10,000	ns
t _{RCD}	14	45	14	50	20	60	ns
t _{RCS}	0		0		0		ns
t _{RP}	40		50		60		ns
t _{RSH}	13		15		15		ns
t _{RWC}	150		180		200		ns
t _{RWD}	80		90		105		ns
t _{RWL}	15		15		20		ns
t _{WP}	10		12		15		ns
t _{WRH}	10		10		10		ns
t _{WRP}	10		10		10		ns



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for t_{WRP} and t_{WRH}. This design implementation will facilitate compatibility with future EDO DRAMs.

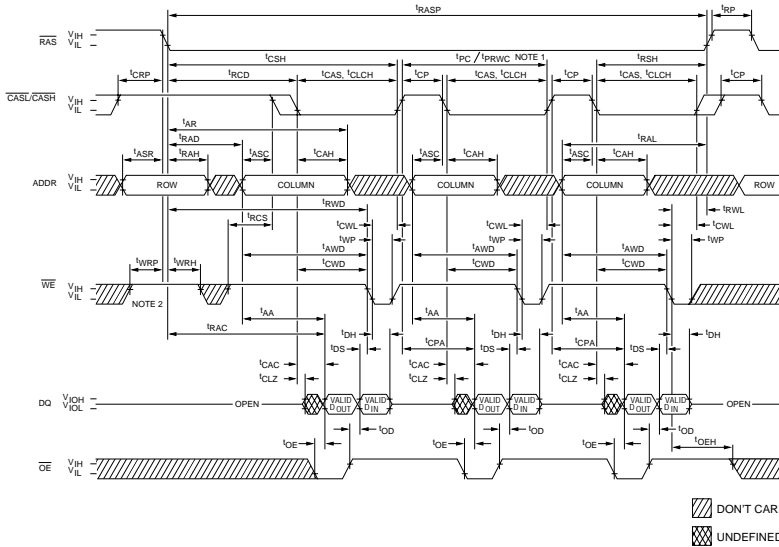
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{ACH}	15		15		20		ns
t _{AR}	45		50		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{CAC}		15		20		20	ns
t _{CAH}	10		12		15		ns
t _{CAS}	12	10,000	13	10,000	20	10,000	ns
t _{CLCH}	10		10		10		ns
t _{CLZ}	0		0		0		ns
t _{COH}	3		3		5		ns
t _{CP}	10		10		10		ns
t _{CPA}		35		40		40	ns
t _{CRP}	5		5		5		ns
t _{CSH}	50		55		60		ns
t _{OD}	0	15	0	15	0	20	ns
t _{OE}		15		20		20	ns
t _{OEHC}	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OEP}	10		10		10		ns
t _{OES}	5		5		5		ns
t _{OFF}	3	15	3	15	0	20	ns
t _{PC}	30		35		40		ns
t _{RAC}		60		70		80	ns
t _{RAD}	12	30	12	35	15	40	ns
t _{RAH}	10		10		10		ns
t _{RAL}	30		35		40		ns
t _{RASP}	60	100,000	70	100,000	80	100,000	ns
t _{RCD}	14	45	14	50	20	60	ns
t _{RCH}	0		0		0		ns
t _{RCS}	0		0		0		ns
t _{RP}	40		50		60		ns
t _{RRH}	0		0		0		ns
t _{RSH}	13		15		15		ns
t _{WRH}	10		10		10		ns
t _{WRP}	10		10		10		ns



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



- NOTE:**
- t_{PC} is for LATE WRITE cycles only.
 - Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

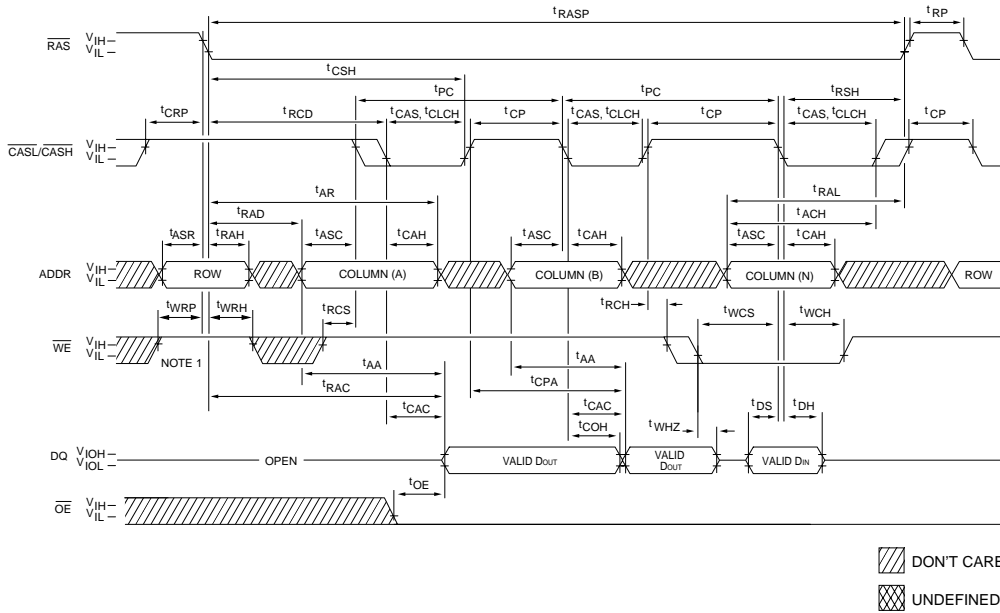
TIMING PARAMETERS

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}		30		35		40	ns
t_{AR}	45		50		60		ns
t_{ASC}	0		0		0		ns
t_{ASR}	0		0		0		ns
t_{AWD}	55		60		65		ns
t_{CAC}		15		20		20	ns
t_{CAH}	10		12		15		ns
t_{CAS}	12	10,000	13	10,000	20	10,000	ns
t_{CLCH}	10		10		10		ns
t_{CLZ}	0		0		0		ns
t_{CP}	10		10		10		ns
t_{CPA}		35		40		40	ns
t_{CRP}	5		5		5		ns
t_{CSH}	50		55		60		ns
t_{CWD}	35		40		45		ns
t_{CWL}	15		15		20		ns
t_{DH}	10		12		15		ns
t_{DS}	0		0		0		ns
t_{OD}	0	15	0	15	0	20	ns

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{OE}		15		20		20	ns
t_{OEh}	12		12		15		ns
t_{PC}	25		30		40		ns
t_{PRWC}	75		85		90		ns
t_{RAC}		60		70		80	ns
t_{RAD}	12	30	12	35	15	40	ns
t_{RAH}	10		10		10		ns
t_{RAL}	30		35		40		ns
t_{RASP}	60	125,000	70	125,000	80	100,000	ns
t_{RCD}	14	45	14	50	20	60	ns
t_{RCS}	0		0		0		ns
t_{RP}	40		50		60		ns
t_{RSH}	13		15		15		ns
t_{RWD}	80		90		105		ns
t_{RWL}	15		15		20		ns
t_{WP}	10		12		15		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

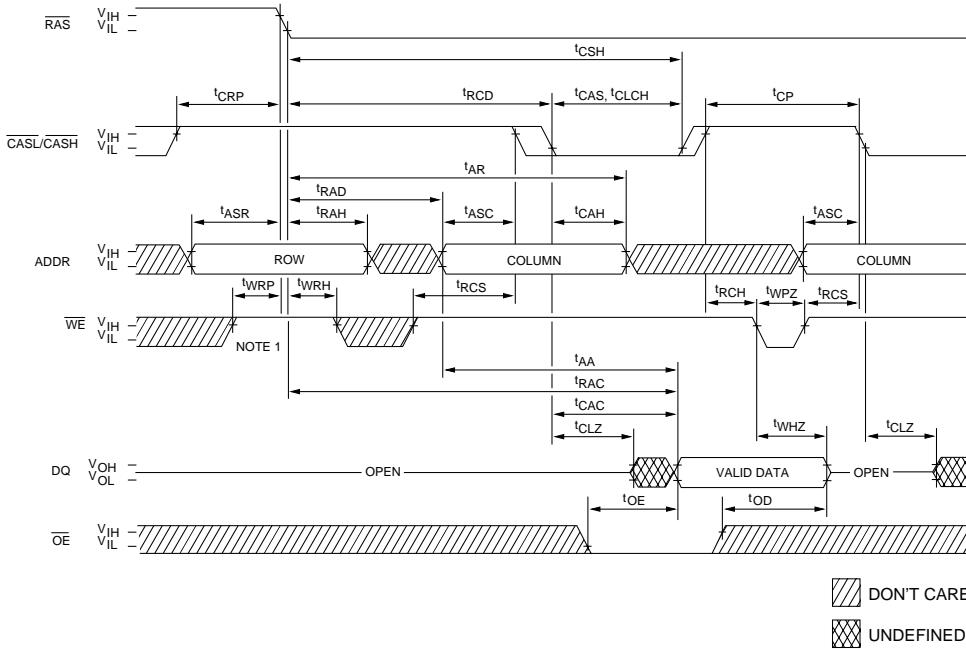
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH	15		15		20		ns
tAR	45		50		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		12		15		ns
tCAS	12	10,000	13	10,000	20	10,000	ns
tCLCH	10		10		10		ns
tCOH	3		3		5		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tDH	10		12		15		ns
tDS	0		0		0		ns
tOE		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tPC	25		30		40		ns
tRAC		60		70		80	ns
tRAD	12	30	12	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	125,000	70	125,000	80	100,000	ns
tRCD	14	45	14	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRSH	13		15		15		ns
tWCH	10		12		15		ns
tWCS	0		0		0		ns
tWHZ	0	13	0	15	0	20	ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns



READ CYCLE
(with WE-controlled disable)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

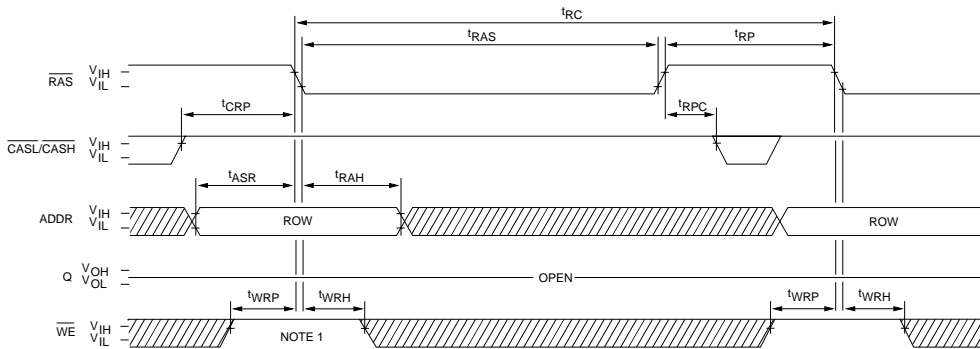
TIMING PARAMETERS

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
tAA		30		35		40	ns
tAR	45		50		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		12		15		ns
tCAH	12	10,000	13	10,000	20	10,000	ns
tCLCH	10		10		10		ns
tCLZ	0		0		0		ns
tCP	10		10		10		ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns

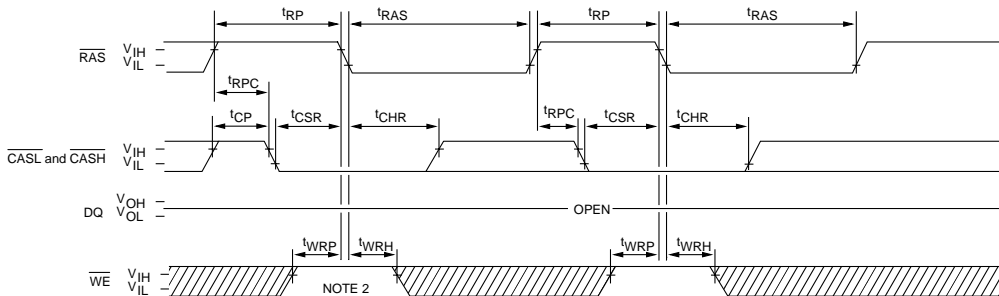
SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
tOD	0	15	0	15	0	15	ns
tOE		15		20		20	ns
tRAC		60		70		80	ns
tRAD	12	30	12	35	15	40	ns
tRAH	10		10		10		ns
tRCD	14	45	14	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tWHZ	0	13	0	15	0	20	ns
tWPZ	10		12		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns



RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE
(Addresses and \overline{OE} = DON'T CARE)



- NOTE:**
1. Although \overline{WE} is a "don't care" at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.
 2. t_{WRP} and t_{WRH} are for system design reference only. The \overline{WE} signal is actually a "don't care" at \overline{RAS} time during a CBR REFRESH. However, \overline{WE} should be held HIGH at \overline{RAS} time during a CBR REFRESH to ensure compatibility with other DRAMs that require \overline{WE} HIGH at \overline{RAS} time during a CBR REFRESH.

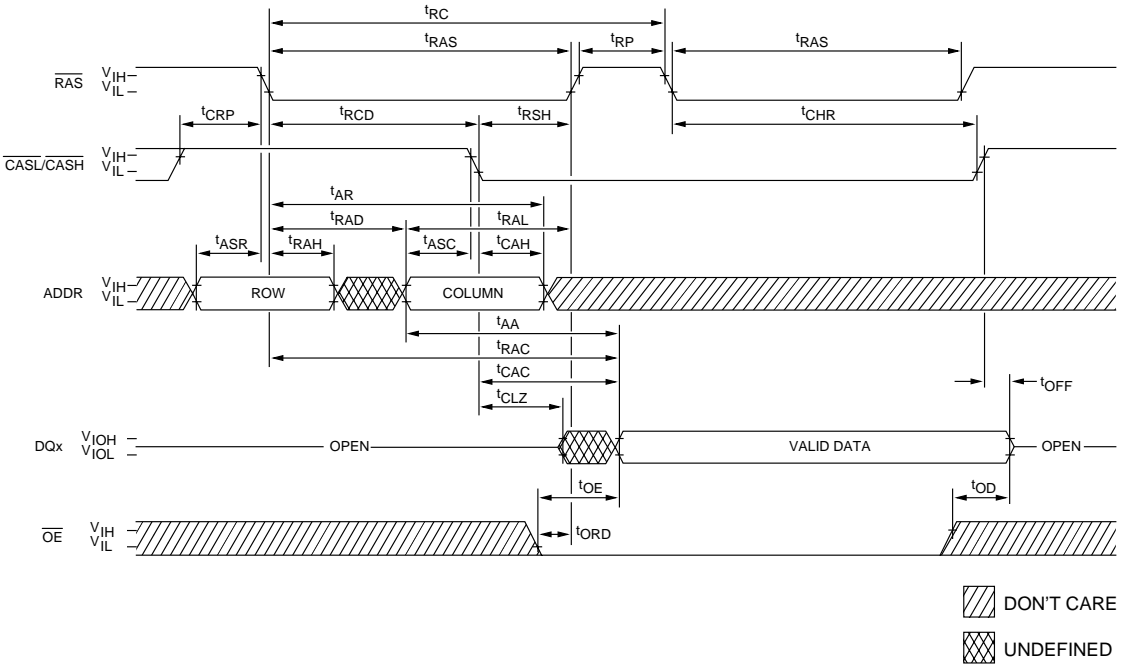
TIMING PARAMETERS

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ASR}	0		0		0		ns
t_{CHR}	10		12		15		ns
t_{CP}	10		10		10		ns
t_{CRP}	5		5		5		ns
t_{CSR}	5		5		10		ns
t_{RAH}	10		10		10		ns

SYM	-6		-7		-8		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAS}	60	10,000	70	10,000	80	10,000	ns
t_{RC}	105		125		150		ns
t_{RP}	40		50		60		ns
t_{RPC}	5		5		5		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns



HIDDEN REFRESH CYCLE³²
(WE = HIGH; OE = LOW)



TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{AR}	45		50		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{CAC}		15		20		20	ns
t _{CAH}	10		12		15		ns
t _{CHR}	10		12		15		ns
t _{CLZ}	0		0		0		ns
t _{CRP}	5		5		5		ns
t _{OD}	0	15	0	15	0	20	ns
t _{OE}		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OFF}	3	15	3	15	3	15	ns
t _{ORD}	0		0		0		ns
t _{RAC}		60		70		80	ns
t _{RAH}	12	30	12	35	15	40	ns
t _{RAL}	10		10		10		ns
t _{RAS}	30		35		40		ns
t _{RAS}	60	10,000	70	10,000	80	10,000	ns
t _{RC}	105		125		145		ns
t _{RCD}	14	45	14	50	20	60	ns
t _{RP}	40		50		60		ns
t _{RSH}	13		15		15		ns



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

