ACT5880

Rev 2, 03-Sep-13

15 Channels Advanced PMU for Smart Phone

FEATURES

- **Flexible CCCV Charger with Internal MOSFET**
  - **Programmable Charge Current**
  - **Programmable Charge Termination Voltage**
  - **Programmable OVP threshold**
  - **Regulation against Die Thermal Condition**
  - **Charge Status Output, LED driving**
  - **Battery Thermal Condition Monitor**
  - **Battery Installation Detection**
  - **USB Charging Compatible**
- **Fifteen Channels of Power Supplies**
  - **Two Step-Down DC/DC Converters**
  - **One Step-up Regulator, ~40V, ~750mA Switch**
  - **Seven High PSRR LDOs**
  - **Three Low Quiescent Current LDOs**
  - **One Always-on LDO**
  - **One Back-up Battery/Super-Capacitor Charger**
- **Advanced System Control and Interfaces**
  - **I²C™ Serial Interface**
  - **Touch Screen Controller with Three AUX Inputs**
- **Advanced Function**
  - **Real Time Clock**
  - **Three CC/PWM LED Drivers, ODO1 Supports up to 40V**

GENERAL DESCRIPTION

The ACT5880 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution, optimized for portable devices like smart phones, Mobile Internet Devices.

This device features two step-down DC/DC converters, one step-up DC/DC regulator, seven high PSRR LDOs, three low quiescent current LDOs, one always-on LDO, and one back-up battery/super-capacitor charger, along with a complete battery charging solution.

This device also integrates a touch screen controller interface with three AUX inputs, three current controlled LED drivers, and a Real Time Clock.

The two step-down DC/DC converters utilize a high efficiency, fixed-frequency (2MHz), current-mode PWM control architecture that requires a minimum number of external components. Two step-down DC/DCs are capable of supplying up to 1200mA and 700mA of output current. All LDOs are high-performance, low-noise, regulators that supply up to 360mA of output current. The back-up battery charger supports up to 3.5mA of output current.

The ACT5880 is available in a compact, Pb-Free and RoHS-compliant, 81 balls, 6mmx6mm FC-FBGA package with 1mm height.

TYPICAL APPLICATION DIAGRAM

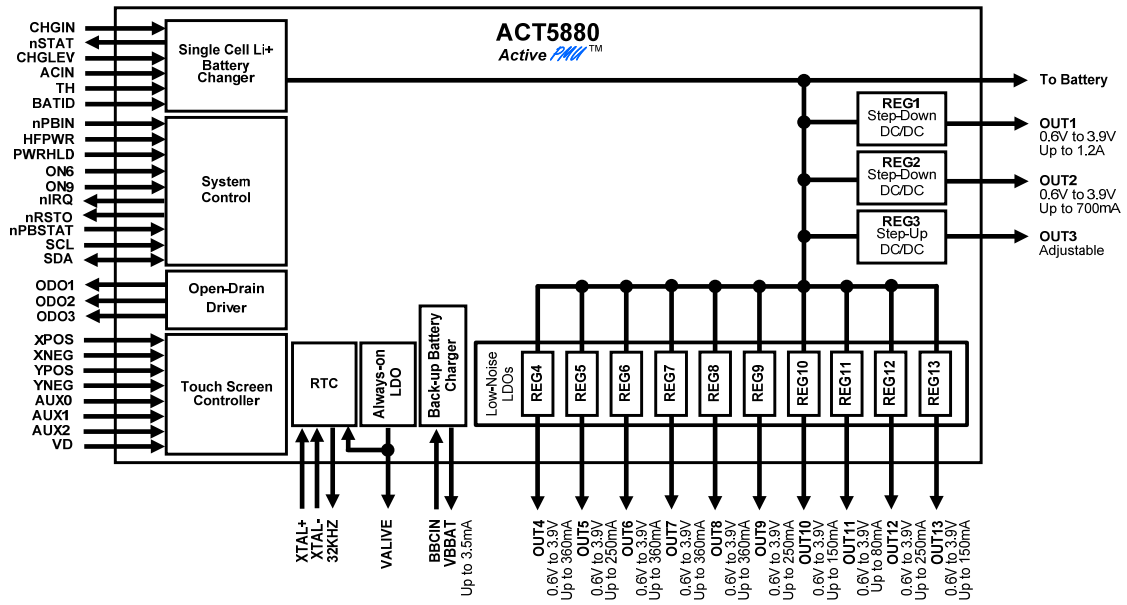
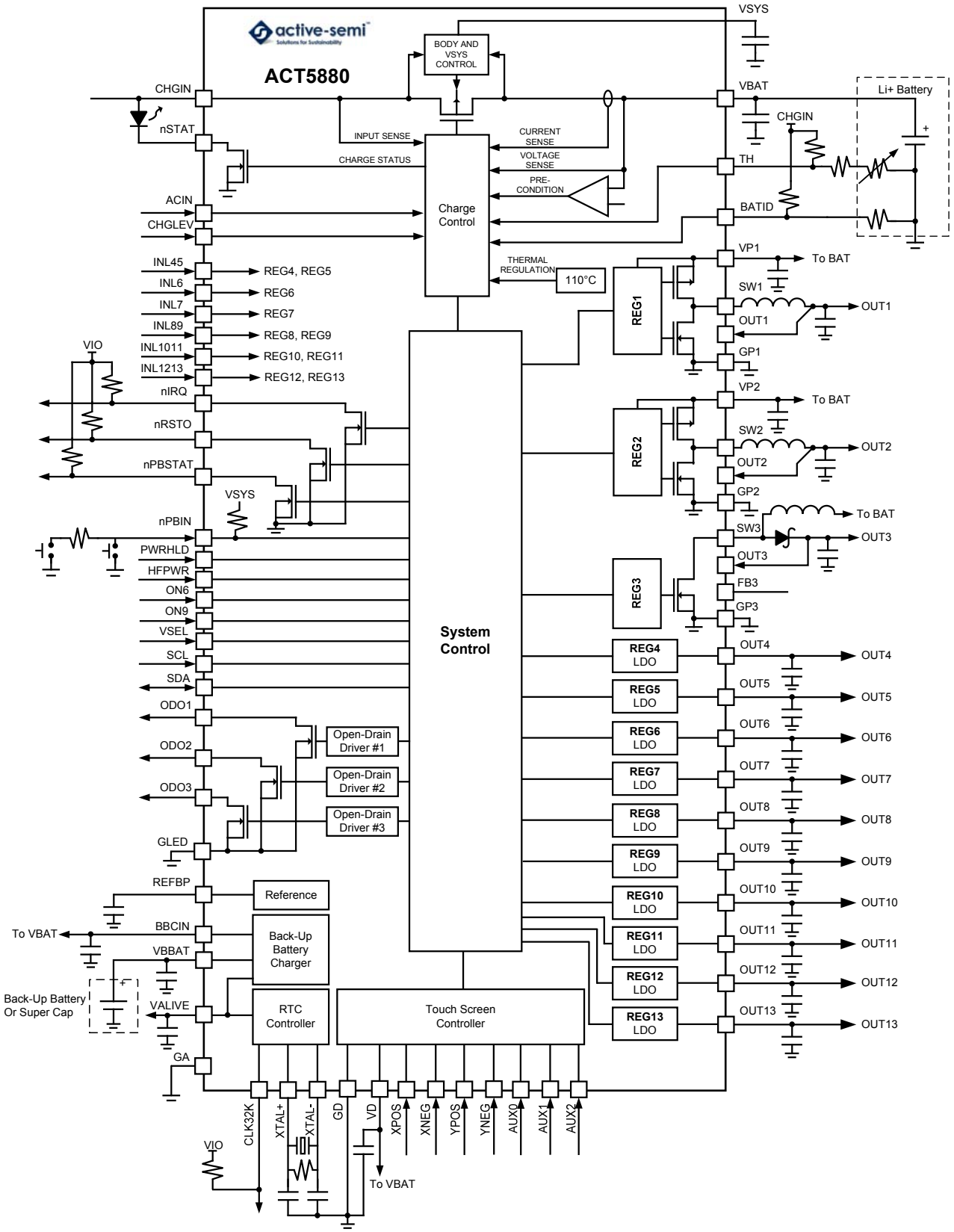


TABLE OF CONTENTS

TABLE OF CONTENTS CONT'D

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①

PART NUMBER	V_{OUT1}/V_{STBY1}②	V_{OUT2}	REG3 MODE	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}
ACT5880WX1150-T	1.2V/1.2V	1.8V	Voltage	5V	2.9V	2.9V	2.9V	3.0V

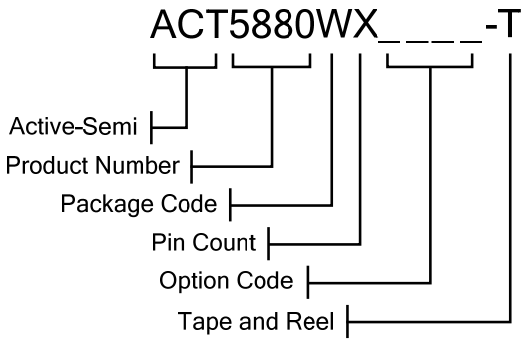
V_{OUT8}	V_{OUT9}	V_{OUT10}	V_{OUT11}	V_{OUT12}	V_{OUT13}	V_{VBAT}	V_{BBAT}	I_{LIMBB}	V_{ALIVE}
2.5V	1.2V	3.3V	1.8V	1.8V	2.8V	4.2V	2.7V	5mA	1.8V

OPEN DRAIN DRIVER DUTY SETTING OPTION	BATTERY INSTALLATION DETECTION OPTION	BATTERY THERMAL CONDITION OPTION	BATTERY THERMAL OR BATTERY INSTALLATION INTERRUPT OPTION
Linear	Enable	Enable	Battery Thermal

PART NUMBER	PACKAGE	PINS	TEMPERATURE RANGE	PACKING
ACT5880WX1150-T	FBGA	81	-40°C to +85°C	Tape and Reel

①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

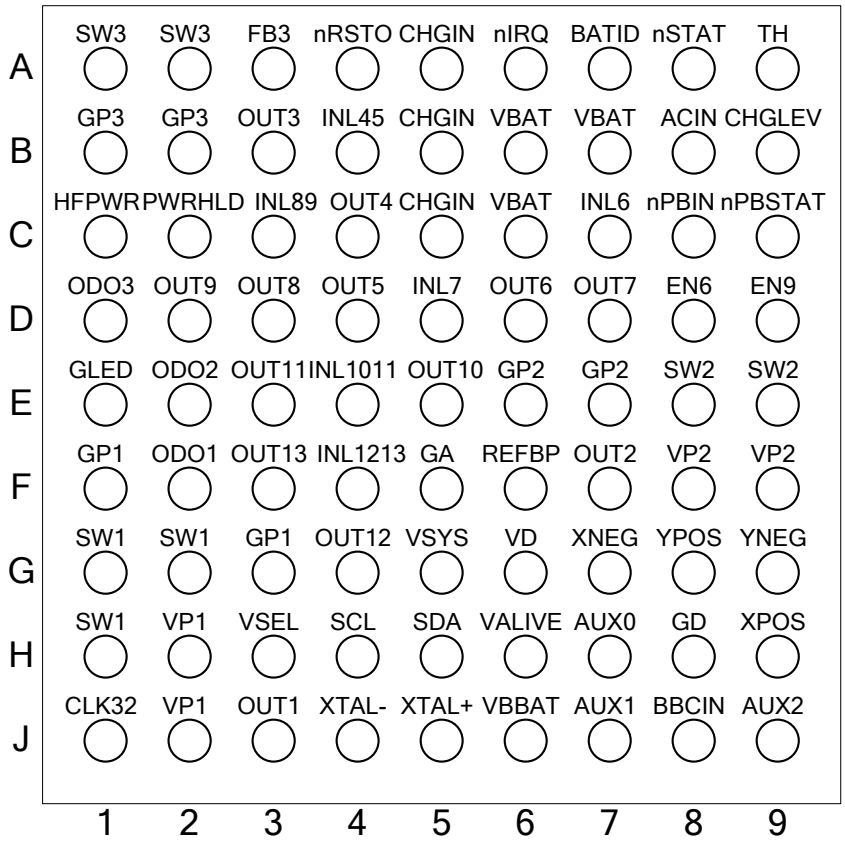
②: Drive VSEL to a logic high to select V_{STBY1} as a output regulation voltage of REG1. The V_{STBY1} can be set by software via I^2C interface, refer to appropriate sections of this datasheet for V_{STBY1} setting.



PACKAGE APPEARANCE AND TOP MARKS

PIN CONFIGURATION

TOP VIEW



81 balls FC FBGA (Pitch: 0.5mm; Ball: 0.3mm)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1	SW3	The Switch Node of the Step-up DC/DC. Same function as pin A2.
A2	SW3	The Switch Node of the Step-up DC/DC. Same function as pin A1.
A3	FB3	The Current Feedback Input in constant current mode, or leave it unconnected in voltage regulation mode. Connect to current sense resistor in serial in the WLED string, sense the voltage to ground to regulate the WLED string current in constant current driver mode, or connect to the voltage sense tip in inverse regulator mode. These modes are factory programmable only.
A4	nRSTO	The Reset Output, OD and Active Low. Asserted low during power up and keep low for 260ms for system reset after OUT1 is in regulation. Refer to *The Power-On Sequences* section for more details .
A5	CHGIN	The Charger Input. Power input to the charger and the system, same function as pin B5 and pin C5. Bypass to GA with a 6.8µF high quality ceramic capacitor.
A6	nIRQ	The Interrupt Request Output, OD and Active Low. Asserted low when specified conditions qualified. De-asserted when reading the respective register bits or writing the respective register bits.
A7	BATID	The Battery Installed Detection. Connect to the ID pin of the battery house connector, to detect if a battery pack is installed by checking the voltage at this pin. Refer to *The Battery Installed Detection* section for more details.
A8	nSTAT	The Charger Status Output, OD with Internal 8mA Current Limit. Sink current when the charger is in precondition, fast charge and top-off states. It turns into high-Z in other charge states.
A9	TH	The Thermistor Monitoring Input. Monitor the battery pack temperature by reading the NTC thermistor in battery pack and only allow charging when the temperature is in a suitable temperature window.
B1	GP3	The Ground Path of Step-up DC/DC. Provide the direct ground return path between internal switch, the external storage capacitor and the input decoupling capacitor. Same function as pin B2. Connect GA, GP1, GP2 and GP3 to a single point as close to the IC as possible.
B2	GP3	The Ground Path of Step-up DC/DC. Same function as pin B1.
B3	OUT3	The Step-up DC/DC Voltage Sense Node in the Voltage Regulation Mode, Over-Voltage Protection Sense Input in the Constant Current Mode. Connect to the Step-up DC/DC output in both modes. The modes are factory programmable only options. Bypass to GA with a 2.2µF high quality ceramic capacitor.
B4	INL45	The Input Node for the LDO REG4 and REG5. Bypass to GA with a 1µF high quality ceramic capacitor placed as close to the IC as possible.
B5	CHGIN	The Charger Input. Same function as pin A5 and pin C5.
B6	VBAT	The Charger Output. Feed power to the battery and the system. Connect to the battery pack positive terminal, same function as pin B7 and pin C6.Bypass to GA with a 4.7µF high quality ceramic capacitor.
B7	VBAT	The Charger Output. Same function as pin B6 and pin C6.
B8	ACIN	The Adaptor Charging Input Detection. Pull this pin to a logic high when an adaptor is available or ground it otherwise.
B9	CHGLEV	The Charge Current Level Selection. A logic input to select charging current when the ACIN is pulled low, which is presumably for charging from the USB V_{BUS}. Set high for 450mA charging and low for 90mA charging. The status of this pin does not affect the charging current during adaptor charging when the ACIN is pulled high.
C1	HFPWR	The Hand-Free Power Request Input. Pull this pin high to request system power on if this chip is not enabled, to initialize the normal power up procedure. When the IC is already enabled, logic changes at this pin asserts nIRQ to request for system host service.
C2	PWRHLD	The Power Hold Input. Pull this pin high to hold the IC to be in enable state.
C3	INL89	The Input Node for the LDO REG8 and REG9. Bypass to GA with a 1µF high quality ceramic capacitor.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
C4	OUT4	The Output of the LDO REG4. Bypass to GA with a 3.3μF high quality ceramic capacitor.
C5	CHGIN	The Charger Input. Same function as pin A5 and pin B5.
C6	VBAT	The Charger Output. Same function as pin B6 and pin B7.
C7	INL6	The Input Node for the LDO REG6. Bypass to GA with a 1μF high quality ceramic capacitor.
C8	nPBIN	The Push-Button Input. Drive nPBIN to GA through a 50kΩ resistor to enable the IC. When the IC is enabled, driving nPBIN to GA through a 50kΩ resistor asserts the nIRQ to call interrupt service from the host system, and driving nPBIN to GA directly asserts a manual reset procedure. nPBIN is internally pulled up to VSYS through a 35kΩ resistor.
C9	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise.
D1	ODO3	The Open Drain Output 3. A current driver output with programmable output current. It could operate in constant current mode, switch on/off mode or PWM mode. The maximum voltage is 6V for this pin.
D2	OUT9	The Output of the LDO REG9. Bypass to GA with a 2.2μF high quality ceramic capacitor.
D3	OUT8	The Output of the LDO REG8. Bypass to GA with a 3.3μF high quality ceramic capacitor.
D4	OUT5	The Output of the LDO REG5. Bypass to GA with a 2.2μF high quality ceramic capacitor.
D5	INL7	The Input Node for the LDO REG7. Bypass to GA with a 1μF high quality ceramic capacitor.
D6	OUT6	The Output of the LDO REG6. Bypass to GA with a 3.3μF high quality ceramic capacitor.
D7	OUT7	The Output of the LDO REG7. Bypass to GA with a 3.3μF high quality ceramic capacitor.
D8	EN6	The Enable Input to the LDO REG6, Active High. This input takes effective only when this IC is enabled.
D9	EN9	The Enable Input to the LDO REG9, Active High. This input takes effective only when this IC is enabled.
E1	GLED	The Ground Node for ODO1, ODO2 and ODO3.
E2	ODO2	The Open Drain Output 2. A current driver output with programmable output current. It could operate in constant current mode, switch on/off mode or PWM mode. The maximum voltage is 6V for this pin.
E3	OUT11	The Output of the LDO REG11. Bypass to GA with a 1μF high quality ceramic capacitor.
E4	INL1011	The Input Node for the LDO REG10 and REG11. Bypass to GA with a 1μF high quality ceramic capacitor.
E5	OUT10	The Output of the LDO REG10. Bypass to GA with a 1.5μF high quality ceramic capacitor.
E6	GP2	The Ground Path of the Step-down DC/DC REG2. Provide the direct ground return path between the internal switch, the external storage capacitor and the input decoupling capacitor. Same function as pin E7. Connect GA, GP1, GP2 and GP3 to a single point as close to the IC as possible.
E7	GP2	The Ground Path of the Step-down DC/DC REG2. Same function as pin E6.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
E8	SW2	The Switch Node of the Step-down DC/DC REG2. Same function as pin E9.
E9	SW2	The Switch Node of the Step-down DC/DC REG2. Same function as pin E8.
F1	GP1	The Ground Path of the Step-down DC/DC REG1. Provide the direct ground return path between the internal switch, the external storage capacitor and the input decoupling capacitor. Same function as pin G3.
F2	ODO1	The Open Drain Output 1. A current driver output with programmable output current. It could operate in constant current mode, switch on/off mode or PWM mode. The maximum voltage is 40V for this pin.
F3	OUT13	The Output of the LDO REG13. Bypass to GA with a 1.5μF high quality ceramic capacitor.
F4	INL1213	The Input Node for the LDO REG12 and REG13. Bypass to GA with a 1μF high quality ceramic capacitor.
F5	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1, GP2 and GP3 to a single point as close to the IC as possible.
F6	REFBP	The Reference Bypass Node. Bypass to GA with a 47nF capacitor for noise suppression and PSRR performance improvement. This pin is discharged to GA in shutdown.
F7	OUT2	The Step-down DC/DC REG2 Feedback Node. Connect it to the output node of REG2.
F8	VP2	The Switch Power Input Node of the Step-down DC/DC REG2. Same function as pin F9.
F9	VP2	The Switch Power Input Node of the Step-down DC/DC REG2. Same function as pin F8.
G1	SW1	The Switch Node of the Step-down DC/DC REG1. Same function as pin G2 and pin H1.
G2	SW1	The Switch Node of the Step-down DC/DC REG1. Same function as pin G1 and pin H1.
G3	GP1	The Ground Path of the Step-down DC/DC REG1. Same function as pin F1.
G4	OUT12	The Output of the LDO REG12. Bypass to GA with a 2.2μF high quality ceramic capacitor.
G5	VSYS	The Internal Bias Bypass. This rail is available all time that this IC works, bypass to GA with a 1μF high quality ceramic capacitor.
G6	VD	The Power Input for Biasing the ADC Circuit. Bypass to GD with a 100nF high quality ceramic capacitor.
G7	XNEG	One of ADC Input, Internally Configured as the Touch Screen Force-Sense Node XNEG with an internal force switch.
G8	YPOS	One of ADC Input, Internally Configured as the Touch Screen Force-Sense Node YPOS with an internal force switch.
G9	YNEG	One of ADC Input, Internally Configured as the Touch Screen Force-Sense Node YNEG with an internal force switch.
H1	SW1	The Switch Node of the Step-down DC/DC REG1. Same function as pin G1 and pin G2.
H2	VP1	The Switch Power Input Node of the Step-down DC/DC REG1. Same function as pin J2.
H3	VSEL	The Output Voltage Selection Input for the Step-down DC/DC REG1. Allow the output voltage of the step-down DC/DC REG1 flies between 2 preset voltages by asserting different logic level at this pin.
H4	SCL	The Clock for the I^2C compatible Serial Interface. Does the same function as the SCL of a normal 400kHz fast I^2C slave device.
H5	SDA	The Data for the I^2C compatible Serial Interface. Does the same function as the SDA of a normal 400kHz fast I^2C slave device.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
H6	VALIVE	The Always-On Low Power LDO Output. Bypass to GA with a 1µF high quality ceramic capacitor.
H7	AUX0	The Auxiliary ADC Input AUX0.
H8	GD	The Ground Node of the ADC Circuit in the IC.
H9	XPOS	One of ADC Input, Internally Configured as the Touch Screen Force-Sense Node XPOS with an internal force switch.
J1	CLK32	The 32kHz Oscillation Output, OD. A pull-up resistor at load end in range of 150kΩ to 300kΩ is recommended.
J2	VP1	The Switch Power Input Node of the Step-down DC/DC REG1. Same function as pin H2.
J3	OUT1	The Step-down DC/DC REG1 Feedback Node. Connect it to the output node of REG1.
J4	XTAL-	The 32kHz Oscillator Crystal Node. This node is pick-up node. Connect it to any terminal of an external crystal.
J5	XTAL+	The 32kHz Oscillator Crystal Node. This node is driving node. Connect it to any terminal of an external crystal.
J6	VBBAT	The Back-up Battery Node. Connect it to the positive node of a back-up battery or storage super cap. The back-up battery charger circuit charges battery or super cap at this node with limited current and outputs a programmable voltage after charging for powering the always-on low power LDO.
J7	AUX1	The Auxiliary ADC Input AUX1.
J8	BBCIN	The Back-up Battery Charger Circuit Input. Bypass to GA with a 1µF high quality ceramic capacitor.
J9	AUX2	The Auxiliary ADC Input AUX2.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
CHGIN to GA (Continuous)	7	V
BATID, TH, ACIN, HFPWR, VSYS and nSTAT to GA	6	
ODO1 to GLED	42	
ODO2, ODO3 to GLED	5	
ON6, ON9, REFBP, BBCIN, VALIVE, VBBAT, XTAL-, XTAL+, CLK32, VSEL, VBAT, CHGLEV, SDA, SCL, PWRHLD, nIRQ, nRSTO, nPBSTAT, nPBIN, OUT1 and OUT2 to GA	6	
XPOS, XNEG, YPOS, YNEG, AUX0, AUX1, AUX2, VD to GD	6	
SW1 to GP1	-0.3 to (VP1 + 0.3)	
SW2 to GP2	-0.3 to (VP2 + 0.3)	
OUT3, SW3, FB3 to any GP3	42	
OUT6 to GA	-0.3 to (INL6 + 0.3)	
OUT7 to GA	-0.3 to (INL7 + 0.3)	
OUT8, OUT9 to GA	-0.3 to (INL89 + 0.3)	
OUT10, OUT11 to GA	-0.3 to (INL1011 + 0.3)	
OUT12, OUT13 to GA	-0.3 to (INL1213 + 0.3)	
Difference between any two ground groups: GP1, GP2, GP3, GLED, GD, GA	-0.3 to + 0.3	
Junction to Ambient Thermal Resistance (θ_{JA})	43	°C/W
Power Dissipation, T_A=25 ˚C	2	W
Power Dissipation Degrading for T_A>25 ˚C	25	mW/°C
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Ambient Temperature range (T_A)	-40 to 85	
Storage Temperature	-55 to 150	
Lead Temperature (soldering for 10 sec.)	300	

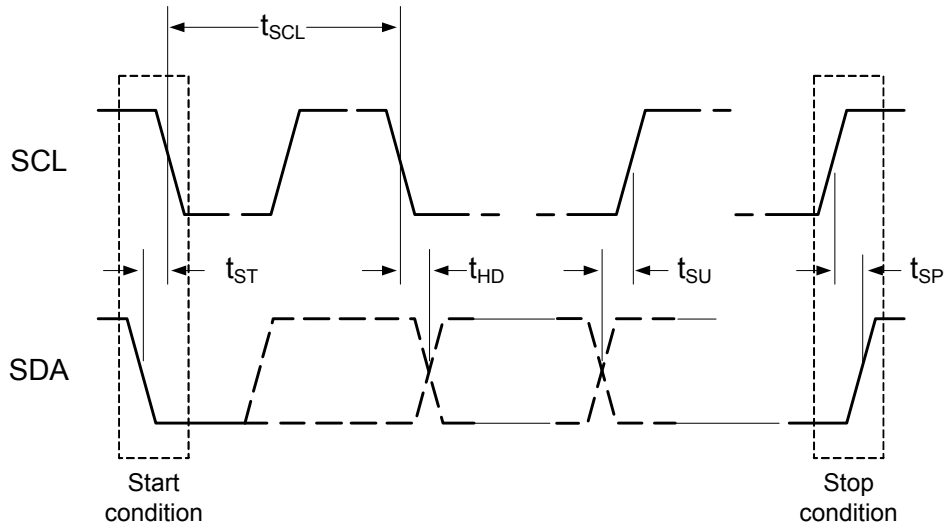
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability. Functional operation at conditions other than the operation conditions specified is not implied. Only one absolute maximum rating should be applied at any time.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.4	V
SCL, SDA Input High	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.4			V
SCL, SDA Leakage Current				1	µA
SDA Output Low	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



Note:
Each session of data transfer is with a start condition, a 7-bits slave address plus a bit to instruct for read or write, followed by an acknowledge bit, a register address byte followed by an acknowledge bit, and a data byte followed by an acknowledge bit and a stop condition. The device address, the register address and the data are all MSB first transferred. Each bit volume is prepared during the SCL is low, is latched-in by the rising edge of the SCL. The data byte is accepted and is put effective by the time that the last bit volume is latched-in.

GLOBAL REGISTER MAP

FUNCTION BLOCK	ADDR.	BITS NAMES AND DEFAULTS							
		D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	TRST	nSYSMODE	nSYSLVMSK	nSYSSTAT	SYSLEV[3]	SYSLEV[2]	SYSLEV[1]	SYSLEV[0]
		0	0	0	R	0	0	0	0
SYS	0x01	EVENT1	EVENT2	EVENT4	RFU	SCRATCH[3]	SCRATCH[2]	SCRATCH[1]	SCRATCH[0]
		0	0	0	0	x	x	x	x
SYS	0x3C	Set to 0x80 before setting nWKALM and RAAI.							
SYS	0x3D	Set to 0x08 before setting nWKALM and RAAI.							
SYS	0x6C	RFU	RFU	STB	STA	RFU	RFU	DATAB	DATAA
		x	x	0	1	x	x	0	0
SYS	0x6D	RFU	RFU	POSB	POSA	RFU	RFU	NEGB	RFU
		x	x	0	1	x	x	0	x
REG1	0x10	x	x	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		0	0	0	1	1	0	0	0
REG1	0x11	x	x	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		0	0	0	1	1	0	0	0
REG1	0x12	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R
REG2	0x20	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	0	0	1	0	0
REG2	0x22	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	1	0	0	0	0	0	R
REG2	0x28	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	0	0	1	0	0
REG2	0x29	x	x	LOWIQ	x	x	x	nFLTMSK	OK
		1	0	1	0	0	0	0	R
REG3	0x30	VSET[7]	VSET[6]	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	1	0	1	0	1	0	0
REG3	0x31	ON	PHASE	RFU	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R
REG4	0x40	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	1	0	1
REG4	0x41	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R
REG5	0x44	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	1	0	1
REG5	0x45	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R

Cont'd in next page.

Note:

SYS: The registers for the system control block; REG1 to REG5: The registers for regulators that generate the OUT1 to OUT5.

RTC: The registers for Real Time Clock block.

RFU is the bit reserved for future use. R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

GLOBAL REGISTER MAP

FUNCTION BLOCK	ADDR.	BITS NAMES AND DEFAULTS							
		D7	D6	D5	D4	D3	D2	D1	D0
REG6	0x48	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	1	0	1
REG6	0x49	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R
REG7	0x4C	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	1	1	0
REG7	0x4D	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R
REG8	0x50	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	0	0	1
REG8	0x51	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R
REG9	0x54	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	0	1	1	0	0	0
REG9	0x55	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R
REG10	0x58	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	1	0	0	1
REG10	0x59	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		1	0	0	0	0	0	0	R
REG11	0x5C	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	0	0	1	0	0
REG11	0x5D	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R
REG12	0x60	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	0	0	1	0	0
REG12	0x61	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R
REG13	0x64	x	x	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		0	0	1	1	0	1	0	0
REG13	0x65	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		0	0	0	0	0	0	0	R

Cont'd in next page.

Note:

REG6 to REG13: The registers for regulators that generate the OUT6 to OUT13.

RFU is the bit reserved for future use. R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

GLOBAL REGISTER MAP

FUNCTION BLOCK	ADDR.	BITS NAMES AND DEFAULTS							
		D7	D6	D5	D4	D3	D2	D1	D0
ODO1	0x70	ISCALE1[1]	ISCALE1[0]	ISET1[5]	ISET1[4]	ISET1[3]	ISET1[2]	ISET1[1]	ISET1[0]
		0	0	0	0	0	0	0	0
ODO1	0x71	DUTY1[7]	DUTY1[6]	DUTY1[5]	DUTY1[4]	DUTY1[3]	DUTY1[2]	DUTY1[1]	DUTY1[0]
		0	0	0	0	0	0	0	0
ODO2	0x73	ISCALE2[1]	ISCALE2[0]	ISET2[5]	ISET2[4]	ISET2[3]	ISET2[2]	ISET2[1]	ISET2[0]
		0	0	0	0	0	0	0	0
ODO2	0x74	DUTY2[7]	DUTY2[6]	DUTY2[5]	DUTY2[4]	DUTY2[3]	DUTY2[2]	DUTY2[1]	DUTY2[0]
		0	0	0	0	0	0	0	0
ODO3	0x76	ISCALE3[1]	ISCALE3[0]	ISET3[5]	ISET3[4]	ISET3[3]	ISET3[2]	ISET3[1]	ISET3[0]
		0	0	0	0	0	0	0	0
ODO3	0x77	DUTY3[7]	DUTY3[6]	DUTY3[5]	DUTY3[4]	DUTY3[3]	DUTY3[2]	DUTY3[1]	DUTY3[0]
		0	0	0	0	0	0	0	0
ODO	0x79	THERMAL_OK	OK1	OK2	OK3	RFU	RFU	RFU	BUFFER
		R	R	R	R	0	0	0	0
RTC	0x80	x	x	SEC[5]	SEC[4]	SEC[3]	SEC[2]	SEC[1]	SEC[0]
		x	x	R	R	R	R	R	R
RTC	0x84	x	x	MIN[5]	MIN[4]	MIN[3]	MIN[2]	MIN[1]	MIN[0]
		x	x	R	R	R	R	R	R
RTC	0x88	x	x	x	HR[4]	HR[3]	HR[2]	HR[1]	HR[0]
		x	x	x	R	R	R	R	R
RTC	0x8C	DAY[7]	DAY[6]	DAY[5]	DAY[4]	DAY[3]	DAY[2]	DAY[1]	DAY[0]
		R	R	R	R	R	R	R	R
RTC	0x8D	DAY[15]	DAY[14]	DAY[13]	DAY[12]	DAY[11]	DAY[10]	DAY[9]	DAY[8]
		R	R	R	R	R	R	R	R
RTC	0x90	x	x	ALMSEC[5]	ALMSEC[4]	ALMSEC[3]	ALMSEC[2]	ALMSEC[1]	ALMSEC[0]
		x	x	0	0	0	0	0	0
RTC	0x94	x	x	ALMMIN[5]	ALMMIN[4]	ALMMIN[3]	ALMMIN[2]	ALMMIN[1]	ALMMIN[0]
		x	x	0	0	0	0	0	0
RTC	0x98	x	x	x	ALMHR[4]	ALMHR[3]	ALMHR[2]	ALMHR[1]	ALMHR[0]
		x	x	x	0	0	0	0	0
RTC	0x9C	CLKSRC	nWKALM	x	x	x	x	x	x
		0	0	0	0	0	0	0	0
RTC	0xA0	x	RCL	RAAI	RDAI	RHAI	RMAI	RSAI	RTCEN
		x	0	0	0	0	0	0	0

Cont'd in next page.

Note:

ODO1 to ODO3: The registers for the open drain driver ODO1 to ODO3; The ODO is the shared register for all the 3 drivers.

RTC: The registers for Real Time Clock block.

RFU is the bit reserved for future use. R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

GLOBAL REGISTER MAP

FUNCTION BLOCK	ADDR.	BITS NAMES AND DEFAULTS							
		D7	D6	D5	D4	D3	D2	D1	D0
RTC	0xA4	x	x	SETSEC[5]	SETSEC[4]	SETSEC[3]	SETSEC[2]	SETSEC[1]	SETSEC[0]
		x	x	0	0	0	0	0	0
RTC	0xA8	x	x	SETMIN[5]	SETMIN[4]	SETMIN[3]	SETMIN[2]	SETMIN[1]	SETMIN[0]
		x	x	0	0	0	0	0	0
RTC	0xAC	x	x	x	SETHR[4]	SETHR[3]	SETHR[2]	SETHR[1]	SETHR[0]
		x	x	x	0	0	0	0	0
RTC	0xB0	SETDAY[7]	SETDAY[6]	SETDAY[5]	SETDAY[4]	SETDAY[3]	SETDAY[2]	SETDAY[1]	SETDAY[0]
		0	0	0	0	0	0	0	0
RTC	0xB1	SETDAY[15]	SETDAY[14]	SETDAY[13]	SETDAY[12]	SETDAY[11]	SETDAY[10]	SETDAY[9]	SETDAY[8]
		0	0	0	0	0	0	0	0
RTC	0xB4	x	x	x	ALMINT	DAYINT	HRINT	MININT	SECINT
		x	x	x	0	0	0	0	0
BBU	0xC8	x	x	VSETBB[5]	VSETBB[4]	VSETBB[3]	VSETBB[2]	VSETBB[1]	VSETBB[0]
		x	x	1	1	0	1	0	1
BBU	0xC9	ONBB	ONRTC	RFU	UNLOCKBB	SCRATCH[3]	SCRATCH[2]	SCRATCH[1]	SCRATCH[0]
		1	1	x	0	0	0	0	0
BBU	0xCA	x	x	VSETRTC[5]	VSETRTC[4]	VSETRTC[3]	VSETRTC[2]	VSETRTC[1]	VSETRTC[0]
		x	x	1	0	0	1	0	0
CHG	0xD0	VSET[3]	VSET[2]	VSET[1]	VSET[0]	ISET[3]	ISET[2]	ISET[1]	ISET[0]
		0	1	0	1	0	1	0	0
CHG	0xD1	SUSCHG	ENVISET	TOTTIMO[1]	TOTTIMO[0]	PRETIMO[1]	PRETIMO[0]	OVPSET[1]	OVPSET[0]
		0	0	0	0	0	0	0	0
CHG	0xD8	TIMR_STAT	TEMP_STAT or BATT_STAT	INPUT_STAT	CHG_STAT	TIMR_DAT	TEMP_DAT or BATT_DAT	INPUT_DAT	CHG_DAT
		0	0	0	0	R	R	R	R
CHG	0xD9	TIMR_PRE	TEMP_POS or BATT_POS	INPUT_POS	CHG_POS	TIMR_TOT	TEMP_NEG or BATT_NEG	INPUT_NEG	CHG_NEG
		0	0	0	0	0	0	0	0
CHG	0xDA	RFU	RFU	CHGSTAT0	CHGSTAT1	RFU	x	x	x
		x	x	R	R	x	x	x	x

Cont'd in next page.

Note:

RTC: The registers for Real Time Clock block; BBU is for the backup battery unit, which includes a backup battery charger and an always-on low power LDO.

RFU is the bit reserved for future use. R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

GLOBAL REGISTER MAP

FUNCTION BLOCK	ADDR.	BITS NAMES AND DEFAULTS							
		D7	D6	D5	D4	D3	D2	D1	D0
TSC ADC	0xF0	nEN	SINGEL	CHANNEL[2]	CHANNEL[1]	CHANNEL[0]	CH03	CH47	ACQ
		1	0	0	0	0	0	0	0
TSC ADC	0xF1	CLEN	PENWKEN	PENSTAT	PENIRQ	DATARDY	nAUTO	PENMSK	DATAMASK
		0	0	R	R	R	1	0	0
TSC ADC	0xE0	XPOS[11]	XPOS[10]	XPOS[9]	XPOS[8]	XPOS[7]	XPOS[6]	XPOS[5]	XPOS[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xE1	XPOS[3]	XPOS[2]	XPOS[1]	XPOS[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xE2	YPOS[11]	YPOS[10]	YPOS[9]	YPOS[8]	YPOS[7]	YPOS[6]	YPOS[5]	YPOS[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xE3	YPOS[3]	YPOS[2]	YPOS[1]	YPOS[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xE4	Z1POS[11]	Z1POS[10]	Z1POS[9]	Z1POS[8]	Z1POS[7]	Z1POS[6]	Z1POS[5]	Z1POS[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xE5	Z1POS[3]	Z1POS[2]	Z1POS[1]	Z1POS[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xE6	Z2POS[11]	Z2POS[10]	Z2POS[9]	Z2POS[8]	Z2POS[7]	Z2POS[6]	Z2POS[5]	Z2POS[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xE7	Z2POS[3]	Z2POS[2]	Z2POS[1]	Z2POS[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xE8	AUX0[11]	AUX0[10]	AUX0[9]	AUX0[8]	AUX0[7]	AUX0[6]	AUX0[5]	AUX0[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xE9	AUX0[3]	AUX0[2]	AUX0[1]	AUX0[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xEA	AUX1[11]	AUX1[10]	AUX1[9]	AUX1[8]	AUX1[7]	AUX1[6]	AUX1[5]	AUX1[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xEB	AUX1[3]	AUX1[2]	AUX1[1]	AUX1[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xEC	AUX2[11]	AUX2[10]	AUX2[9]	AUX2[8]	AUX2[7]	AUX2[6]	AUX2[5]	AUX2[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xED	AUX2[3]	AUX2[2]	AUX2[1]	AUX2[0]	x	x	x	x
		x	x	x	x	x	x	x	x
TSC ADC	0xEE	AUX3[11]	AUX3[10]	AUX3[9]	AUX3[8]	AUX3[7]	AUX3[6]	AUX3[5]	AUX3[4]
		x	x	x	x	x	x	x	x
TSC ADC	0xEF	AUX3[3]	AUX3[2]	AUX3[1]	AUX3[0]	x	x	x	x
		x	x	x	x	x	x	x	x

Note:

RFU is the bit reserved for future use. R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
SYS	0x00	7	TRST	0	W/R	Reset Timer Setting. Defines the reset time-out threshold. Reset time-out is 65ms when value is 1, reset time-out is 260ms when value is 0.
		6	nSYSMODE	0	W/R	SYSLEV Mode Select. Defines the response to the SYSLEV voltage detector, 0: automatic shut down when V_{VSYS} falls below the programmed V_{SYSLEV} threshold, 1: Generate an interrupt when V_{VSYS} falls below the programmed V_{SYSLEV} threshold.
		5	nSYSLVMSK	0	W/R	System Voltage Level Interrupt Mask. SYSLEV interrupt is masked by default, set to 1 to unmask this interrupt.
		4	nSYSSTAT	0	R	V_{VSYS} Status Indication. Value is 0 when V_{VSYS} > VSYSLEV, value is 1 when V_{VSYS} < VSYSLEV.
		3	SYSLEV[3]	0	W/R	4 bits to set the threshold of V_{SYSLEV}. SYSLEV[3:0] = 0000 is for 2.2V. The voltage is linear coded with LSB for 0.1V in the range of 2.2V to 3.7V, where LSB is SYSLEV[0]. The hysteresis is 0.2V in rising. The setting is effective only when V_{VSYS} > V_{UVLO}.
		2	SYSLEV[2]	0		
		1	SYSLEV[1]	0		
		0	SYSLEV[0]	0		
	0x01	7	EVENT1	0	WE/R	For internal use only.
		6	EVENT2	0	WE/R	For internal use only.
		5	EVENT4	0	W/R	Write 1 to enable the sleep mode of REG2, 0 to enable the normal buck mode operation of REG2.
		4	RFU	0	WE/R	For internal use only.
		3	SCRATCH[3]	x	W/R	4 bits scratch register for the equipment system to use. Data in those bits are kept until the VSYS loses.
		2	SCRATCH[2]	x		
		1	SCRATCH[1]	x		
		0	SCRATCH[0]	x		
	0x3C	[7:0]			W/R	Set to 0x80 before setting nWKALM and RAAI.
	0x3D	[7:0]				Set to 0x08 before setting nWKALM and RAAI.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
SYS	0x6C	7	RFU	x	WE/R	Reserved for future use.
		6	RFU	x	WE/R	Reserved for future use.
		5	STB	0	W/R	Write and read for different functions, as flag bit or mask bit, for the HFPWR assertion interrupt. Write 1 allow interrupt, write 0 mask interrupt; Read 1 when interrupt asserted, 0 if no interrupt. Also see DATAB[ ], POSB[ ] and NEGB[ ] for the status and conditions.
		4	STA	1	W/R	Write and read for different functions, as flag bit or mask bit, for the "enable key" push-button assertion interrupt. Write 1 allow interrupt, write 0 mask interrupt; Read 1 when interrupt asserted, 0 if no interrupt. Also see DATAA[ ], POSA[ ] for the status and conditions.
		3	RFU	x	WE/R	Reserved for future use.
		2	RFU	x	WE/R	Reserved for future use.
		1	DATAB	0	W/R	This bit needs to be set 1 for asserting interrupt when HFPWR asserted.
		0	DATAA	0	W/R	This bit needs to be set 1 for asserting interrupt when "enable key" asserted.
	0x6D	7	RFU	x	WE/R	Reserved for future use.
		6	RFU	x	WE/R	Reserved for future use.
		5	POSB	0	W/R	This bit needs to be set 1 for asserting interrupt when HFPWR asserted.
		4	POSA	1	W/R	This bit needs to be set 1 for asserting interrupt when "enable key" asserted.
		3	RFU	x	WE/R	Reserved for future use.
		2	RFU	x	WE/R	Reserved for future use.
		1	NEGB	0	W/R	This bit needs to be set 1 for asserting interrupt when HFPWR de-asserted.
		0	RFU	x	WE/R	Reserved for future use.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG1	0x10	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET0[5]	0	W/R	Voltage Setting for the REG1 output when VSEL=0. Default setting is 1.2V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET0[4]	1	W/R	
		3	VSET0[3]	1	W/R	
		2	VSET0[2]	0		
		1	VSET0[1]	0		
		0	VSET0[0]	0		
	0x11	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET1[5]	0	W/R	Voltage Setting for the REG1 when VSEL=1. Default setting is 1.2V（This voltage setting is also known as "Standby Voltage"). Refer to the STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING table for details.
		4	VSET1[4]	1	W/R	
		3	VSET1[3]	1	W/R	
		2	VSET1[2]	0		
		1	VSET1[1]	0		
		0	VSET1[0]	0		
	0x12	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	PHASE	0	W/R	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, set bit to 0 for the regulator to operate in phase with the oscillator.
		5	MODE	0	W/R	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM mode under all load conditions, set bit to 0 to allow PFM mode under light-load conditions.
		4	DELAY[2]	0	W/R	Regulator Turn-on Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100μs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG2	0x20	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the buck regulation part of the REG2, which is active in normal mode (Refer to byte 0x28 for REG2 output voltage in sleep mode). Default setting is 1.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	0	W/R	
		3	VSET[3]	0	W/R	
		2	VSET[2]	1	W/R	
		1	VSET[1]	0	W/R	
		0	VSET[0]	0	W/R	
	0x22	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	PHASE	1	W/R	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, set bit to 0 for the regulator to operate in phase with the oscillator.
		5	MODE	0	W/R	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM mode under all load conditions, set bit to 0 to allow PFM mode under light -load conditions.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0	W/R	
		2	DELAY[0]	0	W/R	
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
	0x28	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the linear regulation part of the REG2, which is active in sleep mode. Default setting is 1.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	0	W/R	
		3	VSET[3]	0	W/R	
		2	VSET[2]	1	W/R	
		1	VSET[1]	0	W/R	
		0	VSET[0]	0	W/R	
	0x29	7	x	1	WE/R	Not used.
		6	x	0	WE/R	
		5	LOWIQ	1	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode. If it is set to 1, the backup battery charger stops in the deep sleep mode.
		4	x	0	x	Not used.
		3	x	0	x	Not used.
		2	x	0	x	Not used.
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	0	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG3	0x30	7	VSET[7]	0	W/R	Voltage Setting for the REG3 output. Default setting is 5V. Refer to the table of *STEP-UP DC/DC VOLTAGE SETTING* for details.
		6	VSET[6]	1		
		5	VSET[5]	0		
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	0		
	0x31	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	PHASE	0	W/R	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, set bit to 0 for the regulator to operate in phase with the oscillator.
		5	RFU	0	WE/R	Reserved for future use.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	W/R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG4	0x40	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG4 output. Default setting is 2.9V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	1		
	0x41	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
REG5	0x44	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG5 output. Default setting is 2.9V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	1		
	0x45	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG6	0x48	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG6 output. Default setting is 2.9V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	1		
	0x49	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
REG7	0x4C	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG7 output. Default setting is 3.0V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	1		
		0	VSET[0]	0		
	0x4D	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG8	0x50	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG8 output. Default setting is 2.5V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	0		
		1	VSET[1]	0		
		0	VSET[0]	1		
	0x51	7	ON	1	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
REG9	0x54	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	0	W/R	Voltage Setting for the REG9 output. Default setting is 1.2V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	1		
		2	VSET[2]	0		
		1	VSET[1]	0		
		0	VSET[0]	0		
	0x55	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100µs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG10	0x58	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG10 output. Default setting is 3.3V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	1		
		2	VSET[2]	0		
		1	VSET[1]	0		
		0	VSET[0]	1		
	0x59	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100μs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
REG11	0x5C	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG11 output. Default setting is 1.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	0		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	0		
	0x5D	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100μs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
REG12	0x60	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG12 output. Default setting is 1.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	0		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	0		
	0x61	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100μs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.
REG13	0x64	7	x	0	W/R	For internal use only.
		6	x	0	W/R	
		5	VSET[5]	1	W/R	Voltage Setting for the REG13 output. Default setting is 2.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSET[4]	1		
		3	VSET[3]	0		
		2	VSET[2]	1		
		1	VSET[1]	0		
		0	VSET[0]	0		
	0x65	7	ON	0	W/R	Regulator On/Off Bit. Set bit to 1 to turn on the regulator, set bit to 0 to turn off the regulator.
		6	DIS	0	W/R	Output Discharge Control. Set bit to 1 to discharged the LDO output to GA through 1.5kΩ resistor when in shutdown.
		5	LOWIQ	0	W/R	LDO Low-IQ Mode Control. Set bit to 1 for low quiescent current mode, set bit to 0 for normal mode.
		4	DELAY[2]	0	W/R	Regulator Turn-On Delay Control. DELAY[2:0]=000 for no delay. Other code to delay relationship: 001 for 2ms, 010 for 4ms, 011 for 8ms, 100 for 16ms, 101 for 32ms, 110 for 64ms and 111 for 128ms. There is a propagation delay for about 100μs if selecting no delay.
		3	DELAY[1]	0		
		2	DELAY[0]	0		
		1	nFLTMSK	0	W/R	Regulator Fault Interrupt Mask. Set bit to 1 to enable fault-interrupt when the output is out of regulation, set bit to 0 to disable fault-interrupt.
		0	OK	R	R	Regulator Power-OK Status. Value is 0 when the output is out of regulation, value is 1 when the output is in regulation.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
ODO1	0x70	7	ISCALE1[1]	0	W/R	Set the LSB weight of the linear current setting of the open-drain driver. [1:0]=00 for 0.4mA, 01 for 0.8mA, 10 for 1.2mA, 11 for 1.6mA.
		6	ISCALE1[0]	0		
		5	ISET1[5]	0	W/R	Driver output current setting in linear code, no offset. [5:0]=0 for 0mA output. Full scale output currents are 25.2mA, 50.4mA, 75.6mA and 100.8mA respectively with different LSB weights.
		4	ISET1[4]	0		
		3	ISET1[3]	0		
		2	ISET1[2]	0		
		1	ISET1[1]	0		
		0	ISET1[0]	0		
	0x71	7	DUTY1[7]	0	W/R	PWM duty setting. [7:0]=0x00 for 0%, [7:0]=0xFF for 100%. For linear duty setting option, the LSB weight is 0.4% for code 0x00 to 0xFE, which is 0% to 99.2% of duty. The code 0xFF is forced for 100% duty. For the non-linear duty setting option, refer to the table of NON-LINEAR DUTY SETTING for code to duty cross.
		6	DUTY1[6]	0		
		5	DUTY1[5]	0		
		4	DUTY1[4]	0		
		3	DUTY1[3]	0		
		2	DUTY1[2]	0		
		1	DUTY1[1]	0		
		0	DUTY1[0]	0		
ODO2	0x73	7	ISCALE2[1]	0	W/R	Set the LSB weight of the linear current setting of the open-drain driver. [1:0]=00 for 0.4mA, 01 for 0.8mA, 10 for 1.2mA, 11 for 1.6mA.
		6	ISCALE2[0]	0		
		5	ISET2[5]	0	W/R	Driver output current setting in linear code, no offset. [5:0]=0 for 0mA output. Full scale output currents are 25.2mA, 50.4mA, 75.6mA and 100.8mA respectively with different LSB weights.
		4	ISET2[4]	0		
		3	ISET2[3]	0		
		2	ISET2[2]	0		
		1	ISET2[1]	0		
		0	ISET2[0]	0		
	0x74	7	DUTY2[7]	0	W/R	PWM duty setting. [7:0]=0x00 for 0%, [7:0]=0xFF for 100%. For linear duty setting option, the LSB weight is 0.4% for code 0x00 to 0xFE, which is 0% to 99.2% of duty. The code 0xFF is forced for 100% duty. For the non-linear duty setting option, refer to the table of NON-LINEAR DUTY SETTING for code to duty cross.
		6	DUTY2[6]	0		
		5	DUTY2[5]	0		
		4	DUTY2[4]	0		
		3	DUTY2[3]	0		
		2	DUTY2[2]	0		
		1	DUTY2[1]	0		
		0	DUTY2[0]	0		

Note:

W/R: Write and read accessible.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
ODO3	0x76	7	ISCALE3[1]	0	W/R	Set the LSB weight of the linear current setting of the open-drain driver. [1:0]=00 for 0.4mA, 01 for 0.8mA, 10 for 1.2mA, 11 for 1.6mA.
		6	ISCALE3[0]	0		
		5	ISET3[5]	0	W/R	Driver output current setting in linear code, no offset. [5:0]=0 for 0mA output. Full scale output currents are 25.2mA, 50.4mA, 75.6mA and 100.8mA respectively with different LSB weights.
		4	ISET3[4]	0		
		3	ISET3[3]	0		
		2	ISET3[2]	0		
		1	ISET3[1]	0		
		0	ISET3[0]	0		
	0x77	7	DUTY3[7]	0	W/R	PWM duty setting. [7:0]=0x00 for 0%, [7:0]=0xFF for 100%. For linear duty setting option, the LSB weight is 0.4% for code 0x00 to 0xFE, which is 0% to 99.2% of duty. The code 0xFF is forced for 100% duty. For the non-linear duty setting option, refer to the table of NON-LINEAR DUTY SETTING for code to duty cross.
		6	DUTY3[6]	0		
		5	DUTY3[5]	0		
		4	DUTY3[4]	0		
		3	DUTY3[3]	0		
		2	DUTY3[2]	0		
		1	DUTY3[1]	0		
		0	DUTY3[0]	0		
ODO	0x79	7	THERMAL_OK	1	R	Driver circuit over temperature indicator. This bit is cleared to 0 if the driver circuit over temperature happens.
		6	OK1	0	R	Indicator for ODO1 out current of regulation (open LED detected).
		5	OK2	0	R	Indicator for ODO2 out current of regulation (open LED detected).
		4	OK3	0	R	Indicator for ODO3 out current of regulation (open LED detected).
		3	RFU	1	R	Reserved for future use.
		2	RFU	0	W/R	Reserved for future use.
		1	RFU	0	W/R	Reserved for future use.
		0	BUFFER	0	W/R	Set 1 to select data buffers. Buffered data is updated to each output simultaneously when this bit is cleared to 0, for synchronized output.

Note:

W/R: Write and read accessible. R: Read accessible, writing to the bit does not make change to the volume. WE/R: Write and read accessible, write exact what it is before to avoid unexpected behavior. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
RTC	0x80	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	SEC[5]	0	R	RTC seconds data, mod 60, SEC[0] is the LSB.
		4	SEC[4]	0		
		3	SEC[3]	0		
		2	SEC[2]	0		
		1	SEC[1]	0		
		0	SEC[0]	0		
	0x84	7	x	x	x	Not used.
		6	x	x	R	RTC hours data, mod 24, HR[0] is the LSB.
		5	MIN[5]	0	R	RTC hours data, mod 24, HR[0] is the LSB.
		4	MIN[4]	0		
		3	MIN[3]	0		
		2	MIN[2]	0		
		1	MIN[1]	0		
		0	MIN[0]	0		
	0x88	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	x	x	x	Not used.
		4	HR[4]	0	R	RTC hours data, mod 24, HR[0] is the LSB.
		3	HR[3]	0		
		2	HR[2]	0		
		1	HR[1]	0		
		0	HR[0]	0		
	0x8C	7	DAY[7]	0	R	Elapsed days counter, the lower byte of the 16 bits counter. DAY[0] is the LSB.
		6	DAY[6]	0		
		5	DAY[5]	0		
		4	DAY[4]	0		
		3	DAY[3]	0		
		2	DAY[2]	0		
		1	DAY[1]	0		
		0	DAY[0]	0		

Note:

R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
RTC	0x8D	7	DAY[15]	0	R	Elapsed days counter, the upper byte of the 16 bits counter. DAY[15] is the MSB.
		6	DAY[14]	0		
		5	DAY[13]	0		
		4	DAY[12]	0		
		3	DAY[11]	0		
		2	DAY[10]	0		
		1	DAY[9]	0		
		0	DAY[8]	0		
	0x90	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	ALMSEC[5]	0	W/R	The hours of the alarm time setting, mod 24. The ALMHR[0] is the LSB.
		4	ALMSEC[4]	0		
		3	ALMSEC[3]	0		
		2	ALMSEC[2]	0		
		1	ALMSEC[1]	0		
		0	ALMSEC[0]	0		
	0x94	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	ALMMIN[5]	0	W/R	The minutes of the alarm time setting, mod 60. The ALMMIN[0] is the LSB.
		4	ALMMIN[4]	0		
		3	ALMMIN[3]	0		
		2	ALMMIN[2]	0		
		1	ALMMIN[1]	0		
		0	ALMMIN[0]	0		
	0x98	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	x	x	x	Not used.
		4	ALMHR[4]	0	W/R	The hours of the alarm time setting, mod 24. The ALMHR[0] is the LSB.
		3	ALMHR[3]	0		
		2	ALMHR[2]	0		
		1	ALMHR[1]	0		
		0	ALMHR[0]	0		

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
RTC	0x9C	7	CLKSRC	0	W/R	Set 0 for using the xtal oscillator; Set 1 for using the buck switch clock.
		6	nWKALM	0	W/R	Set 0 for enabling alarm against time match. Register 0x3C and 0x3D need to be set 0x80 and 0x08 previous to setting this bit.
		5	x	0	x	Not used.
		4	x	0	x	Not used.
		3	x	0	x	Not used.
		2	x	0	x	Not used.
		1	x	0	x	Not used.
		0	x	0	x	Not used.
	0xA0	7	x	x	x	Not used.
		6	RCL	0	W/R	Set 1 to load RTC with the data stored in all setting registers by its 0 to 1 transition.
		5	RAAI	0	W/R	Set 1 for enabling RTC alarm. Register 0x3C and 0x3D need to be set 0x80 and 0x08 previous to setting this bit.
		4	RDAI	0	W/R	Set 1 for interrupt assertion for 1s when day count changes.
		3	RHAI	0	W/R	Set 1 for interrupt assertion for 1s when hours count changes.
		2	RMAI	0	W/R	Set 1 for interrupt assertion for 1s when minute count changes.
		1	RSAI	0	W/R	Set 1 for interrupt assertion for 0.5s when second count changes.
		0	RTCEN	0	W/R	Set 1 to enable the RTC, set 0 to disable the RTC. This bit is cleared to 0 when the RTC power losses.
	0xA4	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	SETSEC[5]	0	W/R	Setting register for seconds. Store the seconds into this register firstly, then set the RCL[ ] to 1 to load the RTC.
		4	SETSEC[4]	0	W/R	
		3	SETSEC[3]	0	W/R	
		2	SETSEC[2]	0	W/R	
		1	SETSEC[1]	0	W/R	
		0	SETSEC[0]	0	W/R	
	0xA8	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	SETMIN[5]	0	W/R	Setting register for minutes. Store the minutes into this register firstly, then set the RCL[ ] to 1 to load the RTC.
		4	SETMIN[4]	0	W/R	
		3	SETMIN[3]	0	W/R	
		2	SETMIN[2]	0	W/R	
		1	SETMIN[1]	0	W/R	
		0	SETMIN[0]	0	W/R	

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
RTC	0xAC	7	x	x	x	Not used.
		6	x	x		
		5	x	x		
		4	SETHR[4]	0	W/R	Setting register for hours. Store the hours into this register firstly, then set the RCL[ ] to 1 to load the RTC.
		3	SETHR[3]	0		
		2	SETHR[2]	0		
		1	SETHR[1]	0		
		0	SETHR[0]	0		
	0xB0	7	SETDAY[7]	0	W/R	Setting register for the elapsed days. Store the lower byte of days into this register firstly, then set the RCL[ ] to 1 to load the RTC. The SETDAY[0] is the LSB of the days word.
		6	SETDAY[6]	0		
		5	SETDAY[5]	0		
		4	SETDAY[4]	0		
		3	SETDAY[3]	0		
		2	SETDAY[2]	0		
		1	SETDAY[1]	0		
		0	SETDAY[0]	0		
	0xB1	7	SETDAY[15]	0	W/R	Setting register for the elapsed days. Store the upper byte of days into this register firstly, then set the RCL[ ] to 1 to load the RTC. The SETDAY[15] is the MSB of the days word.
		6	SETDAY[14]	0		
		5	SETDAY[13]	0		
		4	SETDAY[12]	0		
		3	SETDAY[11]	0		
		2	SETDAY[10]	0		
		1	SETDAY[9]	0		
		0	SETDAY[8]	0		
	0xB4	7	x	x	x	Not used.
		6	x	x	x	Not used.
		5	x	x	x	Not used.
		4	ALMINT	0	W/R	Interrupt flag. Read 1 if timing alarm asserted. Write 0 to clear.
		3	DAYINT	0	W/R	Interrupt flag. Read 1 if timing alarm asserted. Write 0 to clear.
		2	HRINT	0	W/R	Interrupt flag. Read 1 if timing alarm asserted. Write 0 to clear.
		1	MININT	0	W/R	Interrupt flag. Read 1 if timing alarm asserted. Write 0 to clear.
		0	SECINT	0	W/R	Interrupt flag. Read 1 if every second alarm asserted, Write 0 to clear.

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
BBU	0xC8	7	x	0	W/R	For internal use only.
		6	x	0	W/R	For internal use only.
		5	VSETBB[5]	1	W/R	Voltage setting for back-up battery charger, default 2.7V. This byte only could be written when the UNLOCBB is set to 1. Refer to the table of *VBBAT VOLTAGE SETTINGS* for details.
		4	VSETBB[4]	1		
		3	VSETBB[3]	0		
		2	VSETBB[2]	1		
		1	VSETBB[1]	0		
		0	VSETBB[0]	1		
	0xC9	7	ONBB	1	W/R	Set 1 enable, set 0 disable the back-up battery charger.
		6	ONRTC	1	W/R	Set 1 enable the always-on LDO, which powers the RTC block. Set 0 disable the always-on LDO for saving power when not used.
		5	RFU	0	WE/R	Reserved for future use.
		4	UNLOCKBB	0	W/R	Set 1 to allow change the back-up battery charger output voltage.
		3	SCRATCH[3]	x	W/R	4 bits register for the equipment system to use. Data in those bits are kept until both the main battery and back-up battery loses.
		2	SCRATCH[2]	x		
		1	SCRATCH[1]	x		
		0	SCRATCH[0]	x		
	0xCA	7	x	0	W/R	For internal use only.
		6	x	0	W/R	For internal use only.
		5	VSETRTC[5]	1	W/R	Always-on LDO output voltage setting, default is 1.8V. Refer to the *STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING* table for details.
		4	VSETRTC[4]	0		
		3	VSETRTC[3]	0		
		2	VSETRTC[2]	1		
		1	VSETRTC[1]	0		
		0	VSETRTC[0]	0		
CHG	0xD0	7	VSET[3]	0	W/R	Battery regulation voltage setting for the voltage output in the top-off state. The ENVISET[ ] has to be set to 1 for changing these bits. Refer to the table of CHARGER VOLTAGE SETTING for details.
		6	VSET[2]	1		
		5	VSET[1]	0		
		4	VSET[0]	1		
		3	ISET[3]	0	W/R	Fast charge current setting for the maximum current for fast charge. The ENVISET[ ] has to be set to1 for changing these bits. Refer to the table of FAST CHARGING CURRENT SETTING for details.
		2	ISET[2]	1		
		1	ISET[1]	0		
		0	ISET[0]	0		

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
CHG	0xD1	7	SUSCHG	0	W/R	Set 1 to force the charger into suspend state. Set 0 to allow charging.
		6	ENVISET	0	W/R	Set 1 to enable the changes to charger voltage and current settings.
		5	TOTTIMO[1]	0	W/R	Entire cycle safe timer time-out setting. [1:0]=00 for 180 minutes, 01 for 240 minutes, 10 for 300 minutes and 11 for no time-out.
		4	TOTTIMO[0]	0	W/R	Entire cycle safe timer time-out setting. [1:0]=00 for 180 minutes, 01 for 240 minutes, 10 for 300 minutes and 11 for no time-out.
		3	PRETIMO[1]	0	W/R	Pre-condition safe timer time-out setting. [1:0]=00 for 40 minutes, 01 for 60 minutes, 10 for 80 minutes and 11 for no time-out.
		2	PRETIMO[0]	0	W/R	Pre-condition safe timer time-out setting. [1:0]=00 for 40 minutes, 01 for 60 minutes, 10 for 80 minutes and 11 for no time-out.
		1	OVPSET[1]	1	W/R	Over-voltage thresholds setting, [1:0]=00 for 6.3V, 01 for 6.5V, 10 for 6.7V and 11 for 6.9V.
		0	OVPSET[0]	0	W/R	Over-voltage thresholds setting, [1:0]=00 for 6.3V, 01 for 6.5V, 10 for 6.7V and 11 for 6.9V.
	0xD8	7	TIMR_STAT	0	W/R	Charge Time-out Interrupt Flag/Mask. Write this bit with TIMR_PRE[ ] and/or TIMR_TOT[ ] to 1 to allow interrupt when charge safety timers expire. Read this bit to get charge time-out interrupt status, read back value is 1 when interrupt is generated and it is automatically cleared to 0 upon reading, read back value is 0 when no interrupt is generated. Also see TIMR_DAT[ ], TIMR_PRE[ ] and TIMR_TOT[ ].
		6	TEMP_STAT or BATT_STAT	0	W/R	Battery Temperature or Battery Installation Detection Interrupt Flag/ Mask. Write this bit with TEMP_POS[ ] (BATT_POS[ ]) or/and TEMP_NEG[ ] (BATT_NEG[ ]) to 1 to allow interrupt when a battery temperature event occurs or a battery installation event occurs. Read this bit to get the battery temperature or battery installation detection Interrupt status, read back value is 1 when interrupt is generated and it is automatically cleared to 0 upon reading, read back value is 0 when no interrupt is generated. Also see TEMP_DAT[ ], BATT_DAT[ ], TEMP_POS[ ], TEMP_NEG[ ], BATT_POS[ ] and BATT_NEG[ ].
		5	INPUT_STAT	0	W/R	Input Voltage Interrupt Flag/Mask. Write this bit with INPUT_POS[ ] or/ and INPUT_NEG[ ] to 1 to allow interrupt when CHGIN UVLO or OVP condition occurs. Read this bit to get input voltage interrupt status, read back value is 1 when interrupt is generated and it is automatically cleared to 0 upon reading, read back value is 0 when no interrupt is generated. Also see INPUT_DAT[ ], INPUT_POS[ ] and INPUT_NEG[ ].
		4	CHG_STAT	0	W/R	Charge State Interrupt Flag/Mask. Write this bit with CHG_POS[ ] or/and CHG_NEG[ ] to 1 to allow interrupt when the state machine gets in or out of EOC state. Read this bit to get the EOC state interrupt status, read back value is 1 when interrupt is generated and it is automatically cleared to 0 upon reading, read back value is 0 when no interrupt is generated. Also see CHG_DAT[ ], CHG_POS[ ] and CHG_NEG[ ].
		3	TIMR_DAT	0	R	Charge Timer Status. Value is 1 when precondition time-out or total charge time-out occurs. Value is 0 in other cases.
		2	TEMP_DAT or BATT_DAT	0	R	Temperature or Battery Installation Status. Value is 1 when battery temperature is inside of valid range or battery installation is detected. Value is 0 in other cases.
		1	INPUT_DAT	0	R	Input Voltage Detection Status. Value is 1 when CHGIN voltage is valid, value is 0 when CHGIN voltage is not valid. The valid range is $V_{UVLO}<V_{CHGIN}<V_{OVP}$.
		0	CHG_DAT	0	R	Charge State Machine Status. Value is 1 when the charger state machine is in EOC state. Value is 0 in other cases.

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
CHG	0xD9	7	TIMR_PRE	0	W/R	Pre-charge Time-out Interrupt Mask. Set both this bit and TIMR_STAT[ ] to 1 to allow interrupt when a Pre-charge time-out event occurs.
		6	TEMP_POS or BATT_POS	0	W/R	Battery Temperature or Battery Installation Detection Interrupt Mask. Write this bit with TEMP_STAT[ ] (BATT_STAT[ ]) to 1 to allow interrupt when the main battery temperature goes into the valid range or when the main battery is being installed.
		5	INPUT_POS	0	W/R	Input Voltage Interrupt Mask. Write this bit with INPUT_STAT[ ] to 1 to allow interrupt when CHGIN input voltage goes into the valid range. The valid range is $V_{UVLO}<V_{CHGIN}<V_{OVP}$.
		4	CHG_POS	0	W/R	Charge State Interrupt Mask. Write this bit with CHG_STAT[ ] to 1 to allow interrupt when the state machine gets in the EOC state.
		3	TIMR_TOT	0	W/R	Total Charge Time-out Interrupt Mask. Set both this bit and TIMR_STAT[ ] to 1 to allow interrupt when a total charge time-out event occurs.
		2	TEMP_NEG or BATT_NEG	0	W/R	Battery Temperature or Battery Installation Detection Interrupt Mask. Write this bit with TEMP_STAT[ ] (BATT_STAT[ ]) to 1 to allow interrupt when the main battery temperature goes out of the valid range or when the main battery is being removed.
		1	INPUT_NEG	0	W/R	Input Voltage Interrupt Mask. Write this bit with INPUT_STAT[ ] to 1 to allow interrupt when CHGIN input voltage goes out of the valid range. The valid range is $V_{UVLO}<V_{CHGIN}<V_{OVP}$.
		0	CHG_NEG	0	W/R	Charge State Interrupt Mask. Write this bit with CHG_STAT[ ] to 1 to allow interrupt when the state machine gets out of the EOC state.
	0xDA	7	RFU	x	WE/R	Reserved for future use.
		6	RFU	x	WE/R	Reserved for future use.
		5	CHGSTAT0	0	R	Charger Status. [1:0]=00, charger is off for forced suspend, time-out fault, battery temperature invalid, and operation in LDO mode; 01 is for in Sleep state; 10 is for in the Fast-Charge state, the Top-off state; 11 is for in the Pre-condition state.
		4	CHGSTAT1	0	R	
		3	RFU	x	R	Reserved for future use.
		2	x	x	x	Not used.
		1	x	x	x	Not used.
		0	x	x	x	Not used.

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
TSC ADC	0xF0	7	nEN	1	W/R	Set bit to 0 to enable the TSC ADC block, set bit to 1 to disable it.
		6	SINGLE	0	W/R	Set bit to 1 for one channel only acquisition, set bit to 0 for multi-channel scanning.
		5	CHANNEL[2]	0	W/R	Specify which channel to measure for one channel only acquisition. Channel[2:0]=0 for X-coordinate position, 1 for Y-coordinate position, 2 for Z-coordinate position 1, 3 for Z-coordinate position 2, 4 for AUX0, 5 for AUX1, 6 for AUX2 and 7 for AUX3.
		4	CHANNEL[1]	0		
		3	CHANNEL[0]	0		
		2	CH03	0	W/R	Set bit to 1 for scanning channel 0 to channel 3, set bit to 0 for not scanning. Refer to the *REGISTER AND BIT DESCRIPTIONS* section for CHANNEL[2], CHANNEL[1] and CHANNEL[0] for channel coding.
		1	CH47	0	W/R	Set bit to 1 for scanning channel 4 to channel 7, set bit to 0 for not scanning. Refer to the *REGISTER AND BIT DESCRIPTIONS* section descriptions for CHANNEL[2], CHANNEL[1] and CHANNEL[0] for channel coding.
		0	ACQ	0	W/R	Write and read for different functions. Set bit from 0 to 1 initializes an acquisition procedure designated by the SINGLE, CHANNEL[2:0] or CH03, CH47.
	0xF1	7	CLEN	0	W/R	Data Length of Conversion. Set bit to 0 for 12 bits, set bit to 1 for 8 bits.
		6	PENWKEN	0	W/R	Pen Entry Wake-up Enable. Set bit to 1 to allow waking-up against pen entry.
		5	PENSTAT	R	R	Pen Touch Detection Instant Status. Read back value is 1 for in touching, read back value is 0 for no touching.
		4	PENIRQ	R	R	Pen Touch Detection Interrupt Status. Read back value is 1 when a pen touch interrupt is generated and it is automatically cleared to 0 upon reading. Read back value is 0 when no interrupt is generated.
		3	DATARDY	R	R	Data Ready Interrupt Status. Read back value is 1 when the data ready interrupt is generated and it is automatically cleared to 0 upon reading. Read back value is 0 when no interrupt generated. To start a new conversion, this bit must be cleared to 0.
		2	nAUTO	1	W/R	Acquisition Starting Mode Setting. Set bit to 1 for starting acquisition by when the ACQ bit is set 1. Set bit to 0 for automatic starting by when pen touch is detected. The interrupt asserts only when the acquisition completes and the data is ready.
		1	PENMASK	0	W/R	Write or read for different functions. Pen Touch Interrupt Mask. Set bit to 1 to mask the pen touch detection interrupt, set bit to 0 to allow pen touch detection interrupt.
		0	DATAMASK	0	W/R	Write or read for different functions. Data Ready Interrupt Mask. Set bit to 1 to mask the data ready interrupt, set bit to 0 to allow data ready interrupt.

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
TSC ADC	0xE0	7	XPOS[11]	0	R	X-coordinate position. [11] is the MSB. Force drive voltage and full range input is same as internal 2.5V reference voltage.
		6	XPOS[10]	0		
		5	XPOS[9]	0		
		4	XPOS[8]	0		
		3	XPOS[7]	0		
		2	XPOS[6]	0		
		1	XPOS[5]	0		
		0	XPOS[4]	0		
	0xE1	7	XPOS[3]	0	R	X-coordinate position. [0] is the LSB.
		6	XPOS[2]	0		
		5	XPOS[1]	0		
		4	XPOS[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				
	0xE2	7	YPOS[11]	0	R	Y-coordinate position. [11] is the MSB. Force drive voltage and full range input is same as internal 2.5V reference voltage.
		6	YPOS[10]	0		
		5	YPOS[9]	0		
		4	YPOS[8]	0		
		3	YPOS[7]	0		
		2	YPOS[6]	0		
		1	YPOS[5]	0		
		0	YPOS[4]	0		
	0xE3	7	YPOS[3]	0	R	Y-coordinate position. [0] is the LSB.
		6	YPOS[2]	0		
		5	YPOS[1]	0		
		4	YPOS[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
TSC ADC	0xE4	7	Z1POS[11]	0	R	Z-coordinate position 1. [11] is the MSB. Force drive voltage and full range input is same as internal 2.5V reference voltage.
		6	Z1POS[10]	0		
		5	Z1POS[9]	0		
		4	Z1POS[8]	0		
		3	Z1POS[7]	0		
		2	Z1POS[6]	0		
		1	Z1POS[5]	0		
		0	Z1POS[4]	0		
	0xE5	7	Z1POS[3]	0	R	Z-coordinate position 1. [0] is the MSB.
		6	Z1POS[2]	0		
		5	Z1POS[1]	0		
		4	Z1POS[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				
	0xE6	7	Z2POS[11]	0	R	Z-coordinate position 2. [11] is the MSB. Force drive voltage and full range input is same as internal 2.5V reference voltage.
		6	Z2POS[10]	0		
		5	Z2POS[9]	0		
		4	Z2POS[8]	0		
		3	Z2POS[7]	0		
		2	Z2POS[6]	0		
		1	Z2POS[5]	0		
		0	Z2POS[4]	0		
	0xE7	7	Z2POS[3]	0	R	Z-coordinate position 2. [0] is the MSB.
		6	Z2POS[2]	0		
		5	Z2POS[1]	0		
		4	Z2POS[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
TSC ADC	0xE8	7	AXU0[11]	0	R	AXU0 data acquisition. [11] is the MSB. Full input range is the same as internal reference voltage 2.5V.
		6	AXU0[10]	0		
		5	AXU0[9]	0		
		4	AXU0[8]	0		
		3	AXU0[7]	0		
		2	AXU0[6]	0		
		1	AXU0[5]	0		
		0	AXU0[4]	0		
	0xE9	7	AXU0[3]	0	R	AXU0 data acquisition. [0] is the LSB.
		6	AXU0[2]	0		
		5	AXU0[1]	0		
		4	AXU0[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				
	0xEA	7	AXU1[11]	0	R	AXU1 data acquisition. [11] is the MSB. Full input range is the same as internal reference voltage 2.5V.
		6	AXU1[10]	0		
		5	AXU1[9]	0		
		4	AXU1[8]	0		
		3	AXU1[7]	0		
		2	AXU1[6]	0		
		1	AXU1[5]	0		
		0	AXU1[4]	0		
	0xEB	7	AXU1[3]	0	R	AXU1 data acquisition. [0] is the LSB.
		6	AXU1[2]	0		
		5	AXU1[1]	0		
		4	AXU1[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				

Note:

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS and BIT		NAME	DEFAULT and ACCESS		DESCRIPTION
TSC ADC	0xEC	7	AXU2[11]	0	R	AXU2 data acquisition. [11] is the MSB. Full input range is the same as internal reference voltage 2.5V.
		6	AXU2[10]	0		
		5	AXU2[9]	0		
		4	AXU2[8]	0		
		3	AXU2[7]	0		
		2	AXU2[6]	0		
		1	AXU2[5]	0		
		0	AXU2[4]	0		
	0xED	7	AXU2[3]	0	R	AXU2 data acquisition. [0] is the LSB.
		6	AXU2[2]	0		
		5	AXU2[1]	0		
		4	AXU2[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				
	0xEE	7	AXU3[11]	0	R	AXU3 data acquisition. [11] is the MSB. Full input range is the same as internal reference voltage 2.5V.
		6	AXU3[10]	0		
		5	AXU3[9]	0		
		4	AXU3[8]	0		
		3	AXU3[7]	0		
		2	AXU3[6]	0		
		1	AXU3[5]	0		
		0	AXU3[4]	0		
	0xEF	7	AXU3[3]	0	R	AXU3 data acquisition. [0] is the LSB.
		6	AXU3[2]	0		
		5	AXU3[1]	0		
		4	AXU3[0]	0		
		3	x	x	x	Not used. Data reading in those bits is not certain.
		2				
		1				
		0				

Note:

R: Read accessible, writing to the bit does not make change to the volume. X is uncertain volume.

INTERRUPT DESCRIPTIONS

BLOCK	SITUATION	CONFIGURATION		IDENTIFICATION	
SYS	V_{VSYS}<VSYSLEV	nSYSMODE	nSYSLVMSK	nSYSSTAT	
		1	1	1	
SYS	″Enable Key" press assertion	STA	POSA	STA	DATAA*
		1	1	1	1
SYS	HFPWR assertion	STB	POSB	STB	DATAB*
		1	1	1	1
SYS	HFPWR assertion	STB	NEGB	STB	DATAB*
		1	1	1	1
REG1	OUT1 fault	nFLTMSK		OK*	
		1		0	
REG2	OUT2 fault in buck operation	nFLTMSK		OK*	
		1		0	
REG2	OUT2 fault in linear operation	nFLTMSK		OK*	
		1		0	
REG3	OUT3 fault	nFLTMSK		OK*	
		1		0	
REG4	OUT4 fault	nFLTMSK		OK*	
		1		0	
REG5	OUT5 fault	nFLTMSK		OK*	
		1		0	
REG6	OUT6 fault	nFLTMSK		OK*	
		1		0	
REG7	OUT7 fault	nFLTMSK		OK*	
		1		0	
REG8	OUT8 fault	nFLTMSK		OK*	
		1		0	
REG9	OUT9 fault	nFLTMSK		OK*	
		1		0	
REG10	OUT10 fault	nFLTMSK		OK*	
		1		0	
REG11	OUT11 fault	nFLTMSK		OK*	
		1		0	
REG12	OUT12 fault	nFLTMSK		OK*	
		1		0	
REG13	OUT13 fault	nFLTMSK		OK*	
		1		0	

Note:

*: Instant state output, the reading is the volume by the time of reading.

INTERRUPT DESCRIPTIONS

BLOCK	SITUATION	CONFIGURATION		IDENTIFICATION		
RTC	Alarm assertion	RAAI			ALMINT	
		1			1	
RTC	Day counts changes	RDAI			DAYINT	
		1			1	
RTC	Hour counts changes	RHAI			HRINT	
		1			1	
RTC	Minute counts changes	RMAI			MININT	
		1			1	
RTC	Second counts changes	RSAI			SECINT	
		1			1	
CHG	Pre-condition safety timer time-out	TIMR_STAT	TIMR_PRE	TIMR_PRE	TIMR_STAT	TIMR_DAT
		1	1	1	1	1
CHG	Total charge safety timer time-out	nFLTMSK	TIMR_TOT	TIMR_TOT	TIMR_STAT	TIMR_DAT
		1	1	1	1	1
CHG	Battery thermal condition becomes valid, for the respective option only.	TEMP_STAT	TEMP_POS	TEMP_POS	TEMP_STAT	TEMP_DAT*
		1	1	1	1	1
CHG	Battery thermal condition becomes invalid, for the respective option only.	TEMP_STAT	TEMP_NEG	TEMP_NEG	TEMP_STAT	TEMP_DAT*
		1	1	1	1	1
CHG	Battery installation detected, for the respective option only.	BATT_STAT	BATT_POS	BATT_POS	BATT_STAT	BATT_DAT*
		1	1	1	1	1
CHG	Battery installation not detected, for the respective option only.	BATT_STAT	BATT_NEG	BATT_NEG	BATT_STAT	BATT_DAT*
		1	1	1	1	0
CHG	ACIN input valid	INPUT_STAT	INPUT_POS	INPUT_POS	INPUT_STAT	INPUT_DAT*
		1	1	1	1	1
CHG	ACIN input not valid	INPUT_STAT	INPUT_NEG	INPUT_NEG	INPUT_STAT	INPUT_DAT*
		1	1	1	1	0
CHG	Charge state jumps into the end of charge sleep state.	CHG_STAT	CHG_POS	CHG_POS	CHG_STAT	CHG_DAT*
		1	1	1	1	1
CHG	Charge state jumps out of the end of charge sleep state.	CHG_STAT	CHG_NEG	CHG_NEG	CHG_STAT	CHG_DAT*
		1	1	1	1	0
TSC ADC	Pen touch detected	PENMASK	nAUTO	DATARDY	PENIRQ	PENSTAT*
		0	1	1	1	1
				ACQ	PENMASK	
				0	0	
TSC ADC	TSC ADC conversion done	DATAMASK		DATARDY	ACQ	DATAMASK
		0		1	0	0

Note:

*: Instant state output, the reading is the volume by the time of reading.

STEP-DOWN DC/DC AND LDO OUTPUT VOLTAGE SETTING (not apply to VBBAT)

Unit: V

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

VBBAT OUTPUT VOLTAGE SETTING (with around 10μA load current)

Unit: V

VSET[2:0]	VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.400	0.600	0.800	1.000	1.400	1.800	2.200	3.000
001	0.425	0.625	0.825	1.050	1.450	1.850	2.300	3.100
010	0.450	0.650	0.850	1.100	1.500	1.900	2.400	3.200
011	0.475	0.675	0.875	1.150	1.550	1.950	2.500	3.300
100	0.500	0.700	0.900	1.200	1.600	2.000	2.600	3.400
101	0.525	0.725	0.925	1.250	1.650	2.050	2.700	3.500
110	0.550	0.750	0.950	1.300	1.700	2.100	2.800	3.600
111	0.575	0.775	0.975	1.350	1.750	2.150	2.900	3.700

CHARGER VOLTAGE SETTING

Unit: V

VSET[3:0]															
0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4.1	4.12	4.14	4.16	4.18	4.2	4.22	4.24	4.26	4.28	4.30	4.32	4.34	4.36	4.38	4.4

FAST CHARGE CURRENT SETTING

Unit: mA

ISET[3:0]															
0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
90	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000

NON-LINEAR DUTY SETTING

[7:5]	DUTY_[4:1], DUTY_[0] is ignored for its less change.															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
000	0.0	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.4	0.5	0.5	0.6	0.6	0.7	0.7	0.8
001	0.8	0.9	0.9	1.0	1.0	1.0	1.1	1.1	1.2	1.2	1.3	1.3	1.4	1.4	1.5	1.5
010	1.6	1.7	1.8	1.9	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	3.0	3.1
011	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0	5.2	5.4	5.6	5.8	6.0	6.2
100	6.4	6.8	7.2	7.6	8.0	8.4	8.8	9.2	9.6	10	10	11	11	12	12	12
101	13	14	15	15	16	17	18	18	19	20	21	22	22	23	24	25
110	26	27	29	31	32	34	35	37	38	40	41	43	45	46	48	49
111	52	53	55	58	61	64	67	73	77	80	83	86	89	92	95	100

STEP-UP DC/DC VOLTAGE SETTING

Unit: V

VSET [7:4]	VSET[3:0]															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	3.0 for all codes before 01000000.															
0001																
0010																
0011																
0100	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9	4.0	4.1	4.2	4.3	4.4	4.5
0101	4.6	4.7	4.8	4.9	5.0	5.1	5.2	5.3	5.4	5.5	5.6	5.7	5.8	5.9	6.0	6.1
0110	6.2	6.3	6.4	6.5	6.5	6.7	6.8	6.9	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7
0111	7.8	7.9	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	8.8	8.9	9.0	9.1	9.2	9.3
1000	9.4	9.5	9.6	9.7	9.8	9.9	10.0	10.1	10.2	10.3	10.4	10.5	10.6	10.7	10.8	10.9
1001	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7	11.8	11.9	12.0	12.1	12.2	12.3	12.4	12.5
1010	12.6	12.8	13.0	13.2	13.4	13.6	13.8	14.0	14.2	14.4	14.6	14.8	15.0	15.2	15.4	15.6
1011	15.8	16.0	16.2	16.4	16.6	16.8	17.0	17.2	17.4	17.6	17.8	18.0	18.2	18.4	18.6	18.8
1100	19.0	19.4	19.8	20.2	20.6	21.0	21.6	21.8	22.2	22.6	23	23.4	23.8	24.2	24.6	25.0
1101	25.4	25.8	26.2	26.6	27.0	27.4	27.8	28.2	28.6	29.0	29.4	29.8	30.2	30.6	31	31.4
1110	31.8	32.2	32.6	33.0	33.4	33.8	34.2	34.6	35	35.4	35.8	36.2	36.6	37	37.4	37.8
1111	38.2	38.6	39.0	39.4	39.8	40.2	40.6	41.0	41.4 for all codes after 11111000.							

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{VBAT} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operation Range		V_{VSYS}	2.6		5.5	V
Operation Range		V_{CHGIN}	4.2		6	
UVLO Threshold Voltage		V_{VSYS} Rising	2.4	2.5	2.6	
UVLO Hysteresis		V_{VSYS} Falling		0.2		
SYSLEV Programming Range		V_{VSYS}, for SYSLEV[3:0]=0000 to 1111, and V_{VBAT}>V_{UVLO}		0.1		
SYSLEV Hysteresis		V_{VSYS} Rising		0.2		
Voltage Reference		T_A = -40°C to +85°C		1.2		
Voltage Reference Accuracy		LOWIQ[ ] = 0	-0.5		0.5	%
		LOWIQ[ ] = 1	-1.5		1.5	
Reset Time-out		TRST[ ] = 0		260		ms
		TRST[ ] = 1		65		
Oscillator Frequency			1.8	2	2.2	MHz
IO Logic High Input	HFPWR, PWRHLD, nIRQ, nRSTO, nPBSTAT	V_{VBAT}=2.5V to 5.5V, T_A = -40°C to 85°C.	1.4			V
IO Logic Low Input					0.4	
IO Leakage Current		0-5.5V applied.	-1		1	µA
IO Output Low		Sinking 10mA.			0.3	V
Shutdown Current		All circuit blocks off		12	18	µA
No Load Current		Deep sleep: REG2 in linear mode, the V_{BBAT} and the V_{ALIVE} are on, the RTC is disabled, V_{VSYS}=4.0V.		48		
Thermal Shutdown Temperature		Temperature rising		160		°C
Thermal Shutdown Hysteresis		Temperature falling		20		

Note:

See the I^2C INTERFACE ELECTRICAL CHARACTERISTICS for SCL and SDA specifications.

See the TYPICAL PERFORMANCE CHARACTERISTICS for:

The Reference Voltage Line Regulation.

The Reference Voltage Temperature Coefficient.

The Oscillator Frequency Line Voltage Pulling.

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Voltage Range, V_{VP1}, V_{VP2}			2.7		6	V
UVLO, V_{VP1}, V_{VP2}			2.5	2.6	2.7	
UVLO Hysteresis				100		mV
Output Programming Range			0.6		3.9	V
Output Voltage Accuracy	REG1 or REG2 in buck mode, I_{OUT} = 10mA	For output ⩾1.2V	-1		1	%
		For output <1.2V	-1.5		1.5	
	REG2 in LDO mode, LOWIQ[ ] = 0, I_{OUT} = 10mA		-1.5		1.5	
Maximum Load Current	The REG1		1.2			A
	EVENT4[ ]=0, the REG2, buck mode		0.7			
	EVENT4[ ]=1, the REG2, linear mode		0.02			
Line Regulation	V_{VPX} = Max (V_{OUT} +1V, 3.2V) to 5.5V			0.15		%/V
Load Regulation	Load = 10mA to full maximum load			1.7		%/mA
Turn-On Propagation Delay	From the I^2C last bit latched or PWRHLD set 1 to output changes.			150		µs
Soft Start Ramp Time, REG1 and REG2 buck mode.	Time between 2 intersection points of the ramp slope and 2 voltages; 0% and 100% of the final, no and full load.			400		
Switch Frequency	Normal operation, is the system oscillator frequency.		1.8	2	2.2	MHz
Efficiency	REG1, Load = 200mA, V_{OUT1} = 1.2V			90		%
	REG2, Load=200mA, V_{OUT2}=1.8V			93		
OK Threshold to Normal Ratio	OK[ ] asserts 0			93		
Switch Frequency Fold-back Voltage Threshold to Normal	Switch Frequency folds-back to 1/4 of normal frequency.			25		
No Load Current				65		µA
Shutdown Current					1	

Note:

See the TYPICAL PERFORMANCE CHARACTERISTICS for:

The REG1 Soft-Start from Last I2C Bit, Full Load.

The REG1 Soft-Start from PWRHLD Set 1, No Load.

The REG1 Step Transition Response, Full Load.

The REG1 Efficiency Plot.

The REG2 Efficiency Plot.

The REG1 Load Transition Response.

The REG2 Load Transition Response.

The REG2 Buck mode to the Linear Mode Transition.

STEP-UP DC/DC ELECTRICAL CHARACTERISTICS

(V_{POWER} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{VBAT}	2.7		6	V
UVLO	V_{VBAT}	2.5	2.6	2.7	
UVLO Hysteresis			100		mV
Output Programming Range		3		41.4	V
Output Voltage Accuracy	I_{OUT}=10mA.	-3		3	%
Maximum Load Current	V_{POWER}=4.2V, V_{OUT3}=5V, Voltage regulation option.		0.5		A
FB3 Feedback Voltage	Not available in voltage regulation mode, contact Active-semi for more details.		/		mV
FB3 Input Current			/		nA
Turn-On Propagation Delay	From the I^2C last bit latched or PWRHLD set 1 to output changes.		150		µs
Soft Start Ramp Time, voltage regulation option.	Time between 2 intersection points of the ramp slope and 2 voltages; 0% and 100% of the final, no and full load.		200		
Switch Frequency	Normal operation, is the system oscillator frequency.	1.8	2	2.2	MHz
Minimum Off-Time			40		ns
Minimum On-Time			75	90	
Efficiency	Voltage regulation option, V_{OUT3}=5V, Load=200mA.		90		%
Switch Current Limit			0.75		A
OK Threshold to Normal Ratio	OK[ ] asserts 0		93		%
No Load Current	Switch in operation		1300		µA
	Switch stops		80		
Shutdown Current				1	

Note:

The V_{POWER} is the voltage input that the Step-up DC/DC inductor connects to.

See the TYPICAL PERFORMANCE CHARACTERISTICS for:

The REG3 Start up Waveform, Full Load.

The REG3 Step Transition Response, Full Load.

The REG3 Efficiency Plot.

The REG3 Load Transition Response.

The REG3 External PWM Modulation to Current.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{INL}			2.4		6	V
Output Programming Range				0.6		3.9	
Output Voltage Accuracy	LOWIQ[ ]=0	T_A = 25°C		-1.5		+1.5	%
		T_A = -40°C to 85°C		-2.5		+2.5	
Line Regulation	V_{INL} = (V_{OUT} + 0.5V) to 5.5V				1		%/V
Load Regulation	Load=1mA to maximum load current.				0.03		%/A
Power Supply Rejection Ratio (PSRR)	C_{OUT}=1µF, Load=20mA, V_{OUT}=1.8V, REG5, REG6, REG9, REG10, REG11, REG12,REG13	At 1kHz, LOWIQ[ ]=Any			-80		dB
		At 10kHz.	LOWIQ[ ]=0		-70		
			LOWIQ[ ]=1		-60		
Maximum Load Current	REG4, REG6, REG7, REG8			0.36			A
	REG5, REG9, REG12			0.25			
	REG10, REG13			0.15			
	REG11			0.08			
Current Limit	When 5% Voltage drop is seen from the normal output voltage.	REG4, REG6, REG7, REG8		0.41	0.68		A
		REG5, REG9, REG12		0.28	0.47		
		REG10, REG13		0.17	0.28		
		REG11		0.09	0.15	0.22	
Dropout Voltage	Set load current to 1/4 of max output current; Ramp down input supply until V_{OUT}=V_{SET} - 100mV.				140		mV
Output Noise	REG5, REG6, REG9, REG10, REG11, REG12, REG13, C_{OUT}=1µF, Load=20mA, V_{OUT}=1.8V, LOWIQ[ ]=0				30		μV_{RMS}
Turn-On Propagation Delay	From the I^2C last bit latched or PWRHLD, ON6 or ON9 set 1 to output changes.				150		µs
Soft-Start Ramp Time	Time between 2 intersection points of the ramp slope and 2 voltages; 0% and 100% of the final, no and full load.			30		150	
OK Threshold to Normal Ratio	OK[ ] asserts 0				89		%
Current Limit Fold-Back Ratio	Ratio to the current limit, when output short circuit.				45		
Discharge Resistance	LDO Disabled, DIS[ ] = 1				1. 5		kΩ
Stable C_{OUT} Range	REG4, REG6, REG7, REG8			3.3		20	µF
	REG5, REG9, REG12			2.2		20	
	REG10, REG13			1.5		20	
	REG11			1		20	
No Load Current	LOWIQ[ ]=0				22		µA
	LOWIQ[ ]=1				15		
Shutdown Current						1	

Note: See the TYPICAL PERFORMANCE CHARACTERISTICS for:
The REG4 Start up Waveform, No Load; The REG4 Start up Waveform, Full Load;
The REG4 voltage step transition response; The REG4 Load Transition Response.

SINGLE-CELL LI+ CHARGER ELECTRICAL CHARACTERISTICS

(V_{CHGIN} = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CHARGE INPUT						
Input Voltage Range	Nominal condition V_{CHGIN}		0		7	V
Valid for Charging Input Voltage Range	V_{CHGIN}		4.2		6.0	
CHGIN OVP Threshold	V_{CHGIN} rising, OVPSET[1:0] = 00			6.3		
CHGIN OVP Threshold Adjustment Step	LSB weight for threshold adjustment, OVP-SET[1:0] from 00 to 11 stepping up.			200		mV
CHGIN OVP Threshold Hysteresis	V_{CHGIN} falling			200		
CHGIN UVLO Threshold	V_{CHGIN} rising		3.8	4.0	4.2	V
CHGIN UVLO Hysteresis	V_{CHGIN} falling			500		mV
Logic Low Input Level	For ACIN and CHGLEV.				0.4	V
Logic High Input Level			1.4			
CHGIN Supply Current	V_{CHGIN} < V_{UVLO}			50	100	µA
	Suspended, SUSCHG[ ]=1.			200	300	
	End of charge sleep, CHG_DAT reads 1.			800	1200	
CHARGE REGULATION						
Battery Regulation Voltage	For top-off, floating or LDO mode operation; No load at VBAT.	VSET[3:0]=0101	4.179	4.2	4.221	V
Battery Regulation Voltage Adjustment Resolution		Weight of the LSB, VSET[3:0]=0000 to 1111	19.5	20	20.5	mV
Line Regulation	V_{CHGIN} =4.5V to 5.5V, I_{BAT}=10mA			0.1		%/V
Load Regulation	I_{BAT}=100mA to 1000mA		0.001	0.001	0.001	%/mA
Fast Charge Current	CHGLEV=0 and ACIN=0, or ISET[3:0]=0000		75	90	105	mA
	CHGLEV=1 and ACIN=0, or ISET[3:0]=0100		0.4	0.45	0.5	A
	ACIN=1, ISET[3:0]=1111		0.9	1	1.1	
Fast Charge Current Adjustment Resolution	Change per adjacent code stepping for ISET [3:0] =0001 to 1111, from 0.3A to 1A.			50		mA
Precondition Charge Current, ratio to fast charge current.	ISET[3:0]=0001 to 1111		8	10	12	%
	ISET[3:0]=0000			45		mA
Precondition Threshold	V_{VBAT} rising.		2.75	2.85	3	V
Precondition Threshold Hysteresis	V_{VBAT} falling.			150		mV
End of Charge Residual Ratio	Ratio to the fast charge current		8	10	12	%
Charge Restart Drop	Drop of the battery regulation voltage, falling.		180	220	264	mV
Thermal Regulation Action Range[NOTE]	Thermal regulation starts to current cut temperature range, at the sensor junction.		90		140	°C

SINGLE-CELL LI+ CHARGER ELECTRICAL CHARACTERISTICS CONT'D

(V_{CHGIN} = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On-Resistance	Path resistance from CHGIN to VBAT, in fully on state.		0.5		Ω
Reverse Blocking Put-in Threshold	V_{CHGIN} to V_{VBAT} difference on the closed blocking switch decreasing going.	28	32	42	mV
Reverse Blocking Put-out Threshold	V_{CHGIN} to V_{VBAT} difference on the blocked switch increasing going.	80	93	113	
VBAT Reverse Leakage	V_{CHGIN} <V_{UVLO} or Charging suspended, SUSCHG [ ]=1.		8		μA
CHARGE TIMING					
Precondition Safe Timer Time-out Programming Range	PRETIMO[1:0]=00 to 10 (11 for no timeout)	60		120	min
Total charge Time-out Period Programming Range	TOTTIMO[1:0]=00 to 10 (11 for no timeout).	180		360	
State Transition Delay Time	The time of a new state conditions to be qualified.		32		ms
CONDITIONING AND INDICATION DRIVING					
Battery Installation Trap Level	Voltage at BATID; Level for installation detected.			2	V
No Battery Installation Level	Voltage at BATID; Level for no installation detected.	2.5			
Cell Hot Trap Divider Ratio	Dividing of V_{CHGIN}. Decreasing trip for hot trap, increasing trip for cold trap.		0.349		
Cell Cold Trap Divider Ratio			0.748		
Hot/Cold Trap Reverse Trips Hysteresis			30		mV
nSTAT Sinking Current	V_{nSTAT}=1V to 6V.		8		mA
Input Leakage	Applying 0V to 5V on the BATID, the TH, the nSTAT.	-1		1	μA

Note:

The thermal regulation action range is characterized at small current situation, is guaranteed by design verification, characterization and production process control.

See the TYPICAL PERFORMANCE CHARACTERISTICS for:

The Charge Current to Battery Voltage, at 5V Input.

The Charge Current to Battery Voltage, at 6V Input.

The Charge Current to Ambient Temperature, 6V Input.

The Charger Load Transition Response, LDO Mode.

BACK-UP BATTERY CHARGER ELECTRICAL CHARACTERISTICS

(V_{VBAT} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge Valid Voltage Range	V_{BBCIN}	2.5V or V_{VBBAT}+1.2		5.5	V
Regulation Voltage Range	Programmable by setting VSETBB[3:0]	0.4		3.7	
Output Voltage Accuracy	I_{LOAD}=10μA.	2.552		2.795	V
Load Regulation Drop Per Decade Change of Current	I_{LOAD}=1mA		150	200	mV
Dropout Voltage	I_{LOAD}=1mA, 100mV more drop from the output voltage at the input voltage is 1.2V above the output.		1.18		V
Maximum Charge Current			5		mA
No Load Operation Current				10	μA
Stable C_{OUT}	For I_{LOAD}~5mA		1		μF
Reverse Blocking Leakage	Current flows out off the BBCIN pin at V_{VBBAT}=3.6V, V_{BBCIN}=0V to 2V.			10	nA
Output Short Circuit Current				100	mA

Note:

See the TYPICAL PERFORMANCE CHARACTERISTICS for:
The Backup Battery Charge Current to Input Voltage.

ALWAYS-ON LOW POWER LDO ELECTRICAL CHARACTERISTICS

(V_{VBAT} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operation Voltage Range	V_{BBCIN} or V_{VBBAT}	1.8V or V_{VALIVE}+0.5		5.5	V
Regulation Voltage Range	Programmable by setting VSETRTC[3:0].	0.6		3.9	
Output Voltage Accuracy	Include load regulation and line input regulation.	-3.5		2.5	%
Dropout Voltage	I_{OUT}=5mA, V_{OUT}=3.1V, 100mV more drop from the output voltage at the input voltage is 1V above the output.		150		mV
Maximum Output Current		7	25	50	mA
No Load Operation Current	RTCEN[ ]=0			7	μA
Stable C_{OUT}	For I_{LOAD}~5mA		1		μF
	For I_{LOAD}~20mA		2.2		
Reverse Blocking Leakage	V_{VBBAT}=3.6V, V_{BBCIN}=0V to 2V.		4		μA
Output Short Circuit Current				100	mA

REAL TIME CLOCK ELECTRICAL CHARACTERISTICS

(V_{VBAT} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum Sustainable Supply	Crystal type: MC-146;TXC 9H03200010; AB38T.			1.2	V
Oscillation Starting Supply				1.4	
Maximum Supply Voltage		3.6			
Maintaining Operation Current	No alarm enabled.		5		μA
Shutdown Current	Disabled.			100	nA
CLK32K Output Duty	Test with 5kΩ pull-up to 1.8V.	10		90	%
CLK32K Cycle to Cycle Jitter	Falling edge to falling edge, evaluated for 100ms.				ns
OC Output Low	10mA sinking.			0.3	V
Maximum OC Pull-up Voltage		5.5			
OC Pin Capacitance	OC output off, the board and stripe parasitic removed.		2		pF

OPEN-DRAIN DRIVER ELECTRICAL CHARACTERISTICS

(V_{VBAT} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Adjustment Weight	ISCALE_[1:0]=00			0.4		mA/bit
	ISCALE_[1:0]=01			0.8		
	ISCALE_[1:0]=10			1.2		
	ISCALE_[1:0]=11			1.6		
Output Current Range	Programmable by setting ISET_[5:0]=000000 to 111111		0		100.8	mA
Absolute Current Error	ISCALE_[1:0]=01, ISET_[5:0]=100000 for 25.6mA.	Sinks from 1V source	-2.5		2.5	mA
Chanel to Chanel Mismatch				0.5	2.5	
Load Regulation		ODO1, ODO2 and ODO3, current change for sinking from 1V to sinking from 2.5V; ODO1 also from 2V to from 5V.		0.2	0.3	
				0.2	0.3	
Output Low Voltage		Feed in with 5mA from external source.			0.35	V
Leakage Current	ODO1, sinking from 40V source.				5	μA
	ODO2, ODO3, sinking from 5.5V source.				1	
Internal PWM Frequency				244		Hz
PWM Duty Adjustment	Linear adjustment option, non-linear adjustment option.		0		100	
Chanel to Chanel Delay	BUFFER[ ]=1 (if set 0, the delay is 1/4 of the PWM cycle).			1		ms
Current-On Slew Rate	ODO2, ODO3			40		mA/μs
	ODO1			15		
Over-eating Temperature[NOTE]				135		°C
Operation Current	ISET_[5:0]=000001			27		μA
Shutdown Current	ISET_[5:0]=000000				1	

Note: Guaranteed by design verification, characterization and production process control.

TSC ADC ELECTRICAL CHARACTERISTICS

(V_{VBAT} = V_{VD} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operation Voltage Range	V_{VD}	2.9		5.5	V
Reference Voltage (V_{REF})	T_A = -40°C to +85°C		2.5		
Maximum Available Resolution	CLEN=0		12		bits
Full Scale Dynamic Range at Input (FSDR[NOTE1])	XPOS, YPOS, XNEG, YNEG, AUX0, AUX1, AUX2.		V_{REF}		V
	AUX3		6.024		
Absolute DC Conversion Error	AUX3, measured with V_{VBAT}=3.9V.	-21		21	mV
TSC Conversion Time (Counts of internal clock cycles of the device)	CLEN=0(for 12 bits resolution), Switch frequency 2MHz.		225		µs
INL[NOTE2]	The standard deviation plus the 1st movement of the worst. INL and DNL are from DC sweep histogram analysis; Offset and Gain Error are from least square linear approximation, from data of input in 10% to 90% FSDR; Effective Numbers of Bits is the worst FWHM[NOTE3] of reading a DC volume in same range. Test on channel 0 to channel 6 only, 12 bits conversion.	-4		5	LSB
DNL[NOTE2]		-1		1	
Offset[NOTE2]			8		
Gain Error[NOTE2]			1.5		
Effective Numbers of Bits[NOTE2]					bit
Input Impedance			11		MΩ
Input capacitance			32		pF
Input leakage Current				0.1	µA
Touch Detection Trap Thresholds	Voltage at the XPOS when pen touch trapped.			1	V
Force Current	At force driving voltage drop 5%.		17		mA
Force Switch On-Impedance			4		Ω
Conversion Operation Current			210		µA
Shutdown Current				1	

NOTE1: DC Full Scale Dynamic Range at input.

NOTE2: Guaranted by design verfication, characterization and production process control.

NOTE3: Full Width of Half Magnititude.

See The TYPICAL PERFORMANCE CHARACTERISTICS for:

The DC Sweep Histogram DNL

Note: Guaranteed by design verification, characterization and production process control.

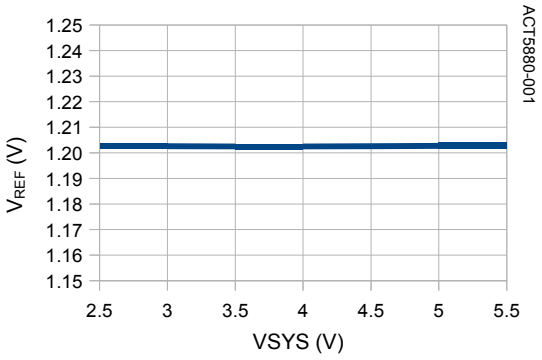
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

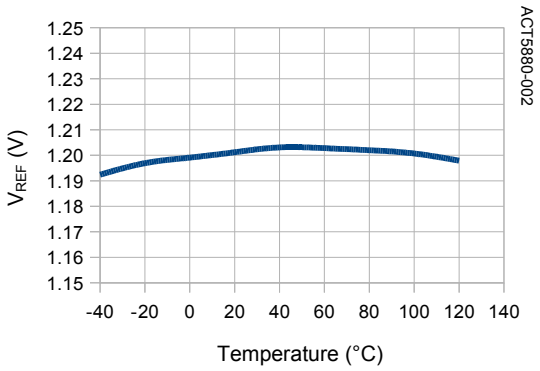
The waveform captures and the plots:

1. The Reference Voltage Line Regulation.	2. The Reference Voltage Temperature Coefficient.
3. The Oscillator Frequency Line Voltage Pulling.	4. The Oscillator Frequency Temperature Pulling.
5. The REG1 Soft-Start from Last I²C Bit, Full Load.	6. The REG1 Soft-Start from PWRHLD Set 1, No Load.
7. The REG1 Step Transition Response, Full Load.	8. The REG1 Efficiency Plot.
9. The REG2 Efficiency Plot.	10. The REG1 Load Transition Response.
11. The REG2 Load Transition Response.	12. The REG2 Buck mode to the Linear Mode Transition.
13. The REG3 Start up Waveform, Full Load.	14. The REG3 Step Transition Response, Full Load.
15. The REG3 Efficiency Plot.	16. The REG3 Load Transition Response.
17. The REG3 External PWM to Current Output.	18. The REG4 Start up Waveform, No Load.
19. The REG4 Start up Waveform, Full Load;	20. The REG4 voltage step transition response.
21. The REG4 Load Transition Response.	22. The Charge Current vs. V_{VBAT}, V_{CHGIN}=5V.
23. The Charge Current vs. V_{VBAT}, V_{CHGIN}=6V.	24. The Charge Current vs. Ambient Temperature, 6V input.
25. The Charger Load Transition Response , LDO Mode.	26. The Backup Battery Charge Current vs. V_{VSYS}
27. The DC Sweep Histogram DNL	28. The DC input Effective Numbers of Bits.

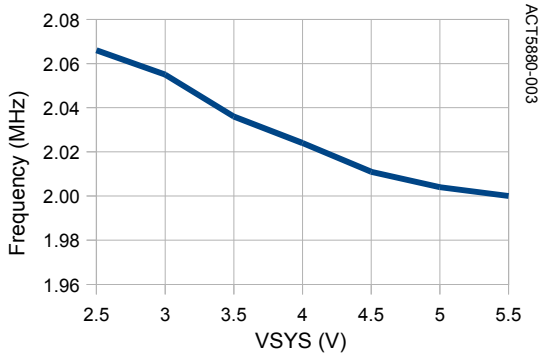
1. The Reference Voltage Line Regulation



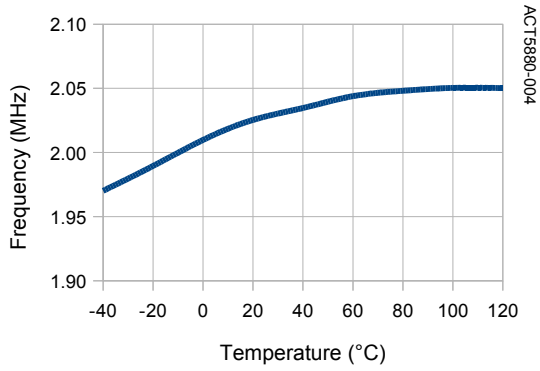
2. The Reference Voltage Temperature Coefficient



3. The Oscillator Frequency Line Voltage Pulling



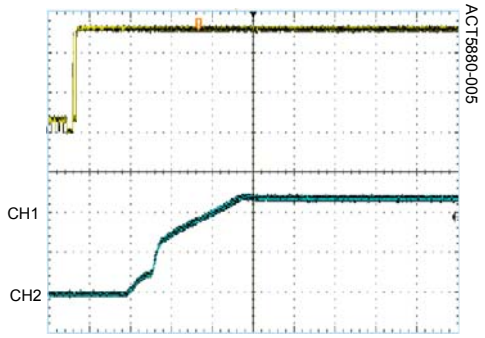
4. The Oscillator Frequency Temperature Pulling



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

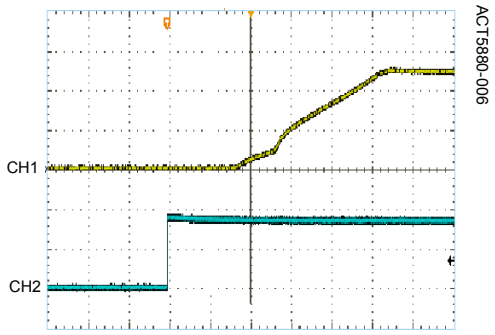
(T_A = 25°C, unless otherwise specified.)

5. The REG1 Start from Last I2C Bit, Full Load



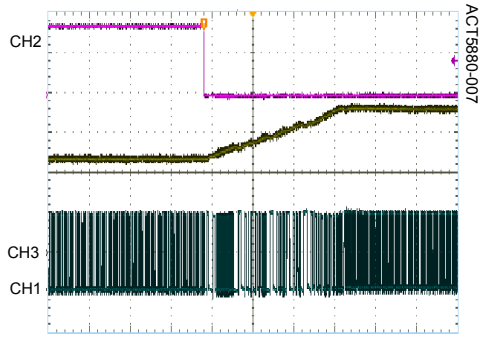
CH1: V_{SCL}, 2V/div
CH2: V_{OUT1}, 0.5V/div
TIME: 100µs/div

6. The REG1 Start from PWRHLD set, no load



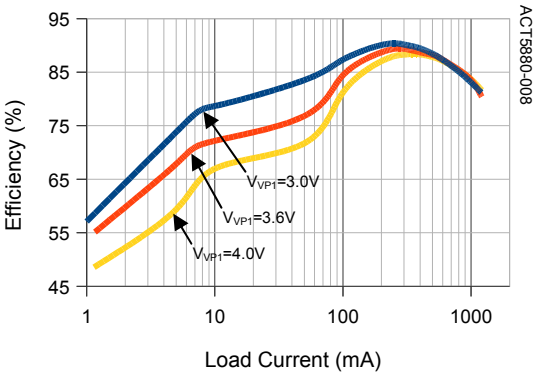
CH1: V_{OUT1}, 0.5V/div
CH2: PWRHLD, 2V/div
TIME: 100µs/div

7. The REG1 Step Transition Response, Full Load

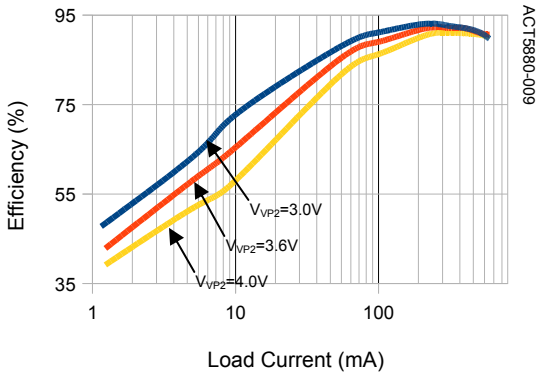


CH1: V_{SCL}, 2V/div,
CH2: V_{SDA}, 2V/div,
CH2: V_{OUT1}, 0.5V/div
TIME: 10µs/div

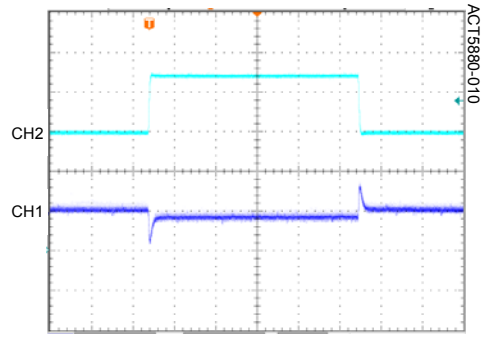
8. The REG1 (1.2V) Efficiency vs. Load Current



9. The REG2 (1.8V) Efficiency vs. Load Current



10. The REG1 Load Transition Response

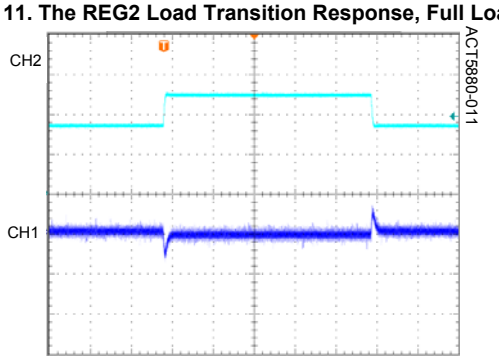


CH1: V_{OUT1}, AC coupled, 10mV/div
CH2: Load Current, 200mA/div
TIME: 400µs/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

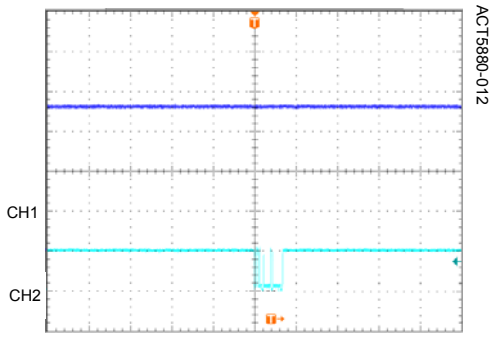
(T_A = 25°C, unless otherwise specified.)

11. The REG2 Load Transition Response, Full Load



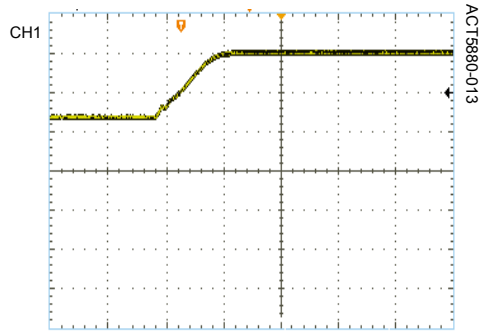
CH1: V_{OUT2}, AC coupled, 10mV/div
CH2: Load Current, 200mA/div
TIME: 400μs/div

12. The REG2 Buck to Linear Mode Transition



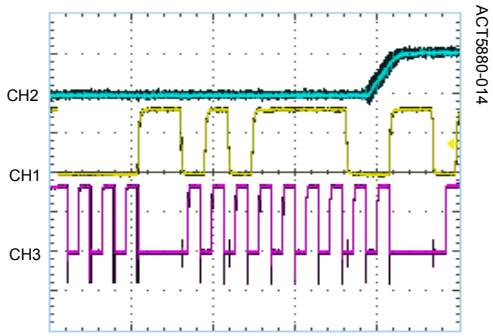
CH1: V_{OUT2}, 0.5V/div
CH2: V_{SDA}, 5V/div
TIME: 400μs/div

13. The REG3 Start up Waveform, Full Load



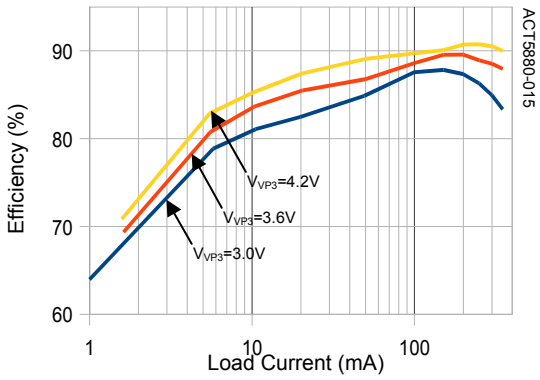
CH1: V_{OUT3},1V/div
TIME: 200μs/div

14. The REG3 Step Transition Response, Full Load

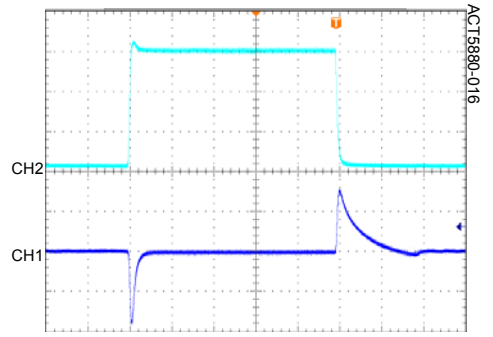


CH1: V_{SDA}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{SCL}, 2V/div
TIME: 400μs/div

15. The REG3 Efficiency vs. Load Current



16. The REG3 Load Transition Response

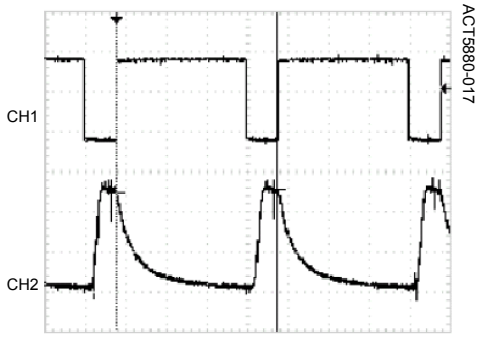


CH1: V_{OUT3}, AC coupled, 200mV/div
CH2: Load Current, 100mA/div
TIME: 400μs/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

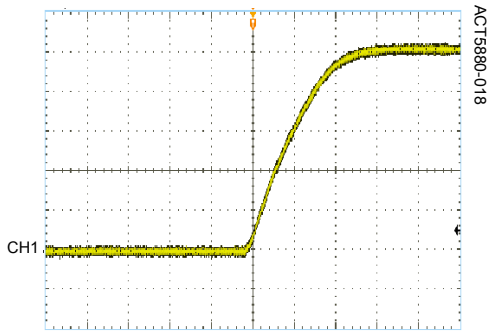
(T_A = 25°C, unless otherwise specified.)

17. The REG3 External PWM Modulation to Current



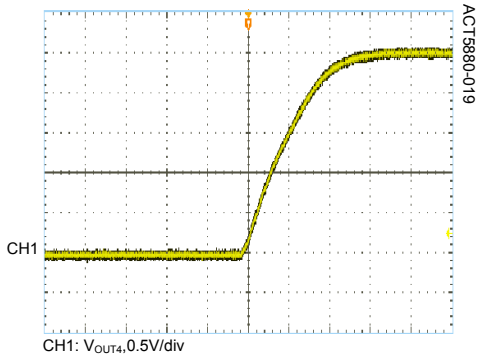
CH1: PWM signal
CH2: LED Current (sensed on sample resistor)
TIME: About 1KHz, 20% Duty Cycle

18. The REG4 Start up Waveform, No Load



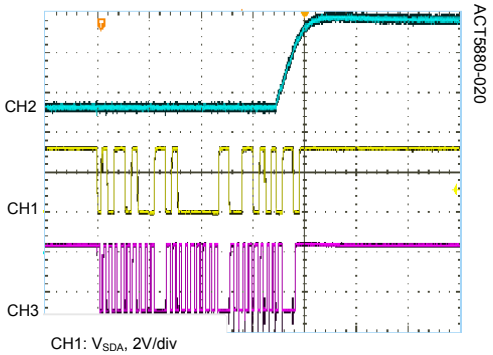
CH1: V_{OUT4}, 0.5V/div
TIME: 40μs/div

19. The REG4 Start up Waveform, Full Load



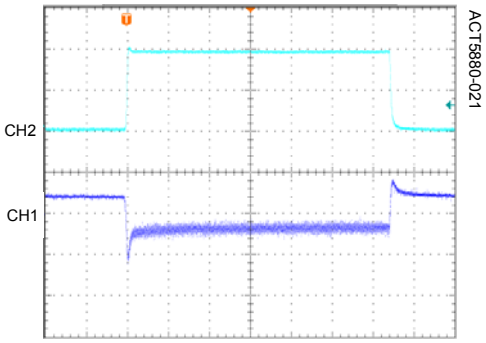
CH1: V_{OUT4},0.5V/div
TIME: 40μs/div

20. The REG4 Step Transition Response



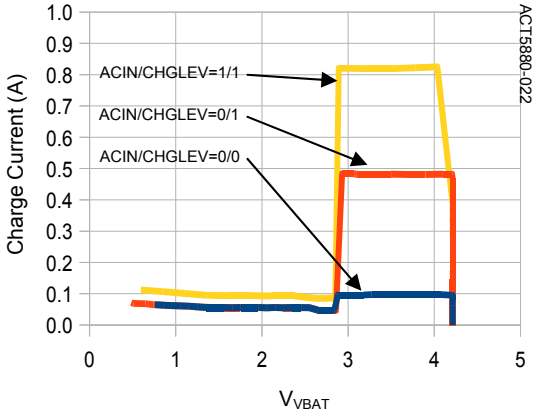
CH1: V_{SDA}, 2V/div
CH2: V_{OUT4}, 0.5V/div
CH3: V_{SCL}, 2V/div
TIME: 100μs/div

21. The REG4 Load Transition Response



CH1: V_{OUT4}, AC coupled, 50mV/div
CH2: Load Current, 200mA/div
TIME: 400μs/div

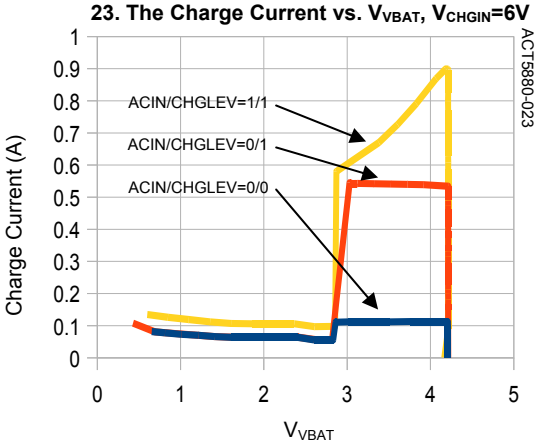
22. The Charge Current vs. V_{VBAT}, V_{CHGIN}=5V



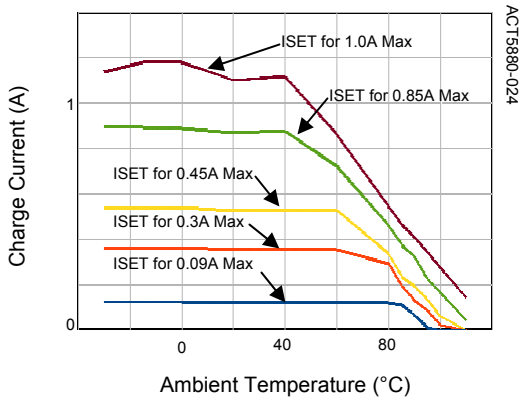
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

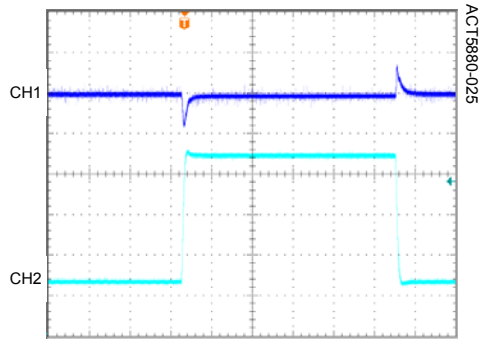
23. The Charge Current vs. V_{VBAT}, V_{CHGIN}=6V



24. The Charge Current vs. Ambient Temperature, V_{CHGIN}=6V

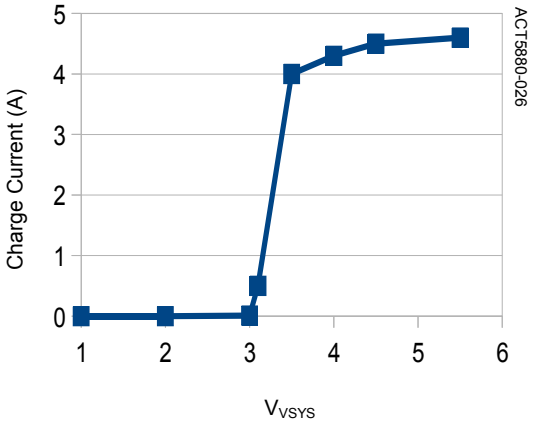


25. Charger Load Transition Response, LDO Mode

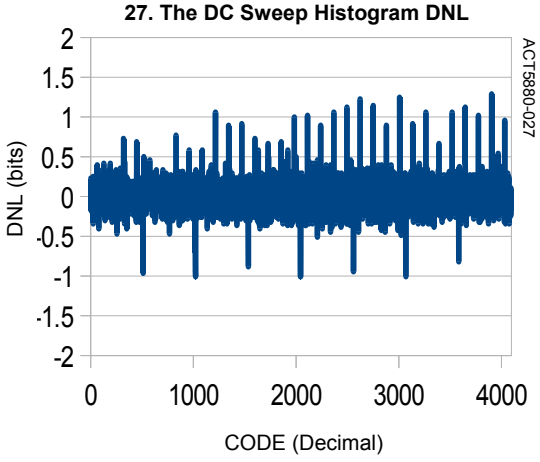


CH1: V_{VBAT}, AC coupled, 100mV/div
CH2: Load Current, 200mA/div
TIME: 200μs/div

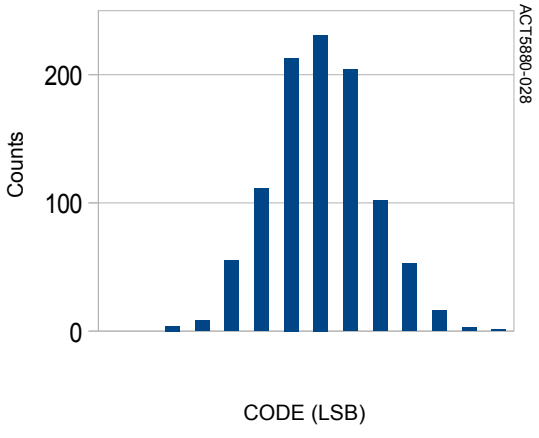
26. Backup Battery Charge Current vs. V_{VSYS}



27. The DC Sweep Histogram DNL



28. The DC Input Effective Numbers of Bits



APPLICATION INFORMATION

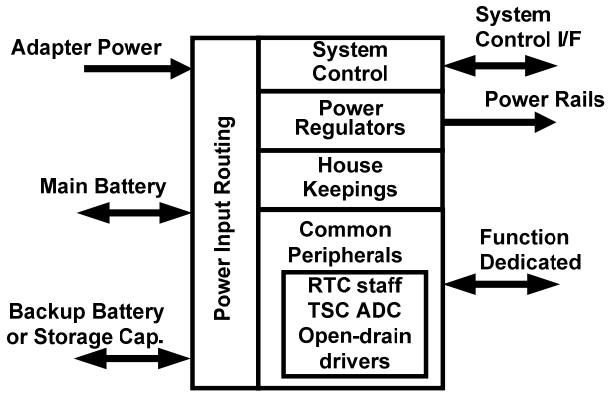
The ACT5880 is a combinations of many circuit blocks including step-down DC/DCs, a step-up DC/DC, LDOs, an RTC, an ADC block with a front end for both TSC and general purpose analogue signal acquisition. Each of those blocks has its own control and configuration register, shares the same interface block, same house keeping block which provides common resource to other blocks, including operation supervising, interrupts, clock reference and voltage references. Those blocks make a two layers architecture in system point of view.

System and Control Information

Figure 1 shows the top level functional block diagram of the ACT5880. The ACT5880 manages 3 different power inputs and 4 groups of functional macro-blocks. The ACT5880 can be enabled, when system control interface and most power regulators are available for using, only when either the adaptor power or the main battery is available, or both of them are available; When there is only the backup power available, only the always-on regulator keeps the VALIVE output and RTC running.

Figure 1:

The Top Level Block Diagram of The ACT5880



The backup battery charger, the always-on regulator and the RTC circuit are not subject to the enable status of the ACT5880. Whenever there is any of adaptor power and/or main battery power are available, the backup battery charger charges or floating charges the backup battery or the storage cap, the always-on regulator outputs to the RTC staff.

Device Power States

The ACT5880 has 2 powered states, which are enable state and disable state. The ACT5880 could be turned into enable state only when either or both the adaptor power and the main battery are available.

In the enable state, the ACT5880 power rails may or may not output, dependent on how those regulators are programmed. There are 5 events or signals that pull the ACT5880 into the enable state, which are the nPBIN assertion, the valid adaptor input voltage, the HFPWR assertion, the PWRHLD assertion and the RTC alarm wake-up event. The ACT5880 turns into disable state only when all those 5 events or signals are de-asserted.

System Control Signals

There are 7 foreign signals and 2 internal signals for the system control in the ACT5880. Table 1 lists those signals.

Table 1:

The System Control Signals to The ACT5880

SIGNALS	DESCRIPTIONS
PBIN	Push-Button input assertion.
HFPWR	Hand-free power requested.
PWRHLD	Input for request to hold the power output.
ON6	Dedicated on/off control for OUT6.
ON9	Dedicated on/off control for OUT9.
SDA	I^2C compatible serial interface.
SCL	
(ACOK)	Internal signal, is true when the CHGIN input voltage is valid.
(ALARM)	Internal signal, is true when the RTC alarm happens if the RTC wake-up is set.

All manipulation and configuration registers are accessible through the "fast mode" (up to 400kHz) I^2C compatible interface with standard I^2C session frame for read/write to one of single byte addressed registers. The ACT5880 is a slave device with device address of [1011010] or 86. In each read/write session, the device address is sent firstly with the 8^{th} bit indicating that the session is for read (1) or for write (0), followed by a register address byte and the bidirectional transferred data byte, each aligns MSB first and is followed by an acknowledge bit.

Among those 9 signals, the ON6, the ON9, the SDA and SLC of the I^2C interface work only when the ACT5880 is enabled.

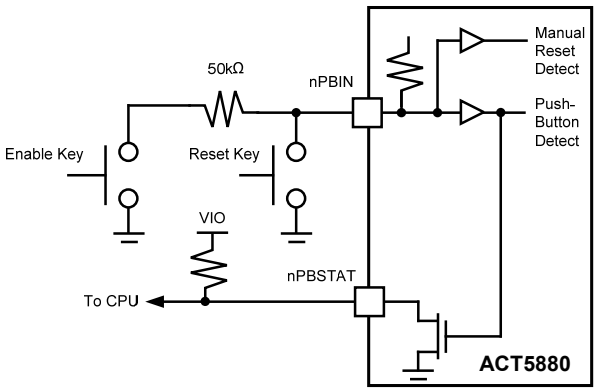
Push-button Inputs

The nPBIN features dual-functions input, by detecting if it is directly shorted to ground or pulled to ground through a resistor of around 50kΩ (good in range of 24kΩ to 82kΩ). See the Figure 2 for the external connection, the push-button that directly grounds the nPBIN input is namely the "Reset Key", is identified as a manual reset request by the ACT5880 when it is pressed; The other push-button is namely the "Enable Key", is identified as a device enable request when it is pressed.

When either "Reset Key" or "Enable Key" is pressed, the nPBSTAT asserts low; In both cases the ACT5880 may assert interrupt to the application system if it is programmed so, by pulling the nIRQ low.

Figure 2:

The External Circuit for The Push button Input



nPBSTAT Output

nPBSTAT is an open-drain output that reflects the state of the nPBIN input; nPBSTAT is asserted low whenever nPBIN is asserted, and is high-Z otherwise. This output is typically used as an push button status signal to the processor, to initiate a software-programmable routine such as operating mode selection or to open a menu. Connect nPBSTAT to an appropriate supply voltage (typically IO voltage) through a 10kΩ or greater resistor.

Control Sequences

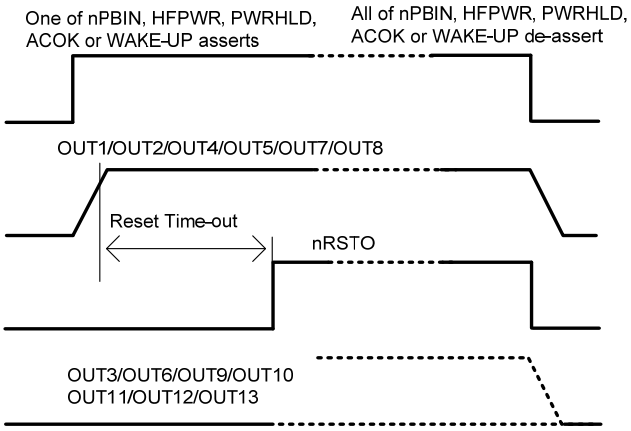
Power Output Sequence

A typical enable sequence initiates as a result of pressing “Enable Key”, which is one of the 5 events mentioned in the "Device Power States", and it turns ACT5880 into the power-on default state or last powered state before being turned off by removing all the 5 events. When REG1 reaches its power-OK threshold, nRSTO is asserted low. If REG1 is above its power-OK threshold when the reset timer expires, nRSTO is de-asserted. If the equipment system pulls the PWRHLD (or any of the HFPWR, ACOK or RTC alarm wake-up) to a logic high before the push-button is released, the enable state of the ACT5880 is kept. If this does not happen, the ACT5880 goes back to the disable state. The Figure 3 shows the states of the ACT5880 and its power rails. The ACT5880 has 2 programmable reset timeout, which is optional on default setting and programmable in operation.

When "Enable Key" is pressed in ACT5880 enable state, the response depends on if the OUT1 outputs is normal at the moment.

Figure 3:

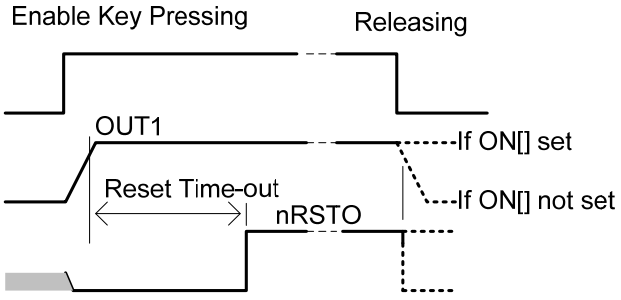
Power Rail Sequence



When OUT1 is already enabled, the push button event only asserts nPBSTAT (and the nIRQ if it is programmed so). When the OUT1 is disabled, the push button event starts OUT1 and pulls the nRSTO low until the reset time-out expires after the OUT1 is in regulation, also asserts nPBSTAT (and nIRQ if it is programmed so), while no change to other rails.Figure 4 shows the "Enable Key" push button event when OUT1 is disabled.

Figure 4:

REG1 to nRSTO Sequence



See Figure 4 for illustration of pressing of "Enable Key" when OUT1 does not output. When OUT1 is in

normal output state, the key press event only asserts nPBSTAT (and the nIRQ when it is programmed so). When OUT1 is disabled, the key press event starts OUT1 and pulls the nRSTO low until the reset time-out expires after the OUT1 is regulated, also asserts nPBSTAT (and nIRQ when it is programmed so), while no change to other rails.

When the manual reset asserts, the ACT5880 pulls the nRSTO output low instantly and holds it low until reset time-out expires after the "Reset Key" is released. As the nRSTO is kept low for a while after the "Reset Key" is released and the power outputs of the ACT5880 remain unchanged, it is assured that the host processor is stopped if no any other of the 5 events holds it on, or is kept on if there is other event holds it.

SLEEP Modes

The ACT5880 features two sleep modes for low quiescent current operation.

The sleep mode is a mode that the PWRHLD is kept high by a circuit external to the ACT5880. Comparing to the normal operation state with different power rail configurations, the sleep mode is a state the host processor keeps essential system functions working. The power rail configurations in sleep mode are in two subsets; One subset keeps at least one of REG1 and REG2 in buck operation, while all the rest rails are flexible to be programmed into any states, the other subset could have both REG1 and REG2 buck mode off while all LDO rails are only programmable in the quiescent current mode, or are forced off if in the low noise mode. As the power rails need to be controlled through the host processor in this mode, it needs to be carefully handled to keep the essential system working.

The deep sleep mode further reduces the quiescent current by stopping all other circuits in the ACT5880 by releasing the PWRHLD to low. In this mode only the always-on regulator, and the linear regulation circuit of the REG2 stay working.

In deep sleep mode, the operation resumes normal by asserting PWRHLD (or any of nPBIN, HFPWR, ACOK or RTC alarm wake-up events), when REG2 starts its buck regulation and other regulators resume their previous states before the removing of PWRHLD. This implies that the deep sleep state has to be put from an operation state of the system by de-asserting PWRHLD. Other ways like turning off the I/O power which may turns the PWRHLD off consequently, may put the system in a state that it could not resume by the assertion of PWRHLD (or any of the nPBIN HFPWR, ACOK or RTC alarm wake-up), until the reloading of power on default state (refer to *UVLOs and Low System Voltage Alert* section for more information).

In both modes, the nRSTO asserts against the resuming of REG1.

Interrupts

The ACT5880 asserts interrupt as designated for a function or when the house keeping circuit finds a condition does not meet the reliable operation situation, by pulling the nIRQ output low. The nIRQ is an open-drain output, which is good for wired-or with other interrupt request sources in the equipment system. Every possible interrupt in the ACT5880 can be masked by resetting/setting the respective register bit. When interrupt asserted, the interrupt is cleared by reading the respective register byte or clearing a respective bit.

There are totally 35 different sources/conditions for interrupt assertion, refer to *INTERRUPT DESCRIBPTIONS* section for a summary. It is practically necessary to mask all the unused interrupts to assure that the equipment system runs efficiently, and to unmask the interrupts in case by case basis for specified applications.

House Keeping Functions

The house keeping functions for the ACT5880 itself include the internal biasing, voltage reference sharing in different blocks, UVLO (Under Voltage Lock-Out), regulation status monitoring, over current protection and over temperature protection. The house-keeping functions assure the ACT5880 only operates reliably in proper system situation, asserts interrupt to the system or shutdown the ACT5880 when necessary condition does not meet. Refer to the following sections for details.

The VSYS and the REFBP

The VSYS is the internal bias rail bypass node, the REFBP is the bypass node for the on-chip reference. The VSYS is driven by an internal pre-regulation circuit, whose output is automatically routed to connect the VBAT when there is no input power at CHGIN is available.

Proper bypass on those nodes reduces the noise and improves the PSRR of every regulator. Capacitors around 47nF~68nF for the REFBP and 1μF~2.2μF for the VSYS are recommended for their bypassing.

UVLOs and Low System Voltage Alert

The ACT5880 has a system UVLO, a V_{VSYS} comparator for low system voltage alert and UVLOs for step-down and step-up DC/DCs. The system

UVLO circuit monitors the voltage at VSYS, it stops the normal operation when the V_{VSYS} is less than the V_{UVLO}, reloads registers with default power on states and starts normal operation when the V_{VSYS} is greater than V_{UVLO}.

All circuit blocks stop but the always-on VALIVE output and the RTC circuit keep running when the system UVLO asserts. The always-on regulator keeps output even when its output voltage drops, the RTC keeps running until its input voltage is too low, the RTCEN bit is reset.

The V_{VSYS} comparator circuit is configurable for stopping the system as the UVLO function does or asserting a system voltage low alert when it sees the V_{VSYS} is less than a programmable threshold. The threshold is programmed by setting the SYSLEV[3:0] in a register, refer to the *GLOBAL REGISTER MAP* and *REGISTER AND BIT DESCRIPTIONS* sections for more details.

Each step-down DC/DCs and the step-up DC/DC has its own UVLO to assure it only operates when both its input voltage and the V_{VSYS} are in proper range.

Over-Current

Each regulator has its own over-current protection. For step-down DC/DCs and the step-up DC/DC , the over-current condition triggers to reduce the switch frequency to ¼ of normal frequency. In LDOs, it triggers fold-back current limit. In both case, the over-current protection consequently causes the drop of output voltage and so the house-keeping interrupt assertion if this function is enabled. Each regulator is safe in unlimited-time output short-circuit (but not the step-up DC/DC, in which the rectifier diode might be burned off).

Over-temperature

When the die temperature goes to about 160°C, the whole circuit of the ACT5880 is shutdown, including all function blocks, with about 20°C hysteresis when temperature falls for recovering. This threshold temperature is higher than functional temperature thresholds used for other temperature dependent circuits, including the die-temperature regulation in charger and the open-drain driver circuit.

House-keeping Oriented Interrupts

There are 14 sources/conditions in 2 types interrupt oriented for house-keeping, each is programmable for allowing interrupt or masked.

Table 2 lists the house-keeping oriented interrupt types. Refer to the *INTERRUPT DESCRIPTIONS* section for a summary of all possible interrupts and the *REGISTER AND BIT DESCRIPTIONS* section for more details.

Table 2:

The House-keeping Oriented Interrupts.

INTERRUPT FOR	CONDITIONS
System Voltage low	V_{VSYS}<Voltage set by SYSLEV[3:0]
Regulator out of regulation	REG1, REG2, REG3 output 7% less than normal; REG4 to REG13 11% less than normal; REG3 over voltage in constant current output mode.

STEP-DOWN DC/DC REGULATORS

General Description

REG1 and REG2 are fixed-frequency, current-mode, synchronous PWM step-down DC/DC converters that achieve peak efficiencies of up to 97%. These regulators operate at a fixed frequency around 2MHz, minimizing noise in sensitive applications and allowing the use of small external components. Additionally, REG1 and REG2 are available with a variety of standard and custom output voltages, and may be software-controlled via the I²C interface for systems that require advanced power management functions. Finally, REG2 features a unique SLEEP mode function that significantly reduces quiescent power consumption yet maintains a regulated output voltage that can supplies up to 10mA nominal (50mA maximum).

By default, REG1 and REG2 operate in fixed-frequency PWM mode at medium to heavy load, then transit to a proprietary power-saving mode at light load for having better efficiency. In applications where low noise is critical, fixed-frequency PWM operation may be retained across the entire load current range (in compromising of the light-load efficiency) by setting the respective MODE[ ] bit via I²C.

REG1 and REG2 are capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

REG1 has 2 banks of registers for setting the output voltage, with the VSEL input to select to output voltage set in which bank.

REG2 has a buck unit and a synergetic linear regulation unit, which is designed to replace the buck unit in light load operation. The linear unit has almost the same programmable features as an LDO, but with a bit to program if to turn on when the buck is tuned off, and it should not be set to active discharge in shutdown.

Manipulation

The output voltages and few other operation options of REG1, the buck unit and synergetic linear unit in REG2 are programmable through the I²C operation. Refer to the REGISTER AND BIT DESCRIPTIONS section for details and the step-down DC/DC converter and LDO Voltage Setting for the code to voltage cross.

Summary of key specifications

Table 3:

Key Specifications of Step-down DC/DC Converters

PARAMETER	VOLUME
Operation Voltage	2.7V to 5.5V
Active Mode Quiescent Supply Current	65μA
Sleep Mode Quiescent Supply Current	23μA
Shutdown Current	1μA
Default Output Voltage	1.2V and 1.2V/REG1, 1.8V/ REG2
Output Range	0.6V to 3.9V
Maximum Output Current	1.2A/REG1, 0.6A/REG2
	10mA/REG2 in Sleep Mode

Soft-Start Step Transient

Both REG1 and REG2 implement constant slope control for soft start ramping in 400μs nominal, as well as the step up transition for outputting two different voltages. This assures no overshoot during start up and changes of voltages. The output voltage drop is load condition dependent during turning off or step down transition.

REG2 Sleep Mode

When set the EVENT4 bit of the system register, the buck operation of REG2 stops and the linear regulator unit starts smoothly with no dropping at output. When the "Enable Key" is pressed or the EVENT4 is cleared, the REG2 is set back to buck operation and the linear regulation unit stops, also in seamless smooth transition. The EVENT4 bit should be cleared by software when wanting the REG2 resumes from the sleep mode to normal mode.

When REG2 is set off before the set of EVENT4, the assertion of EVENT4 starts REG2 in sleep mode. In this condition the clear of EVENT4 sets the REG2 off, without turning it into buck operation.

Irregular Conditions

Both REG1 and REG2 are output short-circuit safe. The over current protection and the over temperature shutdown protection prevent the ACT5880 from being damaged by thermal over stress. When the output voltage drops about 7% off the normal output voltage, the OK bit for the regulator is cleared. When interrupt is unmasked,

this change asserts interrupt to alert the system for out of regulation.

Component Selection

Each step-down DC/DC regulator utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Inductor Selection

The inductors with inductance 1.5μH to 2.2μH for REG1 and 1.5μH to 3.3μH for REG2 are recommended.

Input and Output Capacitor Selection

REG1 and REG2 are designed to operate with small 22μF~27μF and 10μF~22μF output capacitors respectively, over their output voltage ranges. The input bypass capacitors sink the quick component in current, help in suppressing of EMI and improving the efficiency. Capacitance in range 2μF to 10μF is commonly sufficient. X5R and X7R dielectrics are recommended for those capacitors for their suitable and stable characteristics to better performance.

PCB Layout Considerations

The high frequency element in the inductor current alternates between the switch ground path and the input bypass capacitor ground path. Place and route the two paths close, then place the ground end of output capacitor close to them, then place the inductor close is the better order in layout design. Though the practice is difficult to place all components close to the ACT5880, it is necessary to give the step-down DC/DCs the priority for closer placement.

CONFIGURABLE STEP-UP DC/DC REGULATOR

General Description

The step-up DC/DC regulator in the ACT5880 is factory-programmable for the options of operation in voltage regulation mode, constant current mode and negative output mode, which are options against ordering.

The step-up DC/DC has 80ns typical minimum on-time and 40ns minimum off-time, with the flexible factory programmable loop compensation and slope compensation, could output in large dynamic range from slightly high than input to 40V.

The output voltage in voltage regulation mode and the over voltage protection threshold, the switch operation to the system clock phase alignment, and the turn-on delay time are configurable though the I^2C interface. The circuit is enabled and starts to output after the specified turn-on delay when the ON[ ] bit is set to 1. When the ON[ ] is cleared, the step-up DC/DC circuit is shutdown.

When the interrupt function is not masked and the power ok condition is not met, the circuit asserts interrupt. The power ok condition for the voltage regulation mode is that the output voltage is within 7% of the normal output voltage. For the constant current mode, the power ok condition is the over-voltage does not occur. The interrupt function is masked by setting the nFLTMSK[ ] bit. The over-voltage detection monitors the voltage seen at voltage feedback error amplifier input, with an threshold about 30mV to the 1.2V reference voltage.

When the on-time or off-time of the switching is close to the respective minimums, pulse-skipping happens to stay in regulation, which is normal when the input voltage and the output voltage are too close or too far.

See the *STEP-UP DC/DC VOLTAGE SETTING* table for VSET code to voltage cross. This code to voltage cross applies to both the output voltage and the over voltage threshold.

Voltage Regulation Option

In voltage regulation mode operation, the output is sampled at the OUT3 pin with an internal divider network. Figure 5 shows the internal block diagram and the external circuit for the step-up DC/DC in voltage regulation mode.

Current Regulation Option

In current regulation mode operation, the current is sensed in the sinking path at the low end current sense resistor tap. The voltage on the sense resistor is regulated at 200mV, the output current is then derived from the resistance and this 200mV volume. Figure 6 shows the internal block diagram and the external circuit for constant current operation.

The output current can be controlled by feeding a voltage DIMMING into the resistive network composed of RCS, RDM1 and RDM2. The DIMMING voltage can be an analogue signal or a logic signal, which implements analogue current control or PWM on/off control to the current output. When using a logic signal as DIMMING for turning on and off the constant current output, the on and off delay limits the maximum available frequency used for dimming, which is typically less than 2.2kHz. Refer to the waveform captures in *TYPICAL PERFORMANCE CHARACTERISTIC* section for more details.

Figure 5:

The REG3 Circuit for Voltage Regulation Mode.

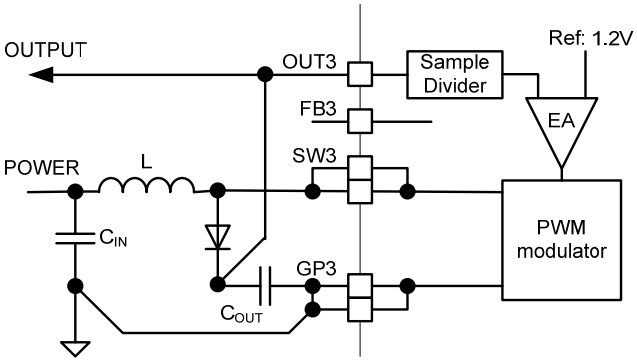
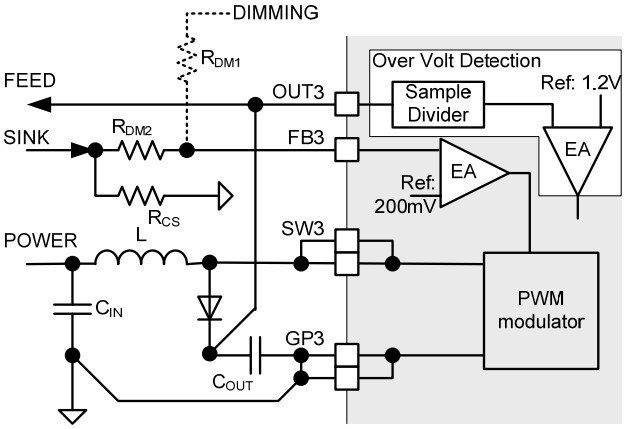


Figure 6:

The REG3 Circuit for Current Mode.



Inversion Regulation Option

When programmed as an inversion regulator option, the error amplifier in the FB3 feedback path is phase inverted for the negative output regulation. An external positive reference voltage is employed for bias an external divider, whose tap connects to the FB3. The voltage at FB3 is still regulated at 200mV in inversion application.

Irregular Conditions

When the load condition, or input to output ratio pull the output out of regulation, the switch current limit prevent the circuit from over stress. As the rectifier diode is serial in the output path, short the output to a voltage lower than input voltage would cause excessive high current through the diode and might damage the diode. Current limit switch or thermal fuse is desired if there is possibility of shorting the boost output.

Component Selection

Table 4 lists the suitable component specifications. The better high frequency performance is important to both inductor and capacitor. Capacitors with X5R or X7R serial dielectrics are recommended.

The inductor DC saturation current should be at least 30% over the limit of switch current. For applications that do not require high current, options with lower current limit are available upon ordering, which is necessary when selecting the inductor with smaller saturation current.

Table 4:

The Components Selection for REG3.

Operation conditions	L (μH)	C_{OUT} (μF)	C_{IN} (μF)
Voltage, 500mA, 5V	10~15	22~27	2.2
Voltage, 35mA, 40V	22	0.68	2.2
Current 35mA, 40V	22	0.47	2.2
Current 100mA, 20V	15	0.68	2.2

PCB Layout Considerations

The inductor current alternately goes into the output capacitor and the power switch, place the output capacitor close to the switch node SW3 and connect the capacitor ground to the same current loop back node GP3 would reduce the risk of excessive noise conducting. Practically it might be difficult to place all components close to the chip. When the available space is constraint, the order for being close to the chip is the rectifier diode, the output capacitor, the inductor and then the input capacitor.

LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

General Description

There are total 13 low drop-out linear regulators in the ACT5880. Except for the one for backup battery charger and the always-on LDO, the rest 11 LDOs have similar way to control and to program through the access of sets of registers, but the one tied for REG2 has an additional control access though a joint manipulation. Refer to Table 5 for a quick summary of output currents and default output voltages for each LDOs.

Table 5

The Key Specifications of LDOs.

NAME	DEFAULT STATUS	DEFAULT OUTPUT(V)	MAXIMUM OUTPUT (mA)
REG4	ON	2.9	360
REG5	ON	2.9	250
REG6	OFF	2.9	360
REG7	ON	3.0	360
REG8	ON	2.5	360
REG9	OFF	1.2	250
REG10	ON	3.3	150
REG11	OFF	1.8	80
REG12	OFF	1.8	250
REG13	OFF	2.8	150
LDO tied in REG2	OFF	1.8	10
Backup Battery Charger	ON	2.7	5
Always-on LDO	ON	1.8	3.5

The OUT6 and the OUT9 also have pin control inputs for controlling their on/off together with the on/off bit controls through the register access. When both the ON bit and ON pin input are used for control, the later change takes effect. Upon the power up, if the default of ON bit is different than the ON pin input, the OUT is ON. In other words, the OUT upon power on is off only both the ON bit and ON pin input are set for off. This arbitration is enough and does well to most cases. However, if one input sets the OUT to have a status that it already outputs for in the condition that the OUT sets for the complementary status by other input, the input should send out a toggle, instead of repeat the same logic volume.

Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

Configuration Options

Output Voltage Programming

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I^2C serial interface as shown in the STEP-DOWN DC/DC and LDO OUTPUT VOLTAGE SETTING table.

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I^2C interface by writing to that LDO's ON[ ] bit. To enable the LDO set ON[ ] to 1, to disable the LDO clear ON[ ] to 0.

Output Discharge

Each of the ACT5880's LDOs features an optional output discharge function, which discharges the output to ground through a 1kΩ resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ] via; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it.

Low-Power Mode

Each of ACT5880's LDOs features a LOWIQ[ ] bit which, when set to 1, reduces the LDO's quiescent current by about 30%, saving power and extending battery lifetime.

OK[ ] and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, the value of that regulator's OK[ ] bit will be 0.

If a LDO's nFLTMSK[ ] bit is set to 1, the ACT5880 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until the OK[ ] bit has been read via I^2C.

The Always-on LDO and the Backup Battery Charger

Two regulators are specialized for always-on powers, as a backup battery charger and a low voltage, low quiescent current always-on regulator. The backup battery charger is a low power voltage regulator with preset current limit of up to 5mA nominal as a constant-voltage and constant-current charger. If applications like the RAM data keeping requires larger current option, contact factory for ordering.

The always-on LDO and the backup battery charger have programmable output voltages, which are set individually as other LDOs but the backup battery charger uses different code to voltage cross as what in the *VBBAT OUTPUT VOLTAGE SETTING* table. As the VBBAT is internally connected to power the always-on LDO, and the always-on LDO powers the RTC, if the RTC function is used, the outputs of both regulator should have enough headroom for the RTC operation.

The backup battery charger LDO outputs at slightly lower voltage than the code voltage with a current related drop before it falls into current regulation, which would have output the exact code voltage when the output current were zero. This drop has close to logarithmic trend to the load current (i.e., doubled every decade change of load current).

Typically the backup battery charger input, the BBCIN connects to the main battery; Its output, the VBBAT connects to a backup battery coin cell or a super cap, charges and floats at the programmed voltage. Its precise voltage setting and current setting accommodate to various battery chemicals of 1.5V to 3.6V output and super caps. When the input power removes, the backup battery charger turns itself shutdown with almost 0 leakage backward from the cell.

The input of the always-on regulator is internally routed to available powers, which is the internal bias in the ACT5880, the VSYS, or the VBBAT. The always-on regulator output is internally connected to power the RTC block. When the RTC function is enabled, the minimum voltage to start oscillation or to maintain the RTC functional is greater than the minimum available programmable output voltage.

The data in register bits for the always-on LDO output voltage setting are kept until both the system power and VALIVE fail.

Two accesses are designed for change the VBBAT regulation voltage. The first access is to set UNLOCK bit, to allow the change to the voltage configuration byte, then the VBBAT is changed by writing to the byte. It is highly recommended to reset the UNLOCK bit after each writing, to avoid possible accidental change to the voltage setting for VBBAT.

For configuration and manipulation, refer to *THE REGISTERS and BITS DESCRIPTION* for detail.

Irregular Conditions

The LDO circuit monitors the output and asserts interrupt if out of regulation happens, if the function is allowed. When short circuit or over current happens, the output current limit folds back to about the 0.45 times of the maximum output current. Each LDO is safe in output short circuit.

The individual LDO does not have its own over temperature protection circuit. Subject to the whole die's thermal condition, the LDOs are turned off when die over temperature happens.

Component Selection

Input Capacitor Selection

Each LDO requires a small ceramic input capacitor to supply current to support fast transients at the input of the LDO.

Output Capacitor Selection

Each LDO requires a small ceramic output capacitor for stability. Each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection.

The input and output capacitor values are listed in Table 6. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Table 6

Component Recommendation for LDOs

LDO NAME	OUTPUT CAP (µF)	INPUT CAP (µF)
REG4, REG6, REG7, REG8	3.3	1
REG5, REG9, REG12	2.2	1
REG10, REG13	1.5	1
REG11	1	1
LDO tied in REG2	1~1.5	-
Backup Battery Charger	1~1.5	-
Always-on LDO	1~1.5	-

PCB Layout Considerations

PCB Layout Considerations The ACT5880's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

OPEN-DRAIN DRIVERS

The ODO1, the ODO2 and the ODO3 are open-drain drivers, which could operate as simple open-drain outputs, or as constant current sinkers, set by individual configuration. Each of them could also output in PWM pattern for extended output power adjustment range. One of the driver output, the ODO1, has high operation voltage range of up to 40V and the other 2 have the ranges of up to 5V, make them flexible and powerful.

Each driver is configured and manipulated through the access to respective register bit. Refer to *THE REGISTER BIT DESCRIPTION* for more details.

The BUFFER bit sets how a current setting or PWM duty cycle affects the output. When the BUFFER is set to 0, the data written into the respective current or duty register affects the output instantly; When it is set to 1, the data written into the register does not affect the output until the bit is set to 0. This BUFFER bit has power over all the 3 drivers, which makes the outputs of drivers change simultaneously, independent to when the data is set.

Operation Modes

Constant Current Driving

The current is set by configuring the weight for LSB and a 6 bits current code. Combining the weight and the current code, the adjustment to current for each driver covers 0 to 100.8mA nominal.

PWM Switching

Each driver could be turned on and off with an internal generated PWM pattern at nominal 244Hz. The duty cycle of PWM pattern is either linear coded or non-linear coded, optioned against ordering. If linear coded, the duty cycle is the ratio of the integer volume put into the duty register over 255. See respective tables for non-linear coded duty cycle setting and the register setting. Figure 7 shows the duty cycle to code plot for both the linear and non-linear code, with an exponential curve for reference.

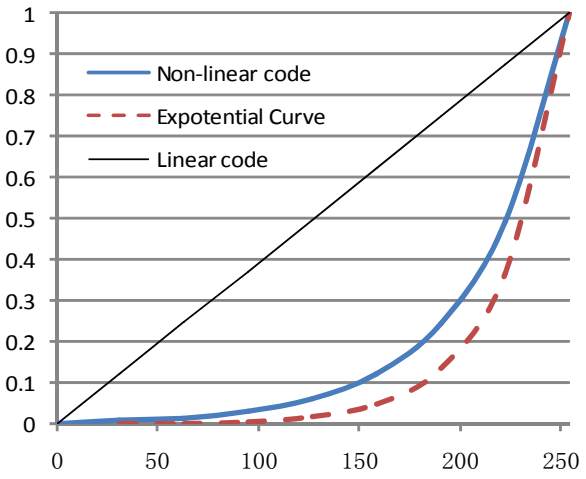
The non-linear coded duty cycle setting provides a close to exponential code to brightness approximation, which gives similar feeling difference in changing the code linearly, against the Webber's law.

Phase Shift and Delay

In case of driving backlight assembly with long wire and close to the EMI sensitive LCD display, both PWM phase shift and sequential on are implemented in the driver circuitry additional to the current-on slew rate limit of 40mA/μs nominal, which assure no flicker, no fake operation in various size for high quality image display.

Figure 7:

The PWM Adjustment Curves.



Combined Modulations

The PWM pattern could modulate the constant current output on and off, as well as the simple open drain output on and off. The combined modulation extends the dynamic range for backlight brightness adjustment. For multi-strings backlight application, the current setting could be used for matching different strings while the PWM is used for overall brightness control.

Inductive Load

For inductive load driving, like driving a vibrator motor, an external dump clamp diode is desired to avoid voltage overstress by current breaking voltage surge caused by the serial inductance. As specified in the characteristics table, the drivers have a controlled current on slew rate of 40mA/μs nominal. This slew rate control only applies on the turning on of the current, not on the turning off.

Irregular Conditions

The driver block has her own overheat monitoring, with a threshold temperature lower than the over temperature shutdown threshold. If overheat is detected in this block, the drivers are turned off before the system is possibly forced into thermal-shutdown. Each driver also has a LED open detection circuit, which monitors the driving level of the output stage. When it is driven saturated, then

an open-LED is detected presumably. The overheat and open-LED situation does not send out signal to alert the system, the system could identify the situation by ready respective bits in the ODO register (0x79).

Low LED bias voltage or high serial impedance may cause false reading of an open LED situation. The host system needs other measures to verify the true situation and takes action accordingly.

This open LED detection function provides a way of driving headroom detection for making adaptive backlight driving, which is biasing the LED with a voltage just enough for maintain the wanted current.

Typical Application Consideration

With the thoughtful function design and the parameter design, the driver circuit in the ACT5880 provides high flexible and rich solutions for design trade-off. The range of constant current, the range of voltage and its programmability are enough to most mobile backlight applications with up to 7" display.

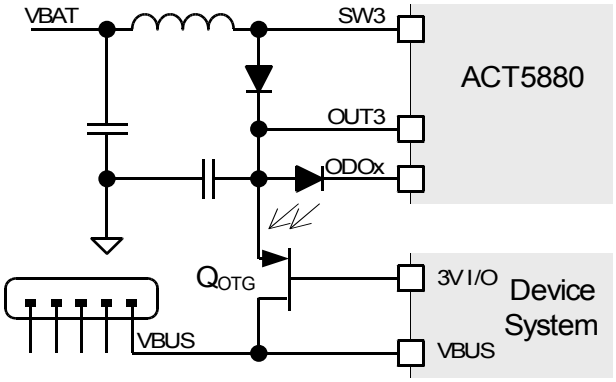
The thermal constraint of the ACT5880 plays the limit of effective use of its capability. Cooperation between the programmable step-up DC/DC of the ACT5880 and the adaptive headroom management could realize the feasible thermal design for high power backlighting of up to 100mA and 40V.

The mix-modulation to power output brings another approach of adaptive backlighting, which is to draw the possible maximum current from a bias power with varying voltage such as a battery by checking if the headroom is sufficiently kept, and stabilize the light output, what is the product of current and PWM duty ratio, by change the PWM duty ratio.

Figure 8 shows a sample of how this approach is used in a slightly different way, which is meaningful sample of how the comprehensive use of the ACT5880 capability benefits the application. In the circuit, the step-up DC/DC output is used to bias the WLED, and to power the USB OTG port as well. The WLED forward voltage drop is in range of 2.8V to 3.8V typical, dependent on LED temperature and brightness wanted. During the backlight only operation, the step-up DC/DC output should be adaptively set to a voltage for maintaining proper headroom on the driver output, in which the voltage is normally less than 5V. During powering the OTG port, the step-up DC/DC outputs 5V, in which case a large drop on the LED driver is seen. For reducing the thermal generated in the driver, the constant current should be increased as high as possible, and as such the drop on driver decreases, while the PWM duty ratio is reduced for maintain the stable brightness.

Figure 8:

A Sample Circuit for the OTG Power.



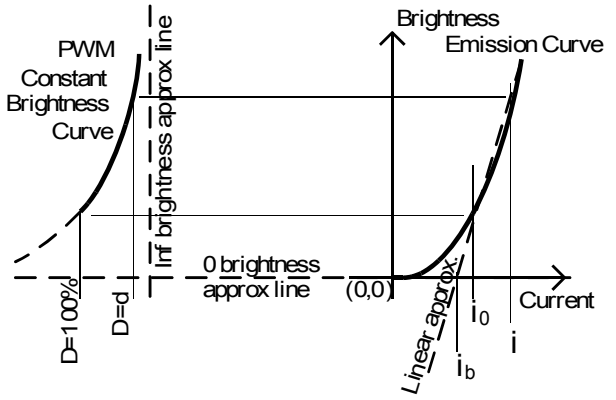
The duty ratio d for keeping the same brightness is the function of the current i, the current at 100% duty ratio i_0, and a constant i_b, as showed in the equation below:

$d=(i_0-i_b)/(i-i_b)$

where the i_b is a characterized parameter for a given LED type from the test of finding the duty ratio d_m at a current i_M for keeping the same brightness, in which the volume of i_M used should be close to the available maximum current in the particular circuit. The curves and their linear approximations for deriving the equation are shown in Figure 9.

Figure 9:

Deriving Adjustment for Maintaining Brightness.



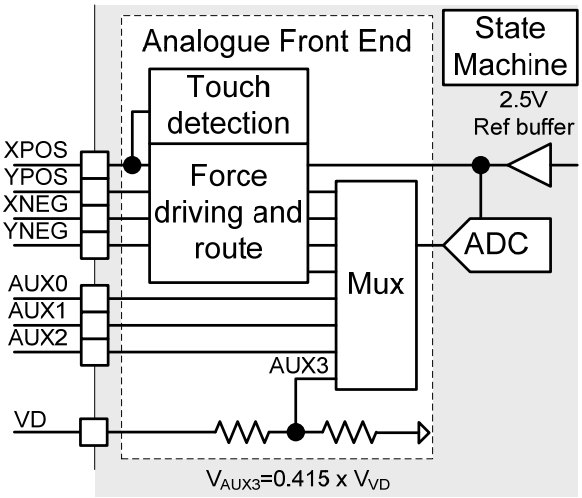
TSC ADC

The ACT5880 has a shared SAR ADC with a state-machine for deploying actions to do resistive touch panel measurement as well as normal ADC conversion. The features and performance of the circuit are optimized for applications with hand-held size touch panel and related housekeeping. The shared ADC core has 12 or 8 bits resolutions, assures that it fits both the position measurement and the contact evaluation.

The touch screen measurement circuit employs an analogue front end and a touch detection circuit with acquisition management, makes the circuit a full function TSC (i.e., the touch screen controller). Refer to Figure 10 for the top level block diagram of the TSC ADC circuit.

Figure 10:

The TSC ADC Block Diagram.



The analogue front end is designed to provide force driving bias and signal routes for 4-wire type resistive touch panel and the auxiliary inputs for common purpose ADC. Both the touch panel measurement and the common purpose ADC conversion are organized to manipulate with operation to same sets of registers, the state machine controls scanning to get each signal converted in a sequential frame or doing a single channel conversion, as it is programmed. Refer to *Acquisition Configuration* for details. And refer to Table 7 for the key specifications.

4-wire Touch Screen Interface

The TSC ADC has following internal connections for touch screen force and sense, as showed in Table 8.

Table 7:

The Key Feature of the TSC ADC.

PARAMETERS		
Resolution (bits)		12 or 8
Input Impedance		11MΩ
Input Capacitance		32pF
Force Driving Voltage and ADC Reference		2.5V
Maximum Force Driving Current		18mA
Full Scale Input Voltage	AUX0, AUX1, AUX2	2.5V
	AUX3(VD)	6.024V

Table 8:

The Touch Screen Interface Connections.

XPOS	XNEG	YPOS	YNEG	CHANNEL	DESCRIPTION
PEN	Hi-Z	Hi-Z	GND		Standby
ADC	Hi-Z	2.5V	GND	0	Y-coordinate
2.5V	GND	ADC	Hi-Z	1	X-coordinate
ADC	GND	2.5V	Hi-Z	2	Z2-coordinate
Hi-Z	GND	2.5V	ADC	3	Z1-coordinate

Notes:

PEN: The pen touch detection connects to this pin;

2.5V: The 2.5V reference buffer output;

ADC: One of the ADC channel input.

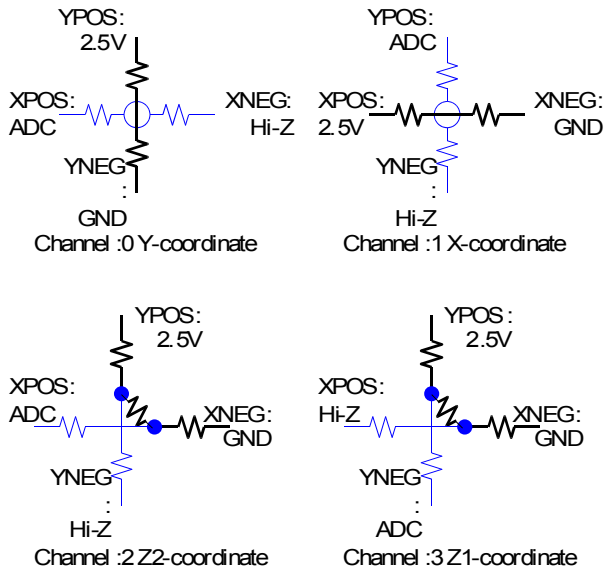
The respective force and sense to touch panel is shown in Figure 11.

The resistors lay in vertical and horizontal represent the equivalent resistances of the transparent films split by the touch spot, the resistors lay oblique is the equivalent of the films contacting in the touch spot, the paths in bold are the force current goes through. Considering the current into the ADC input is neglecting comparing the force current and the even gradient slope of potential in the area between two bias bar, the channel 0 and channel 1 read exact the electrical equivalent coordinates in the axes (the electrical equivalent coordinates then are scaled to graphic user interface coordinates by the application software). Giving the 3 equivalent resistors in the force paths for the channel 2 or channel 3 connections make the Z axis, the channel

2 and channel 3 read the 2 coordinate equivalences Z2 and Z1 on Z axis. These Z2 and Z1 are used for contact evaluation; Refer to *Contact Evaluation* for more details.

Figure 11:

The Simplified Circuits for Touch Screen Measuring.



Touch Detection

When the function is enabled, the touch detection circuit measures the contact between two film layers of the touch screen panel. The detection circuit only biases the XPOS in standby when no any conversion in progress and no conversion result waiting for system to read. When contact between 2 film layers happens, a touch event is detected and an interrupt asserts for request system service. The layer to layer coupling may cause false touch detection when applying the bias, the first touch event right after applying should be ignored.

A wake-up against pen touch detection function is designed for further power saving in applications like E-book, in which the main processor may power off. To enable this function, the PENWKEN bit needs to be set and the TSC ADC circuit needs to be powered independently to the operation of the ACT5880, such as being powered with battery directly.

Contact Evaluation

The (Z1−Z2) read the resistive divide ratio of the contact impedance over the whole force path impedance. As the film resistors in the path are coordinate dependent, the (Z1−Z2) are consequently X coordinate and Y coordinate dependent. The linear estimation on the film resistor impedances are used to normalize the (Z1−Z2) to proportional factor C to one of the two film impedances. As a sample, giving the effective dimensions of the touch films is 1:F for X-dimension to Y-dimension ratio and the X film impedance is 1, the Y film impedance is then F and the film thickness is same; Also giving the full scale reading is FS, the Y film resistor impedance in the path is (FS−Y)·F, the C is derived as:

$$C=(Z1-Z2)\cdot[X+(FS-Y)]/[FS-(Z1-Z2)].$$

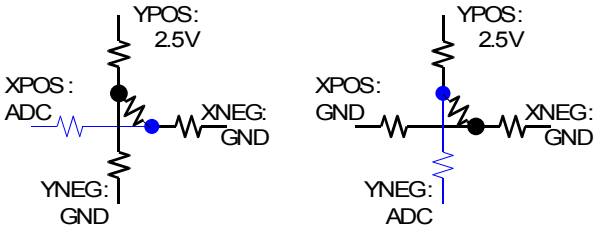
The volume C represents the tightness of contact in the touch spot, which is proportional to the touch pressure and touch area size.

The high resolution conversion, the reference buffer force driving and the flexible acquisition features make the ACT5880 suitable for contact evaluation applications like finger touch and fingers touch. The finger touch has low contact impedance than the round tip touch; the C volume can be used to detect the finger touch.

With two additional I/O pins to pull the Hi-Z pins in channel 2 and channel 3 connections to ground separately, the equivalent span changes of the touch spot on X axis and Y axis can be evaluated, so forth the 2 fingers wiping shaped touch is identified. See connections in Figure 12 for reference.

Figure 12:

The 2 Fingers Touch Measuring.



Y touch spot span evaluation , the YNEG grounded during Channel 2 measurement.

X touch spot span evaluation , the YNEG grounded during Channel 3 measurement.

Internal Reference

The TSC ADC circuit has an internal reference buffer to generate a 2.5V reference voltage for the ADC circuit and the force driving in the analogue front end. This reference is user trim-able for getting better accuracy is necessary. Refer to the *REGISTER AND BIT DESCRIPTIONS* section for more details.

TSC ADC Registers

The conversion manipulation and the configuration are all user accessible through the register bits writing or reading. Purposes of most register bits are straight and clear, refer to the *REGISTER AND BIT DESCRIPTIONS* section for detail.

Acquisition Configuration

The whole TSC ADC circuit could be disabled by setting the nEN bit for reducing the operation current. For any TSC ADC operation, clear the nEN bit to 0 firstly.

The acquisition configuration includes how an acquisition is started, how conversions are grouped in an acquisition, the conversion length selection, the calibration time selection, the conversion clock divider selection, and selection of sampling to conversion start delay.

The analogue front end only provides force driving to the touch panel when the group scan to touch screen interface is selected, which reduces the power consumption for driving the panel when it is not measured. When the group scan is not selected, 3 of the 4 touch screen interface pins could be used as normal input path for ADC.

Interrupts and Status Bits

If not masked, interrupt is asserted when a touch is detected and/or an acquisition is done and the result waits for being read. Each of the interrupt conditions could be masked by its mask bit and the status of the detection and acquisition could be read through the I^2C interface, regardless if it is masked. Refer to the *REGISTER AND BIT DESCRIPTIONS* section for detail.

Application Program Consideration

Touch spot tracking desires intensive computing. Dynamic processing resource allocation and interrupt mask reconfiguration are necessary to accelerate the tracking process.

Before any touch press is detected, the TSC ADC is set to wait for touch press event and to assert interrupt when a touch is detected. When touch press is ever detected, the pen-touch detection interrupt should be masked and the interrupt disposing routine should initialize for a polling routine which starts conversion and reads result with a fix time interval.

When applying the force voltage onto one layer of the touch screen, a coupled voltage is seen at another layer through the layer to layer capacitance if there is no effective resistive leakage path at the another layer. This mechanism causes a false touching at the first time enabling the pen touch detection function, which should be ignored by application software. This mechanism also causes false reading of around center point touching if reading without touching detected firstly. There is no false reading in automatic conversion operation when the nAUTO[ ] is cleared to 0, where the conversion starts only when touching is detected.

REAL TIME CLOCK

The real time clock or namely the RTC circuit in the ACT5880 is powered by the VALIVE output of the always-on LDO. The circuit includes a crystal oscillator running with 32.768kHz quartz resonator, a rank of counters and manipulation interface. The RTC time counts for seconds, minutes, hours and days, alarms against comparison of second, minute and hour, outputs a square wave at its oscillator's frequency, asserts interrupt or wakes up the system if it is configured so. The data settings and the configuring are through I^2C operation. Refer to the REGISTER MAP AND DESCRIPTIONS section for details.

A bit in the control register, RTCEN[ ], enables the RTC circuit when it set 1, whose default is 0. Whenever power loss happens, it returns to 0 to disable the RTC counter. It is necessary to check this bit to assure the RTC runs normally before taking the time from the RTC. The oscillator and the square wave output are not affected by this bit, which keeps operation until it could works.

Crystal Selection

A precise 32.768k clock crystal is required to run the oscillator. The oscillation circuit works properly with large variety of load capacitances, C_{L1} and C_{L2} in range of 5pF to 30pF. The maximum serial resistance R_S of the crystal for having stable oscillation is about 60kΩ to this device, while the less serial resistance is the easier to starting and maintaining oscillation. Commonly, the bigger size crystals have less serial resistance. For small size SMD crystal, an external shut resistor is required. Table 9 lists few crystal models and the external component parameter suggested. Refer to Figure 13 for the circuit diagram.

Table 9:

Typical Crystal Parameters.

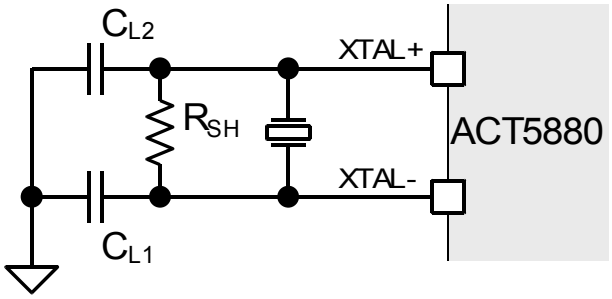
MODEL	C_{L1}, C_{L2} (pF)	R_{SH} (MΩ)
MC-146	10 (7~15)	5.6 (4.7~8.2)
TXC 9H03 2000 10		
AB38T		

RTC Interrupt and Wake-up

The RTC can be configured to assert interrupt and/ or to wake-up the ACT5880 from disabled state or deep sleep state. When the hour counts, the minute counts and the second counts all match the alarm time set in respective registers, interrupt asserts in normal operation or wake-up the ACT5880, then to wake up the host system, just as if a power-on button press event happens. To enable the alarm function, 2 control bytes, 0x3C and 0x3D need to be set to 0x80 and 0x08 respectively first, then set the RAAI[ ] bit and clear the nWKALM[ ] bit.

Figure 13:

The Crystal Oscillation Circuit.



When an interrupt occurs, its assertion is kept until the 0x3C is read for clearing; an internal latch circuit enabled by the nWKALM[ ] bit (=0) forces an on-state for possible wake-up, which also generates and holds both nIRQ and nPBSTAT low. The nWKALM[ ] bit has to be set 1 to release the forced on state and the nIRQ low state after the alarm, to allow other signals like PWRHLD to take control of power state again.

Following is a sample of setting RTC alarm or wake up functions:

To enable the RTC wake-up alarm:

Set RTCEN[ ]=1 to enable the RTC running;

Set low 8 bits of Day by writing 0xB0, high 8 bits of Day by writing 0xB1;

Set Seconds/Minutes/Hours by writing 0xA4, 0xA8, 0xAC;

Set RCL[ ]=1 to load counters;

Set byte 0x3C to 0x80;

Set byte 0x3D to 0x08;

Set alarm Seconds/Minutes/Hours by writing 0x90, 0x94, 0x98;

Set nWKALM[ ]=0, RAAI[ ]=1 to enable the alarm.

To clear the RTC wake-up alarm interrupt:

Set bit nWKALM[ ] = 1 ;

Read byte 0x3C;

Read byte 0x3D.

To disable the RTC wake-up alarm:

Set bit nWKALM[ ] = 1;

Set bit RAAI[ ] = 0.

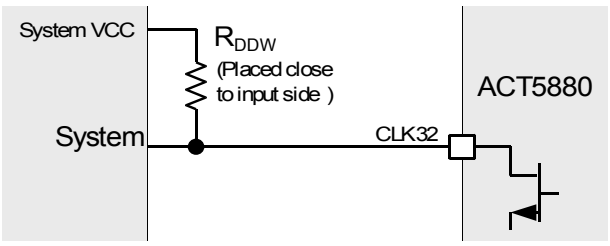
And every change interrupt is also available in the ACT5880, enabled by setting respective register bits of the RDAI[ ], RHAI[ ], RMAI[ ] and RSAI[ ]. This functions helps in maintaining the clock display refresh against the day counts changes, the hour counts changes, the minute counts changes and the second counts changes. When the every change happens, the interrupt output is kept for 0.5s for second change, for 1s for minute change, hour change and day change. Resetting respective enabling bit to 0 clears the interrupt output immediately.

Oscillator Square Wave Output

The CLK32 is the shaped output of the oscillator, an open-drain output that requires an external pull-up resistor. The pull-up resistor is pulled-up to the same rail that powers the circuit that wants the clock input, is easy for logic level interfacing between the RTC circuit and the system. The pull-up resistance is selected against the edge slope rate wanted and the parasitic capacitance of the connection, which is typically in range of 7pF to 35pF for pins and normal trace width of 5mil to 10mil and length of 400mil to 1000mil. Typically, a 300k resistance is the highest volume acceptable to most systems and placing the resistor close to the input pin provides slightly better performance. Refer to Figure 14 for the circuit diagram.

Figure 14:

The Output Circuit of the CLK32 Output.



SINGLE-CELL LI+ BATTERY CHARGER

The charger circuit in the ACT5880 deploys the constant current and constant voltage scheme for charging, with pre-condition charging and suspending. Most parameters for CC/CV control is programmable, together with the battery installed detection, the adaptor charging detection, the battery thermal condition, the die temperature regulation, the charging time-out counters and the LDO mode operation, it composes an autonomic-able, flexible yet powerful battery management sub system, which satisfies most applications.

Program and Manipulate

Most of the charging profile control parameters are programmed by writing respective registers though the I^2C interface. The charge states, the logic inputs are read and the charge behavior is manipulated through the same interface by reading or writing respective bits.

Most programming and manipulation are done with one time access to respective register. For changing the battery regulation voltage and the fast charger current, which are safe related, an enable bit, the ENVISET[ ] register has to be set firstly, to avoid the accidental change. Refer to the *REGISTER AND BIT DESCRIPTIONS* section for more details.

Power Path Management

The ACT5880 has simple power path management. Refer to Figure 15, the charger only has one controlled path for pre-condition charging, fast charging and providing power to the load. By any time, the regulated voltage and regulated current apply to the load and the battery simultaneously. The load directly pours current from the battery or from the charge path, provides the most efficient way of using the energy stored in the battery.

This is the most common path management in cellular phone and smart phone designs. Few issues need to be carefully designed for the optimizing use of this path management:

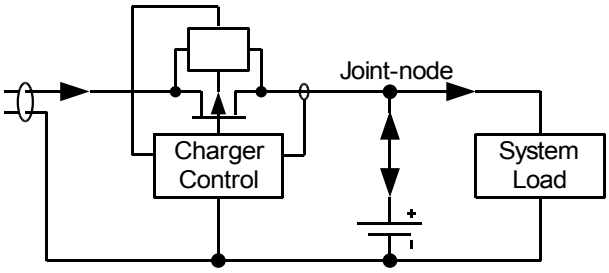
1.Start from a weak/dead battery;

2.Charging termination.

The ACT5880 provides rich of programmability and effective solutions for dealing with these issues against system designer's trade-off. The ACT5880 has a pre-condition timer and a total charge timer for safe charging of a weak/dead battery, and it does not start the system until the battery voltage is charged to high enough voltage. The ACT5880 itself is designed to start at as low voltage as the precondition finishes, which reduces the time to wait before start. Additionally, the ACT5880 provides a LDO mode for starting system without battery.

Figure 15:

The Power Path of the Charger in the ACT5880.



The ACT5880 provides rich of programmability and effective solutions for dealing with these issues against system designer's trade-off. The ACT5880 has a pre-condition timer and a total charge timer for safe charging of a weak/dead battery, and it does not start the system until the battery voltage is charged to high enough voltage. The ACT5880 itself is designed to start at as low voltage as the pre-condition finishes, which reduces the time to wait before start. Additionally, the ACT5880 provides a LDO mode for starting system without battery.

When the current goes into load is bigger than the current threshold for end of charge detection, the charging termination may never happen. The system operates in this situation, is known as long cord powered time operation. In this situation the system could program the charger to output at a slightly lower voltage for safe floating.

Adaptor Input Detection

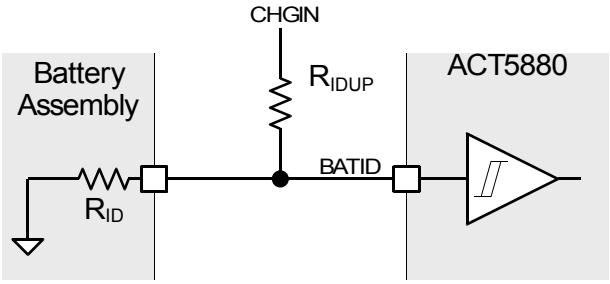
The ACIN is the detection of adaptor charging input, which is a logic input with precise logic thresholds. A resistor divider can be used for sensing the voltage applies at the adaptor input receptacle for simple detection. Ref to the "USB Charging" and "Dual Input and USB-OTG Paths" for detection of USB adaptor.

Battery Installed Detection

A grounded resistor in battery assembly is desired together with the BATID of the ACT5880 for the battery installed detection. The BATID is a logic input with higher voltage precise logic thresholds , please refer to the *SINGEL-CELL LI+ CHARGER ELECTRICAL CHARACTERISTICS* table for more details.

Figure 16:

The Battery Installation Detection Circuit.



Refer to Figure 16, the R_{ID} is known as battery identification resistor in many commodity battery pack designs, which is also used to identify the battery model for the system. The resistance of R_{ID} could be specified by ordering the battery pack, or be whatever the commodity battery packs have, for examples, the Nokia BLB-2 has a 68kΩ resistor and the Nokia BLC-2 has a 75kΩ resistor. The RIDUP is recommended to pull up to CHGIN, whose resistance is derived from the thresholds and the suitable charging voltage range.

The battery installed detection works only when there is suitable charging voltage applied on the CHGIN, no power loss occurs if not attaching onto an external power source. When there is an external power available at the CHGIN, the logic level at the BATID decides if to operate as a normal CCCV charger or to operate in LDO mode, in which the charger regulator works like a LDO for outputting the battery regulation voltage. When the voltage the CHGIN is higher than the "No Battery Installation Level" specified in the electrical characteristics table, the charger is in LDO mode, the maximum charge current still works to limit the maximum output current.

When the battery does not have an ID resistor, ground the BATID with a resistor to force the logic level is equal to battery installed for normal charge operation; Or connect it to an I/O of the system to allow the system to control the logic level.

CC/CV Charging Profile

The core of the charger is a state machine which manages the state transitions for the CC/CV charging with a precondition state. The state machine waits for the available condition for operation. If the input power is available and battery is detected, it monitors either the voltage at VBAT or the current through the charge path, and regulates either the current or the voltage, as the profile showed in Figure 17. The profile is showed in time plane with typical I and V change to time curves. The top-off portion of curves, which is in shorter period comparing to the fast charge period, are plotted with expended time scale for showing in detail.

Summary of Key Specifications

Table 10:

The Key Specification of the Charger Block.

PARAMETER	VOLUME	TYPE
Battery Regulation Voltage (V)	4.10 to 4.40	Programmable
Fast Charge Current (mA)	90 to 1000	Programmable
End-of-Charge Current Residual Ratio	10.00%	Fixed
Total Charge Time-out (minutes)	180 to 300	Programmable or Disabled
Pre-condition Threshold (V)	2.8	Fixed
Pre-condition Current (mA, or %/Fast Charge Current)	45mA or 10%	Fixed
Pre-condition Time-out (minutes)	40 to 80	Programmable or disabled
Operation Voltage (V)	4.2 to 6	Fixed
UVLO Voltage (V)	3.1, 4	Programmable
Over Voltage Threshold (V)	6.3 to 6.9	Programmable
Input Voltage Range (V)	0 to 7	Fixed
Regulation Die Temp(°C)	140 max.	Fixed
Hot Threshold, %	34.9	Fixed
Cold Threshold, %	74.8	Fixed

Charge Current Sharing

The charge current may go into the battery or the load, decided by their dynamic impedances. During Top-off state or floating, the fast voltage regulation loop puts most current into the charger path until the charge path current reaches the fast charge current limit, reduces the AC current into battery. This prevents the battery from aging caused by continuous passing AC current.

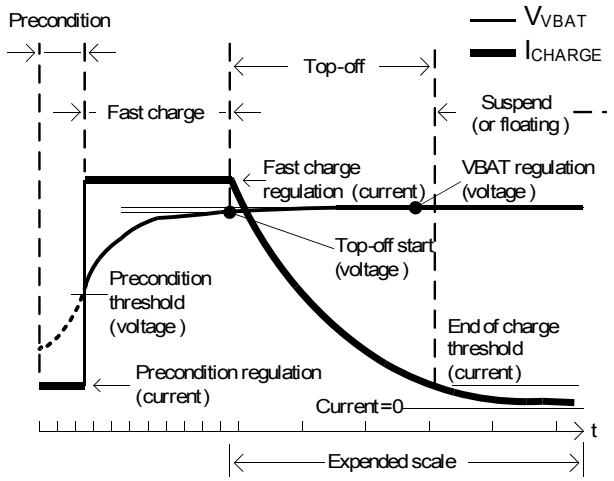
Thermal Regulation

The ACT5880 has an internal thermal feedback loop that reduces the charge current when necessary to ensure the die temperature does not

rise far beyond a thermal threshold of nominal 100°C. The current reduction is about 50mA/°C for die temperature over the threshold. This feature prevents the ACT5880 from excessive junction temperature and makes it more accommodating of aggressive thermal designs without risk of damage. When the thermal regulation reduces the current, it takes longer time to charge the battery. The thermal regulation is counted in end of charge detection, which assures that the battery could be charged to the same status as a normal charged battery when the end of charge detected.

Figure 17:

The Charging Profile of the ACT5880 Charger.



Charger State-Machine

The I and V parameter changes, input condition and the time-out outputs of 2 timers trigger the state transitions.

State Transition Table

The LDO mode is a lonely state when the BATID detection is configured and the BATID reads invalid. The other states are subset available when the BATID reads valid or the BATID detection is not configured. Refer to Table 11 for transition details.

Pre-condition State

When the V_{VBAT} is less than the precondition threshold voltage, the cell is charged at a reduced current of either 45mA or 10% of the fast charge current, whichever is the greater.

Fast-Charge State

When V_{VBAT} is greater than the precondition threshold and before it reaches to the battery regulation voltage, or over 200mV falls down from the battery regulation voltage, the charger operates in fast-charge state, when the cell is charged with the fast charge current, or a less current restricted by the thermal regulation and power source capability. Once the V_{VBAT} reaches the battery regulation voltage; the state machine jumps into Top-Off State.

Table 11:

The State Transition Summary.

CURRENT STATE	NEXT STATE	CONDITIONS
Any state	Sleep	$V_{CHGIN}<V_{VBAT}$, SUSCHG=1 or (total charge timer time-out)
Any state	Temp-Fault	Battery Temp Out of Range
Temp-Fault	Sleep	Battery Temp is OK
Pre-condition	Time-Fault	Pre-condition timer times-out.
Time-Fault	Sleep	Presumably battery replaced.
Sleep	Fast-Charge	SUSCHG=0, V_{CHGIN} valid and $V_{VBAT}<$ (BRV-200mV)
Pre-condition	Fast-Charge	V_{VBAT}>PTV, not Temp-Fault.
Fast-Charge	Top-Off	V_{VBAT}=BRV and not (Total Charge Time-Out)
Top-Off	Sleep	ICHG=IEOC and not (Charge Time-Out)
Sleep	Pre-condition	V_{VBAT}<PTV

Note: The PTV stands for pre-condition threshold voltage, the BRV stands for battery regulation voltage, the ICHG stands for charge path current and the IEOC stands for end of charge current.

Top-Off State

In the Top-Off state, the cell is charged in constant voltage mode where the V_{VBAT} is regulated at battery regulation voltage, which equals to the charge termination voltage specified in battery specification. The charge current goes less and less from the fast charge current as the charging is on and on, against the chemical and physical composition changes in the cell. Once the charge current goes less than the end of charge current threshold, the state machine jumps into Sleep State while the cell is recognized as full charged, the state is also the state of Sleep.

Sleep State

In the Sleep State, the charger represents as high-impedance to the cell and is with only the leakage current. The V_{VBAT} is actively monitored by the state machine all the time. When V_{VBAT} drop of typical 200mV being seen, the state machine begins a new charge cycle.

Time-Fault State

If the function is enabled, the pre-condition charge time are counted. When the pre-condition time-out happens, the state machine jumps into Time-Fault State. The Time-Fault State could only exit into End -of-Charge State when V_{VBAT} ever goes to less than the pre-condition threshold voltage or BATID ever reads invalid, which is presumably a battery replacement. Charge input power recycle does not reset the Time-Fault State.

Temp-Fault

When this function is enabled, the battery temperature is monitored whenever a suitable power applies on CHGIN. When battery is too cold or too hot, the state machine jumps into Sleep State for the temp-fault. In this state, the charger represents as high impedance to the cell, the charger circuitry remains functional waiting for the battery thermal condition changes.

Charge State Output

nSTAT Output

The nSTAT is an open-drain output for simple charge status output. It has an internal 8mA current limit and is capable to drive an LED for visual indication without the need of current limit resistor or other external circuitry doing the current limit. The nSTAT sinks current in precondition state, fast-charge state and top-off state. It turns into high impedance in sleep state and time-fault state.

CHG_STAT0[ ] and CHG_STAT1[ ] registers indicate 4 different charge states, which are the Off state (the force suspend state, the Time-Fault state, the Temp-Fault state or the LDO mode), the Sleep state, the Fast-Charge state or Top-Off state and the Pre-condition state. Those bits can be read through the I^2C interface.

Charge Oriented Interrupts

When the configuration enables to assert interrupt, the state change in the charger asserts interrupt to call service from the host system. The interrupt configuration is flexible to select which state and what kind of state change for interrupt assertion. Each interrupt has 2 bits to allow interrupt, one bit of the latest status of the respective state by the time of reading and a bit to specify which kind of change for asserting interrupt.

It is factory-option to have the Temp-Fault state or the BATID state to use the same set of 3 bits for configuring and flag. When Temp-Fault option is selected, which enables the battery thermal condition, the BATID state is not cared for interrupting. When the BATID is selected, the battery thermal condition is disabled, then the BATID state uses the set of the 3 bits. Refer to the *INTERRUPT DESCRIPTION* table for more details. Reading the CHGSTAT byte to clear the asserted interrupt.

Safe Charge and Operation

It is important to a system running on high energy battery that it only charges and operates on a qualified cell, and the behavior is within an predictable safe situation. The ACT5880 has following features available for system design selection.

Resistive Battery Identification

The ACT5880 has 3 auxiliary ADC inputs. The auxiliary input could be used to read voltage when forcing a current through the designed identification resistor in the battery pack.

Charge Safety Timer

The ACT5880 has 2 configurable time-out timers to count the elapsed time during precondition and the overall elapsed time during charge.

When this function is enabled, if the cell could not be charged to correct state in predicted maximum time, the charger stops charging and restarts only when the battery is replaced presumably.

Both time-out periods are programmable, refer to the *REGISTER MAP AND DESCRIPTIONS* section for more details.

Battery Thermal Condition

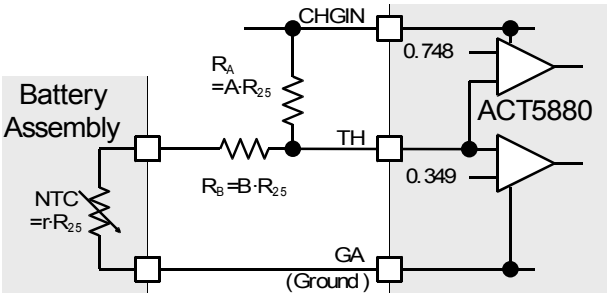
The battery thermal condition is a feature option against ordering. If this feature is optioned, the battery temperature is monitored and the charging is allowed only when the battery voltage is within a specified temperature window for the safe of battery and the equipment normal operation.

Precise window comparators are used for battery thermal condition, see the Figure 18 for circuit diagram. The window thresholds are trimmed to 2 precise ratios, and the external sense string is forced with the same force voltage used for comparators, the V_{CHGIN}. The 2 resistors, R_A and

R_B, are used to condition the string to have the desired ratios at the wanted hot threshold temperature and cold threshold temperature.

Figure 18:

The Battery Thermal Condition Circuit.



The normal temperature range cells typically work in -20°C to 40°C while the extended range is -20°C to 60°C. Giving the a NTC thermistor with 25°C characteristic resistance of R_{25}, the resistance ratio at hot threshold temperature is r_H and at cold threshold temperature is r_C, the proportion factor A and B for having the 2 precise ratios 0.748 and 0.349 are found as:

$A=0.411\cdot(r_C-r_H)$

$B=0.220\cdot r_C-1.22\cdot r_H$

It is necessary to verify how much power is desired to bias the selected NTC thermister, to assure no excessive self heating generated.

The resistance ratio r is the ratio of the resistance at a temperature to the resistance at 25°C. This ratio is found from the NTC specification in a table or a curve plot.

Reverse Block

The ACT5880 has a reverse block circuit in the charge path. Whenever the V_{CHGIN} is less than V_{VBAT}, as low as to 0V, the reverse block circuit prevents the reverse leakage from VBAT to CHGIN and the state machine jumps into Sleep State. This reverse block circuit does not work in LDO mode operation.

Input Over Voltage

The CHGIN allows applying continuous 12V and momentary 14V on it. When the voltage applied on CHGIN is greater than the over voltage threshold, the state machine jumps into Sleep State and charging stops.

As in the real application circuitry often has other connection to the CHGIN, such as the VBUS of USB circuit, the pull-up of charge state LED, the pull-up for BATID input, the pull-up for ACIN input and the pull-up for TH input. It may not be allowed to apply higher voltage on the CHGIN considering those other connections.

Typical Application Consideration

The charger circuit is well compensated, can be used to charge various capacities cells without modifying the input and output decoupling caps, which is 6.8μF~22μF for the input and 4.7μ~10μF for the output.

Autonomic and Slave Charge

The charge state machine in the ACT5880 is a complete autonomy. It senses the condition parameters, manages charge profile and indicates charge status without any foreign involvement.

The charger wakes up the host system, and calls for host system involvement if it is configured so. With this mechanism, the ACT5880 could work as a slave charger with host system involvement on demand.

Li+ Poly Cell and Li+ Cell Charge

The scheme and the default setting are optimized for single cell Li+ poly charging. Li+ poly cells with 4.2V charge termination voltage, which are the most common battery types in phone designs.

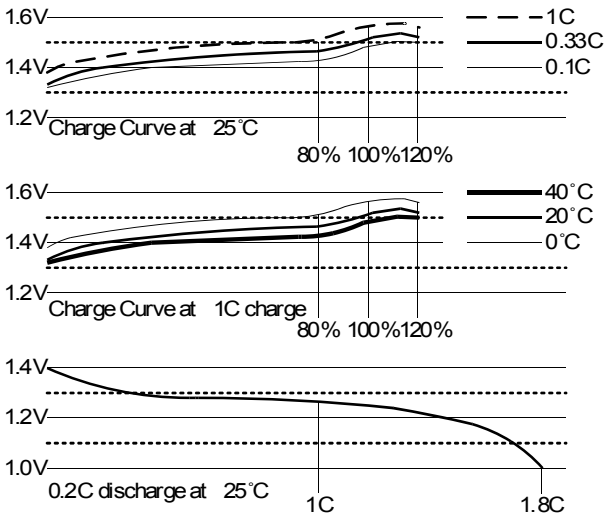
In case of using 18650 cylindrical cell, which is typically with 4.1V charge termination voltage (the termination voltage is anode material dependent, is specified for a battery model), applying 4.2V on it does not cause instant damage. It is possible to start with 4.2V battery regulation voltage and then program it to 4.1V later, but this is not rational for safe charging. Contact factory for ordering parts with 4.1V default.

NiMH cells charge

Though the charge scheme is not optimized for charging NiMH cells, its current limit and voltage limit, auto-restart features make the ACT5880 charger a practically applicable charger in fix wireless terminal applications for 3 NiMH cells charging with its 4.2V to 4.4V battery regulation voltages. In this kind of applications, the cells are floating charged at 1.4V to 1.47V per cell, which is in the good range for floating and uses the most part of the battery capability. Figure 19 shows the typical curves for NiMH battery.

Figure 19:

The Charge and Discharge Curves for NiMH Cell.



Long Cord Power Operation

When a device whose normal operation is with a power cord connected, the charger may frequently seesaw charges the battery. Programming the fast charge current to a smaller volume could have the end of charge current less than the operation current and then the end of charge condition does not happen, forces the charger into floating. The floating state causes less aging than the frequent seesaw charge does. For staying in floating, the total charge time-out function should be disabled and the battery regulation should be programmed to 100mV lower than the nominal battery charge termination voltage, which is desired for safe floating and enlarges the battery life cycles.

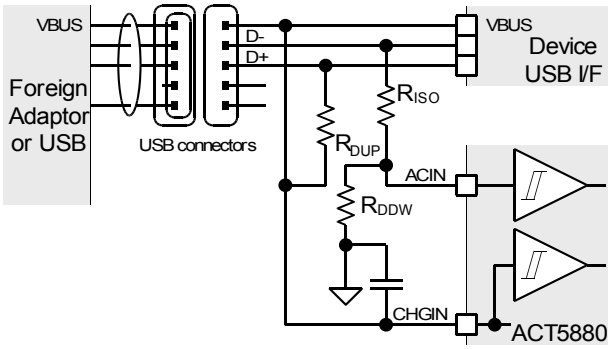
USB Charging

The ACT5880 provides the adaptor charge input detection, the battery installed detection, the CHGLEV charge current set input and with few programmable registers for the USB charging. 3 situations in battery powered devices specified in the "Battery Charging" specification of the USB IF are supported, the no-battery situation, the weak/dead battery situation and the battery normal situation. Specified device behavior in those situations is required only if the power source is identified as a host charger or a hub charger.

The ACT5880 deploys the resistive method recommended by the USB IF for the power source identification, with its precise threshold ACIN input. Ref to the Figure 20, a sample circuit uses single port for both USB connection and charging, in which the R_{DUP} is 220kΩ, the R_{ISO} is 240kΩ and the R_{DDW} is 220kΩ. The input of an adaptor in compliance with the "Battery Charging" and the "YD/T1591" specifications is identified if both the CHGIN and the ACIN are read valid. Only the CHGIN read valid is for USB host attached or for hub attached, while only the ACIN read valid is for USB OTG A-device attached or for an over-loaded weak adaptor attached. The resistive detection provides reliable detection in most cases but the case of a USB OTG A-device powering the VBUS with its local 5V, which is a known operation state of the device. The R_{DUP} and the R_{ISO} should be placed close to the traces connecting the USB receptacle pins and USB PHY pins, for less branching effect, which is important to running high speed transmission.

Figure 20:

The Sample Circuit for USB Charging.



When a suitable voltage power applied on the CHGIN, and while charging function allowed (SUSCHG=0), if no battery detected, the charger path turns into the LDO mode, in which it regulates the VBAT voltage to power the system. The system defines its way of operation in no-battery situation, either as a no-battery USB device or turns its self into device suspend mode with less than 2.5mA drawn from USB port. In the LDO mode, the output voltage is set by the VSET[ ], the pass current is limited to the fast charge current set as a function of the ISET[ ] and the CHGLEV, and the charge timers are cleared. The thermal regulation keeps preventing the die from overheating.

When a USB or a hub is attached while the device is with a weak/dead battery from the device system point of view, while the charging function is default enabled (SUSCHG=0), the ACT5880 starts charging with the fast charge set by the CHGLEV or precondition charges the battery, dependent on if the battery voltage is greater or less than the precondition threshold. The CHGLEV should be connected to an I/O of the host system with a pull-down resistor around 1MΩ. Before the processor

could start normal operation and possibly changes the I/O output, the ACT5880 preconditions and then charges battery with only 90mA current limit, as specified in the "Battery Charging", until the battery is charged to high enough voltage for device system to start.

If USB attaching is identified in a battery normal system, the device system should start and try to connect the host within 100ms, as required by the USB protocol. Within this 100ms, 100mA drawn from the port is allowed, what is greater than the 90mA the ACT5880 takes. After the connection , the device system takes control of charging, either charging as a standard load to USB port or pouring larger current as allowed, or turning into USB SUSPEND without charging.

Fast Charge Current Adaptive

The over load to the USB port or a weak adaptor could be identified by the loss of reading CHGIN valid while the ACIN keeps reading valid. If the over load happens, the device system could program the ACT5880 to a less fast charge current volume to make the power source normal while still getting as much as possible power.

Dual inputs and USB-OTG Paths

In applications that 2 power input receptacles wanted, 2 low forward voltage diodes and a 240kΩ resistor R_{DAD} are used in addition to circuit in Figure 20, as showed in Figure 21. When no suitable input attaches to the Adaptor In, the circuit works similarly to the circuit in the Figure 20. When suitable input attaches to the Adaptor In, both ACIN and CHGIN are read valid, regardless what attaches to the USB receptacle.

Figure 21:

The Sample Circuit for Dual-inputs Charging.

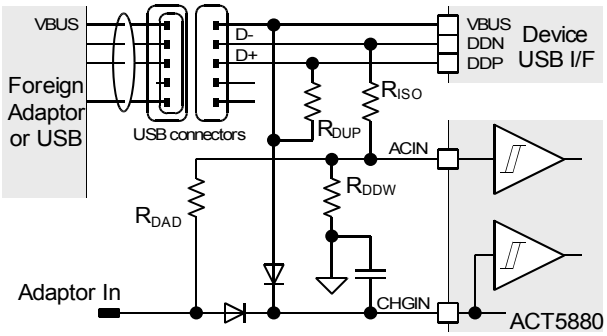


Figure 22 is the typical circuit connecting a 5V internal rail to the VBUS for providing power for OTG application. In this circuit the Q_{OTG} has to be with V_{GTH} greater than 2V and to be effectively conductive when V_{GTH} is 5V. The Q_{OTG} is used to isolate the capacitance on 5V rail during the VBUS pulsing required by the SRP, and also provides a controlled path for using the external 5V from VBUS to replace the internal 5V rail.

Figure 22:

The Sample Circuit for Using External 5V rail.

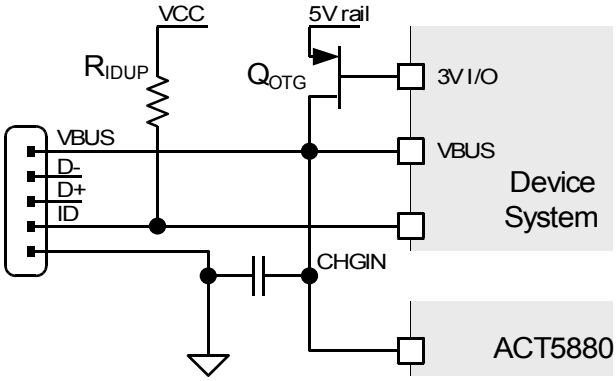


Figure 23:

The Sample Circuit of Dual-inputs and External 5V.

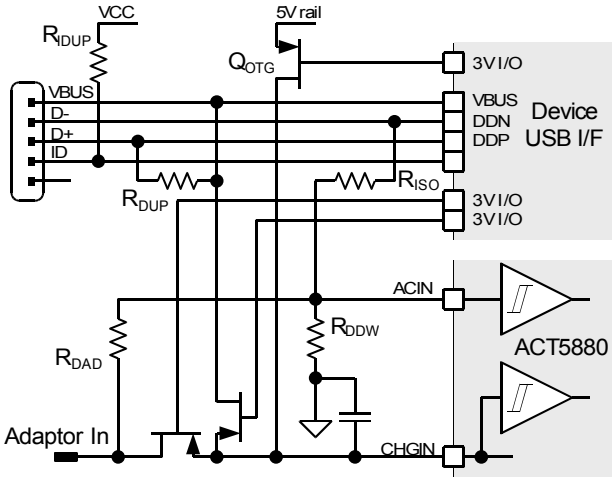


Figure 23 is a sample of providing high current 5V from an adaptor to the VBUS and for replacing the internal 5V rail. All the 3 PFETs should be good for control with 3V I/O, level shifters are desired otherwise.

THERMAL ANALYSIS

The package thermal dissipation is not designed to handle the total heating generated by run every circuit at its maximum rating, which is an over-killed situation for true applications. The sum of nominal LDO maximum current is 2.18A and the total DC/DC input equivalent current is 0.95A to 1.06A for battery voltage 3.6V to 4.2V, which are 2.4W to 3.3W power dissipation respectively in the ACT5880. Those numbers are greater than the maximum power dissipation for the ACT5880 in FC FBGA package, what is around 2W at 25°C.

Typical Operation Condition

The worst case thermal budget analysis against the typical application is necessary. A sample case is simultaneous video capture and transmission operation condition. Table 12 is a reference for thermal budget analysis with experience data.

Users should use their own data to replace those in this table for their designs.

Table 12:

The Thermal Condition Analysis.

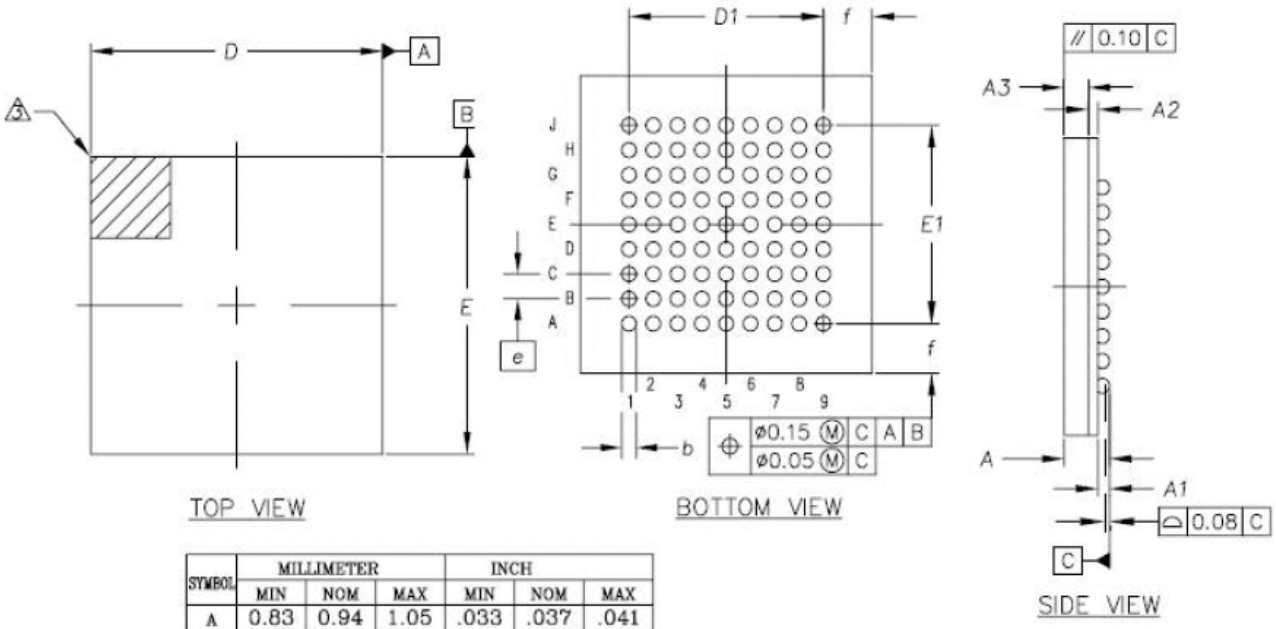
CHANNEL	VOLTAGE (V)	CURRENT (mA)	BUDGET	LOAD BLOCK
OUT1 DC/DC	1.2	Out:600 In:190	0.07	COREs
OUT2 DC/DC	1.8	Out:350 In:165	0.07	Memory
OUT3 DC/DC	5	Out:300 In:390	0.13	4.3'' Backlight and OTG
OUT4	2.85	150	0.2	RF TxRx
OUT5	2.85	150	0.2	RF digital
OUT6	2.85	50	0.07	TCXO
OUT7	3	200	0.24	I/O, ROMs
OUT8	2.5	150	0.26	I/O, Memory
OUT9	1.2	50	0.15	PLL
OUT10	3.3	50	0.04	CODEC
OUT11	1.8	25	0.06	SIM
OUT12	1.8	150	0.36	Camera digital
OUT13	2.8	80	0.11	Camera analog
3 OD drivers		0	0	LED
Total		1800	1.96	

Thermal Budget Allocation during Charging

Reference to the total current in Table 12, what is over the possible maximum charge current of the ACT5880. This implies that in worst case there is no current from adaptor is allocated for charge. Eventually, the die temperature regulation to charge current would allocate the thermal budget to other circuits, to the circuit desired for system operation firstly.

PACKAGE OUTLINE AND DIMENSIONS

81 Balls FC FBGA; Pitch: 0.5mm; Ball: 0.3mm.



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.83	0.94	1.05	.033	.037	.041
A1	0.20	0.24	0.28	.008	.009	.011
A2	0.16	0.20	0.24	.006	.008	.009
A3	0.47	0.50	0.53	.019	.020	.021
b	0.25	0.30	0.35	.010	.012	.014
D	5.90	6.00	6.10	.232	.236	.240
D1	4.00 BSC			.157 BSC		
E	5.90	6.00	6.10	.232	.236	.240
E1	4.00 BSC			.157 BSC		
e	0.50 BSC			.020 BSC		
f	0.90	1.00	1.10	.035	.039	.043

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