National Semiconductor

# 74VHC4040
# 12-Stage Binary Counter

## General Description

The VHC4040 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC4040 is a 12-stage counter which increments on the negative edge of the input clock and all outputs are reset to a low level by applying a logical high on the reset input. An input protection circuit insures that 0V to 7V can be applied to the inputs without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

## Features

- High speed
- Low power dissipation: $I_{CC}$ = 4 μA (max) at $T_A$ = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range: $V_{CC}$ (opr) = 2V ~ 5.5V
- Low noise: $V_{OLP}$ = 0.8V (max)
- Pin and function compatible with 74HC4040

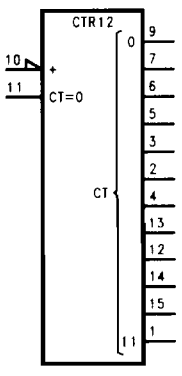
## Ordering Code: See Section 6

| Commercial | Package Number | Package Description |
|---|---|---|
| 74VHC4040M | M16A | 16-Lead Molded JEDEC SOIC |
| 74VHC4040N | N16E | 16-Lead Molded DIP |

**Note:** Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter 'X' to the ordering code.

## Logic Symbols

IEEE/IEC

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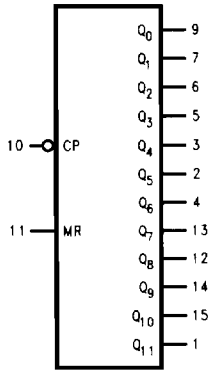


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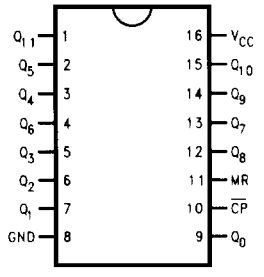
## Connection Diagram

Pin Assignment for SOIC and PDIP

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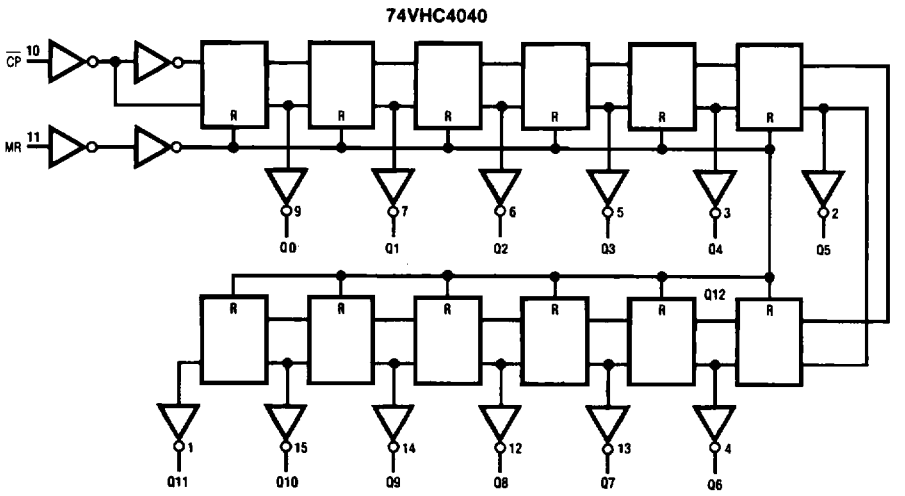
| Pin Names | Description |
|---|---|
| $Q_0$–$Q_{11}$ | Flip-Flop Outputs |
| $\overline{CP}$ | Negative Edged Triggered Clock |
| MR | Master Reset |

## Logic Diagram

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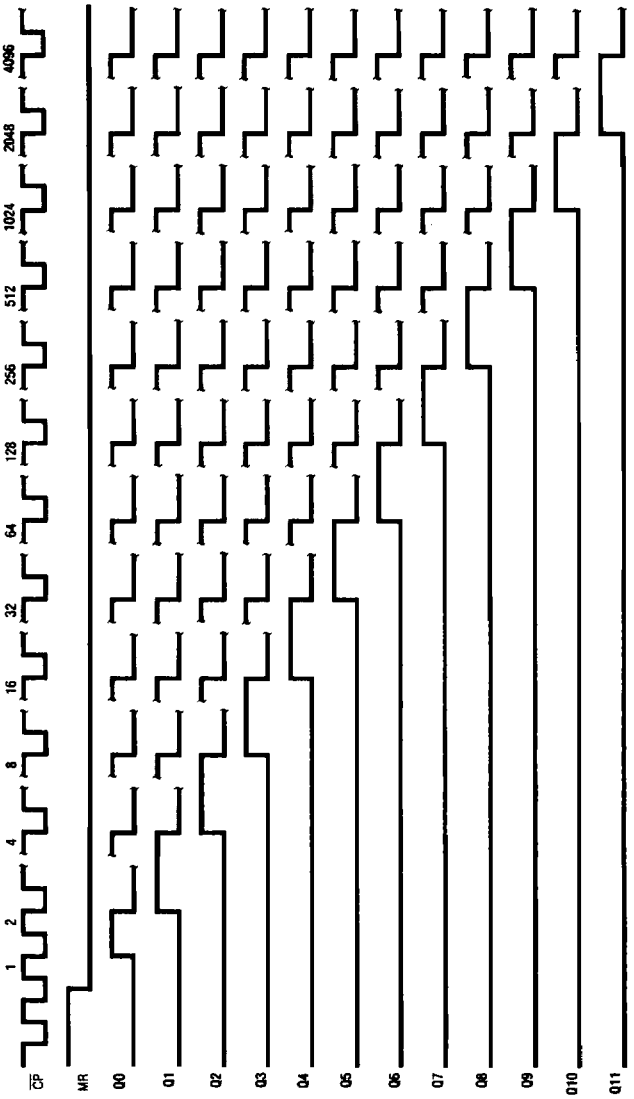
## Timing Diagram

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## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Voltage ($V_{IN}$) | −0.5V to +7.0V |
| DC Output Voltage ($V_{OUT}$) | −0.5V to $V_{CC}$ + 0.5V |
| Input Diode Current ($I_{IK}$) | −20 mA |
| Output Diode Current ($I_{OK}$) | ±20 mA |
| DC Output Current ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$/GND Current ($I_{CC}$) | ±75 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Lead Temperature ($T_L$) (Soldering, 10 seconds) | 260°C |

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 2.0V to +5.5V |
| Input Voltage ($V_{IN}$) | 0V to +5.5V |
| Output Voltage ($V_{OUT}$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_{OPR}$) | −40°C to +85°C |
| Input Rise and Fall Time ($t_r$, $t_f$) | |
| $V_{CC}$ = 3.3V ±0.3V | 0 ~ 100 ns/V |
| $V_{CC}$ = 5.0V ±0.5V | 0 ~ 20 ns/V |

## DC Characteristics for 'VHC Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 74VHC $T_A$ = 25°C Min | Typ | Max | 74VHC $T_A$ = −40°C to +85°C Min | Max | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | 2.0 | 1.50 | | | 1.50 | | V | | |
| | | 3.0–5.5 | 0.7 $V_{CC}$ | | | 0.7 $V_{CC}$ | | | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | 0.50 | | 0.50 | V | | |
| | | 3.0–5.5 | | | 0.3 $V_{CC}$ | | 0.3 $V_{CC}$ | | | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | | | |
| | | 3.0 | 2.58 | | | 2.48 | | V | | $I_{OH}$ = −4 mA |
| | | 4.5 | 3.94 | | | 3.80 | | | | $I_{OH}$ = −8 mA |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 4.5 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 3.0 | | | 0.36 | | 0.44 | V | | $I_{OL}$ = 4 mA |
| | | 4.5 | | | 0.36 | | 0.44 | | | $I_{OL}$ = 8 mA |
| $I_{IN}$ | Input Leakage Current | 0–5.5 | | | ±0.1 | | ±1.0 | μA | $V_{IN}$ = 5.5V or GND | |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | | | 4.0 | | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND | |

## AC Electrical Characteristics for 'VHC Family Devices: See Section 2 for Waveforms

| Symbol | Parameter | $V_{CC}$ (V) | 74VHC $T_A = +25°C$ Min | Typ | Max | 74VHC $T_A = -40°C$ to $+85°C$ Min | Max | Units | Conditions | | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time to $Q_1$ | 3.3 ±0.3 | | 7.5 | 11.9 | 1.0 | 14.0 | ns | | $C_L$ = 15 pF | 2-6 |
| | | | | 10.0 | 15.4 | 1.0 | 17.5 | | | $C_L$ = 50 pF | 2-6 |
| | | 5.0 ±0.5 | | 4.8 | 7.3 | 1.0 | 8.5 | ns | | $C_L$ = 15 pF | 2-6 |
| | | | | 6.3 | 9.3 | 1.0 | 10.5 | | | $C_L$ = 50 pF | 2-6 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time between Stages from $Q_n$ to $Q_{n+1}$ | 3.3 ±0.3 | | | | | | ns | | $C_L$ = 15 pF | 2-5, 6 |
| | | | | 2.4 | 4.4 | 1.0 | 5.0 | | | $C_L$ = 50 pF | 2-5, 6 |
| | | 5.0 ±0.5 | | | | | | ns | | $C_L$ = 15 pF | 2-5, 6 |
| | | | | 1.6 | 3.1 | 1.0 | 3.5 | | | $C_L$ = 50 pF | 2-5, 6 |
| $t_{PHL}$ | Propagation Delay Time MR−$Q_n$ | 3.3 ±0.3 | | 8.3 | 12.8 | 1.0 | 15.0 | ns | | $C_L$ = 15 pF | 2-6 |
| | | | | 10.8 | 16.3 | 1.0 | 18.5 | | | $C_L$ = 50 pF | 2-6 |
| | | 5.0 ±0.5 | | 5.6 | 8.6 | 1.0 | 10.0 | ns | | $C_L$ = 15 pF | 2-6 |
| | | | | 7.1 | 10.6 | 1.0 | 12.0 | | | $C_L$ = 50 pF | 2-6 |
| $f_{MAX}$ | Maximum Clock Frequency | 3.3 ±0.3 | 90 | 140 | | 75 | | MHz | | $C_L$ = 15 pF | |
| | | | 55 | 80 | | 50 | | | | $C_L$ = 50 pF | |
| | | 5.0 ±0.5 | 150 | 210 | | 125 | | MHz | | $C_L$ = 15 pF | |
| | | | 95 | 125 | | 80 | | | | $C_L$ = 50 pF | |
| $C_{IN}$ | Input Capacitance | | | 4 | 10 | | 10 | pF | $V_{CC}$ = Open | | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 21 | | | | pF | (Note 1) | | |

**Note 1:** $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC}$ (opr) = $C_{PD} * V_{CC} * f_N + I_{CC}$.

## AC Operating Requirements for 'VHC Family Devices: See Section 2 for Waveforms

| Symbol | Parameter | $V_{CC}$ (V) | 74VHC $T_A = 25°C$ Typ | Guaranteed Minimum | 74VHC $T_A = -40°C$ to $+85°C$ | Units | Conditions | Fig. No. |
|---|---|---|---|---|---|---|---|---|
| $t_{w(L)}$ $t_{w(H)}$ | Minimum Pulse Width (CP) | 3.3 ±0.3 | | 5.0 | 5.0 | ns | | 2-6 |
| | | 5.0 ±0.5 | | 5.0 | 5.0 | | | |
| $t_{w(L)}$ | Minimum Pulse Width (MR) | 3.3 ±0.3 | | 5.0 | 5.0 | ns | | 2-6 |
| | | 5.0 ±0.5 | | 5.0 | 5.0 | | | |
| $t_{rem}$ | Minimum Removal Time (MR) | 3.3 ±0.3 | | 5.0 | 5.0 | ns | | 2-6, 9 |
| | | 5.0 ±0.5 | | 5.0 | 5.0 | | | |