

## FEATURES

- Ultrasmall package:** 2 mm × 2 mm, 8-lead LFCSP
- High relative accuracy (INL):** ±2 LSB maximum at 16 bits
- Low drift, 2.5 V reference:** 2 ppm/°C typical
- Selectable span output:** 2.5 V or 5 V
- Total unadjusted error (TUE):** ±0.06% of FSR maximum
  - Offset error:** ±1.5 mV maximum
  - Gain error:** ±0.05 % of FSR maximum
- Low glitch:** 0.1 nV-sec
- High drive capability:** 20 mA
- Low power:** 1.2 mW at 3.3 V
- Independent logic supply:** 1.8 V to 5.5 V
- Wide operating temperature range:** -40°C to +105°C
- Robust 4 kV HBM ESD protection**

## APPLICATIONS

- Process controls
- Data acquisition systems
- Digital gain and offset adjustment
- Programmable voltage sources
- Optical modules

## GENERAL DESCRIPTION

The [AD5693R/AD5692R/AD5691R](#), members of the *nanoDAC+*® family, are low power, single-channel, 16-/14-/12-bit buffered voltage output DACs. The devices include an enabled by default internal 2.5 V reference, offering 2 ppm/°C drift. The output span can be programmed to be 0 V to  $V_{REF}$  or 0 V to  $2 \times V_{REF}$ . All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The devices are available in a 2.00 mm × 2.00 mm, 8-lead LFCSP or a 10-lead MSOP.

The internal power-on reset circuit ensures that the DAC register is written to zero scale at power-up while the internal output buffer is configured in normal mode. The [AD5693R/AD5692R/AD5691R](#) contain a power-down mode that reduces the current consumption of the device to 2 μA (maximum) at 5 V and provides software selectable output loads.

The [AD5693R/AD5692R/AD5691R](#) use an I<sup>2</sup>C interface. Some device options also include an asynchronous  $\overline{\text{RESET}}$  pin and a  $V_{LOGIC}$  pin, allowing 1.8 V compatibility.

## FUNCTIONAL BLOCK DIAGRAM

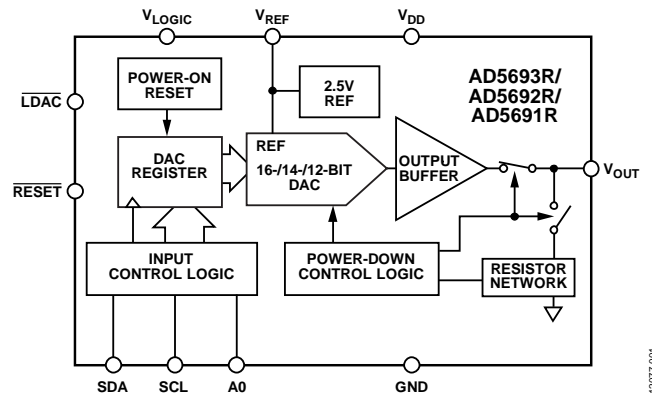


Figure 1. MSOP

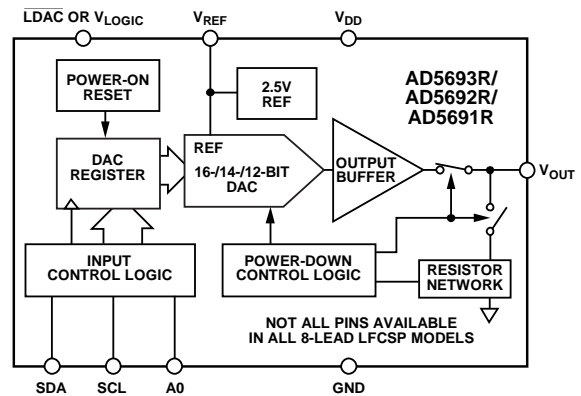


Figure 2. LFCSP

**Table 1. Related Devices**

Interface	Reference	16-Bit	14-Bit	12-Bit
SPI	Internal	<a href="#">AD5693R</a>	<a href="#">AD5692R</a>	<a href="#">AD5691R</a>
	External			
I <sup>2</sup> C	Internal	<a href="#">AD5693R</a>	<a href="#">AD5692R</a>	<a href="#">AD5691R</a>
	External			

## PRODUCT HIGHLIGHTS

1. High relative accuracy (INL): ±2 LSB maximum ([AD5693R](#), 16-bit).
2. Low drift, 2.5 V on-chip reference: 2 ppm/°C typical and 5 ppm/°C maximum temperature coefficient.
3. 2 mm × 2 mm, 8-lead LFCSP and 10-lead MSOP.

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## REVISION HISTORY

2/14—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  to GND,  $C_L = 200\text{ pF}$  to GND,  $V_{REF} = 2.5\text{ V to }V_{DD} - 0.2\text{ V}$ ,  $V_{LOGIC} = 1.8\text{ V to }5.5\text{ V}$ ,  $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE <sup>1</sup>					
AD5693R					
Resolution	16			Bits	
Relative Accuracy (INL)					
A Grade			$\pm 8$	LSB	Gain = 2
B Grade			$\pm 2$	LSB	Gain = 1
Differential Nonlinearity			$\pm 3$	LSB	Guaranteed monotonic by design
			$\pm 1$	LSB	
AD5692R					
Resolution	14			Bits	
Relative Accuracy			$\pm 4$	LSB	
Differential Nonlinearity			$\pm 1$	LSB	Guaranteed monotonic by design
AD5691R					
Resolution	12			Bits	
Relative Accuracy					
A Grade			$\pm 2$	LSB	
B Grade			$\pm 1$	LSB	
Differential Nonlinearity			$\pm 1$	LSB	Guaranteed monotonic by design
Zero Code Error			1.25	mV	All 0s loaded to DAC register
Offset Error			$\pm 1.5$	mV	
Full-Scale Error			$\pm 0.075$	% of FSR	All 1s loaded to DAC register
Gain Error			$\pm 0.05$	% of FSR	
Total Unadjusted Error			$\pm 0.16$	% of FSR	Internal reference, gain = 1
			$\pm 0.14$	% of FSR	Internal reference, gain = 2
			$\pm 0.075$	% of FSR	External reference, gain = 1
			$\pm 0.06$	% of FSR	External reference, gain = 2
Zero Code Error Drift		$\pm 1$		$\mu\text{V}/^\circ\text{C}$	
Offset Error Drift		$\pm 1$		$\mu\text{V}/^\circ\text{C}$	
Gain Temperature Coefficient		$\pm 1$		ppm/ $^\circ\text{C}$	
DC Power Supply Rejection Ratio		0.2		mV/V	DAC code = midscale, $V_{DD} = 5\text{ V} \pm 10\%$
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		$V_{REF}$	V	Gain = 0
	0		$2 \times V_{REF}$	V	Gain = 1
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	$R_L = 2\text{ k}\Omega$
Resistive Load	1			k $\Omega$	$C_L = 0\text{ }\mu\text{F}$
Load Regulation		10		$\mu\text{V}/\text{mA}$	$V_{DD} = 5\text{ V}$ , DAC code = midscale, $-30\text{ mA} \leq I_{OUT} \leq +30\text{ mA}$
		10		$\mu\text{V}/\text{mA}$	$V_{DD} = 3\text{ V}$ , DAC code = midscale, $-20\text{ mA} \leq I_{OUT} \leq +20\text{ mA}$
Short-Circuit Current	20		50	mA	
Load Impedance at Rails <sup>2</sup>		20		$\Omega$	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>REFERENCE OUTPUT</b>					
Output Voltage	2.4975		2.5025	V	At ambient temperature
Voltage Reference TC <sup>3</sup>					See the Terminology section
A Grade		5	20	ppm/°C	
B Grade		2	5	ppm/°C	
Output Impedance		0.05		Ω	
Output Voltage Noise		16.5		μV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient temperature, f = 10 kHz, C <sub>L</sub> = 10 nF
Capacitive Load Stability		5		μF	R <sub>L</sub> = 2 kΩ
Load Regulation Sourcing		50		μV/mA	At ambient temperature, V <sub>DD</sub> ≥ 3 V
Load Regulation Sinking		30		μV/mA	At ambient temperature
Output Current Load Capability		±5		mA	V <sub>DD</sub> ≥ 3 V
Line Regulation		80		μV/V	At ambient temperature
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
<b>REFERENCE INPUT</b>					
Reference Current		35		μA	V <sub>REF</sub> = V <sub>DD</sub> = V <sub>LOGIC</sub> = 5.5 V, gain = 1
		57		μA	V <sub>REF</sub> = V <sub>DD</sub> = V <sub>LOGIC</sub> = 5.5 V, gain = 2
Reference Input Range <sup>4</sup>			V <sub>DD</sub>	V	
Reference Input Impedance		120		kΩ	Gain = 1
		60		kΩ	Gain = 2
<b>LOGIC INPUTS</b>					
I <sub>IN</sub> , Input Current			±1	μA	Per pin
			±3	μA	SDA and SCL pins
V <sub>INL</sub> , Input Low Voltage <sup>4</sup>			0.3 × V <sub>DD</sub>	V	
V <sub>INH</sub> , Input High Voltage <sup>4</sup>	0.7 × V <sub>DD</sub>			V	
C <sub>IN</sub> , Pin Capacitance		2		pF	
<b>LOGIC OUTPUTS (SDA)<sup>4</sup></b>					
Output Low Voltage, V <sub>OL</sub>			0.4	V	I <sub>SINK</sub> = 200 μA
Output High Voltage, V <sub>OH</sub>	V <sub>DD</sub> - 0.4			V	I <sub>SOURCE</sub> = 200 μA
Pin Capacitance		4		pF	
<b>POWER REQUIREMENTS</b>					
V <sub>LOGIC</sub> <sup>5</sup>	1.8		5.5	V	
I <sub>LOGIC</sub> <sup>5</sup>		0.25	3	μA	V <sub>IH</sub> = V <sub>LOGIC</sub> or V <sub>IL</sub> = GND
V <sub>DD</sub>	2.7		5.5	V	Gain = 1
	V <sub>REF</sub> + 1.5		5.5	V	Gain = 2
I <sub>DD</sub> <sup>6</sup>					V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND
Normal Mode <sup>7</sup>		350	500	μA	Internal reference enabled
		110	180	μA	Internal reference disabled
Power-Down Modes <sup>8</sup>			2	μA	

<sup>1</sup> Linearity calculated using a reduced code range: AD5693R (Code 512 to Code 65,535); AD5692R (Code 128 to Code 16,384); AD5691R (Code 32 to Code 4096). Output unloaded.

<sup>2</sup> When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 20 Ω typical channel resistance of the output devices; for example, when sinking 1 mA, the minimum output voltage with 20 Ω, 1 mA generates 20 mV. See Figure 35 for more details.

<sup>3</sup> Voltage reference temperature coefficient is calculated as per the box method. See the Terminology section for more information.

<sup>4</sup> Substitute V<sub>LOGIC</sub> for V<sub>DD</sub> if the device includes a V<sub>LOGIC</sub> pin.

<sup>5</sup> The V<sub>LOGIC</sub> pin is not available on all models.

<sup>6</sup> If the V<sub>LOGIC</sub> pin is not available, I<sub>DD</sub> = I<sub>DD</sub> + I<sub>LOGIC</sub>.

<sup>7</sup> Interface inactive. DAC active. DAC output unloaded.

<sup>8</sup> DAC powered down.

## AC CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  to GND,  $C_L = 200\text{ pF}$  to GND,  $V_{REF} = 2.5\text{ V to }V_{DD} - 0.2\text{ V}$ ,  $V_{LOGIC} = 1.8\text{ V to }5.5\text{ V}$ ,  $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , typical at  $25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time <sup>1,2</sup>	5	7	$\mu\text{s}$	Gain = 1
Slew Rate	0.7		$\text{V}/\mu\text{s}$	
Digital-to-Analog Glitch Impulse <sup>1</sup>	0.1		$\text{nV}\cdot\text{s}$	$\pm 1$ LSB change around major carry, gain = 2
Digital Feedthrough <sup>1</sup>	0.1		$\text{nV}\cdot\text{s}$	
Total Harmonic Distortion <sup>1</sup>	-80		dB	$V_{REF} = 2\text{ V} \pm 0.1\text{ V}$ p-p, frequency = 10 kHz
Output Noise Spectral Density <sup>1</sup>	300		$\text{nV}/\sqrt{\text{Hz}}$	DAC code = midscale, 10 kHz
Output Noise	6		$\mu\text{V}$ p-p	0.1 Hz to 10 Hz; internal reference
SNR	90		dB	At ambient temperature, bandwidth (BW) = 20 kHz, $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$
SFDR	83		dB	At ambient temperature, BW = 20 kHz, $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$
SINAD	80		dB	At ambient temperature, BW = 20 kHz, $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$

<sup>1</sup> See the Terminology section.

<sup>2</sup> For the AD5693R, to  $\pm 2$  LSB. For the AD5692R, to  $\pm 1$  LSB. For the AD5691R, to  $\pm 0.5$  LSB

## TIMING CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{LOGIC} = 1.8\text{ V to }5.5\text{ V}$ ,  $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter <sup>1</sup>	Min	Typ	Max	Unit	Description
$f_{SCL}$ <sup>2</sup>			400	kHz	Serial clock frequency
$t_1$	0.6			$\mu\text{s}$	SCL high time, $t_{HIGH}$
$t_2$	1.3			$\mu\text{s}$	SCL low time, $t_{LOW}$
$t_3$	100			ns	Data setup time, $t_{SU; DAT}$
$t_4$ <sup>3</sup>	0		0.9	$\mu\text{s}$	Data hold time, $t_{HD; DAT}$
$t_5$	0.6			$\mu\text{s}$	Setup time for a repeated start condition, $t_{SU; STA}$
$t_6$	0.6			$\mu\text{s}$	Hold time (repeated) start condition, $t_{HD; STA}$
$t_7$	1.3			$\mu\text{s}$	Bus free time between a stop and a start condition, $t_{BUF}$
$t_8$	0.6			$\mu\text{s}$	Setup time for a stop condition, $t_{SU; STO}$
$t_9$	20		300	ns	Rise time of SDA signal, $t_r$
$t_{10}$ <sup>4</sup>	$20 \times (V_{DD}/5.5\text{ V})$		300	ns	Fall time of SDA signal, $t_f$
$t_{11}$	20		300	ns	Rise time of SCL signal, $t_r$
$t_{12}$ <sup>4</sup>	$20 \times (V_{DD}/5.5\text{ V})$		300	ns	Fall time of SCL signal, $t_f$
$t_{SP}$ <sup>5</sup>	0		50	ns	Pulse width of suppressed spike (not shown in Figure 3)
$t_{13}$	400			ns	$\overline{\text{LDAC}}$ falling edge to SCL falling edge
$t_{14}$	400			ns	$\overline{\text{LDAC}}$ pulse width (synchronous mode)
$t_{15}$	20			ns	$\overline{\text{LDAC}}$ pulse width (asynchronous mode)
$t_{16}$	75			ns	$\overline{\text{RESET}}$ pulse width
$t_{REF\_POWER\_UP}$ <sup>6</sup>		600		$\mu\text{s}$	Reference power-up (not shown in Figure 3)
$t_{SHUTDOWN}$ <sup>7</sup>			6	$\mu\text{s}$	Exit shutdown (not shown in Figure 3)

<sup>1</sup> Maximum bus capacitance is limited to 400 pF. All input signals are specified with  $t_r = t_f = 1\text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

<sup>2</sup> The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate; however, it has a negative effect on the EMC behavior of the device.

<sup>3</sup> The master should add at least 300 ns for the SDA signal (with respect to the  $V_{OH}$  (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

<sup>4</sup> Substitute  $V_{LOGIC}$  for  $V_{DD}$  on devices that include a  $V_{LOGIC}$  pin.

<sup>5</sup> Not applicable for standard mode.

<sup>6</sup> Expect the same timing when powering up the device after  $V_{DD}$  is equal to 2.7 V.

<sup>7</sup> Time to exit power-down to normal mode of AD5693R/AD5692R/AD5691R operation.

Timing Diagrams

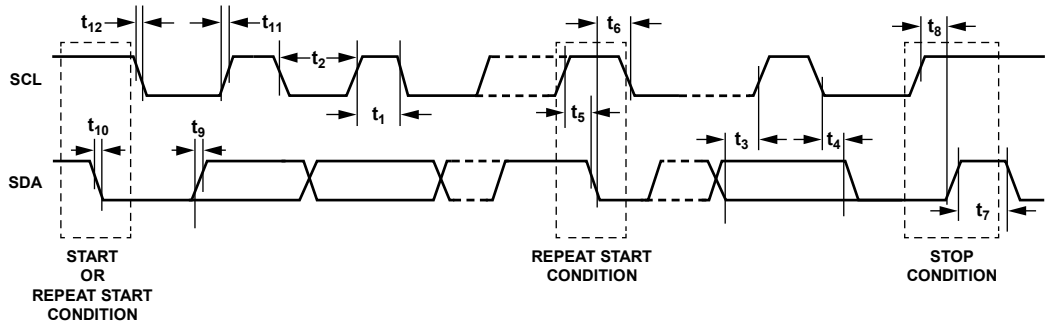


Figure 3. I<sup>2</sup>C Serial Interface Timing Diagram

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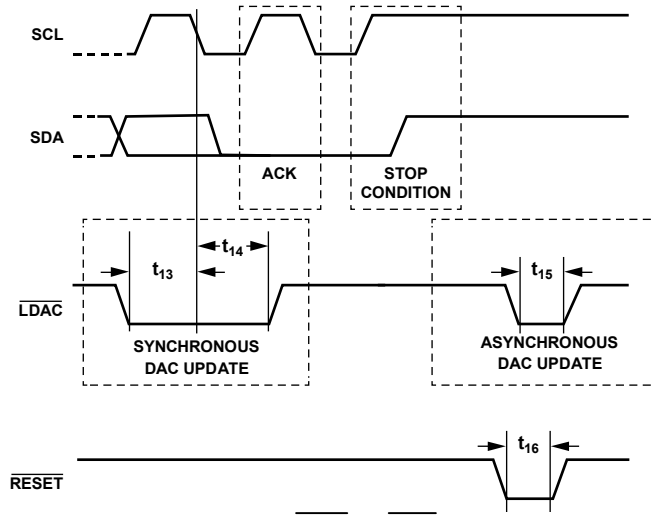


Figure 4. I<sup>2</sup>C  $\overline{\text{RESET}}$  and  $\overline{\text{LDAC}}$  Timing

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## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_{LOGIC}$ to GND	-0.3 V to +7 V
$V_{OUT}$ to GND	-0.3 V to $V_{DD} + 0.3$ V or +7 V (whichever is less)
$V_{REF}$ to GND	-0.3 V to $V_{DD} + 0.3$ V or +7 V (whichever is less)
Digital Input Voltage to GND <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or +7 V (whichever is less)
Operating Temperature Range Industrial	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_J$ max)	135°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
ESD <sup>2</sup>	4 kV
FICDM <sup>3</sup>	1.25 kV

<sup>1</sup> Substitute  $V_{DD}$  with  $V_{LOGIC}$  on devices that include a  $V_{LOGIC}$  pin.

<sup>2</sup> Human body model (HBM) classification.

<sup>3</sup> Field-Induced Charged-Device Model classification.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 6. Thermal Resistance<sup>1</sup>

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead LFCSP	90	25	°C/W
10-Lead MSOP	135	N/A	°C/W

<sup>1</sup> JEDEC 2S2P test board, still air (0 m/sec airflow).

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

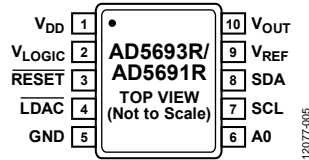


Figure 5. Pin Configuration, 10-Lead MSOP

Table 7. Pin Function Descriptions, 10-Lead MSOP

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V. Decouple the supply to GND.
2	V <sub>LOGIC</sub>	Digital Power Supply. Voltage ranges from 1.8 V to 5.5 V. Decouple the supply to GND.
3	RESET	Hardware Reset Pin. The RESET input is low level sensitive. When RESET is low, the device is reset and external pins are ignored. The input and DAC registers are loaded with zero code value and control register loaded with default values. Tie this pin to V <sub>LOGIC</sub> if not used.
4	LDAC	Load DAC. Transfers the content of the input register to the DAC register. It can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. This pin can be tied permanently low, and the DAC updates when new data is written to the input register.
5	GND	Ground Reference.
6	A0	Programmable Address for Multiple Package Decoding. The address pin can be updated on-the-fly.
7	SCL	Serial Clock Line.
8	SDA	Serial Data Input/Output.
9	V <sub>REF</sub>	Reference Input/Output. In the AD5693R/AD5691R, this is a reference output pin by default.
10	V <sub>OUT</sub>	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.



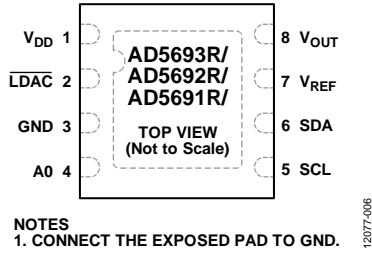


Figure 6. Pin Configuration, 8-Lead LFCSP, LDAC Option

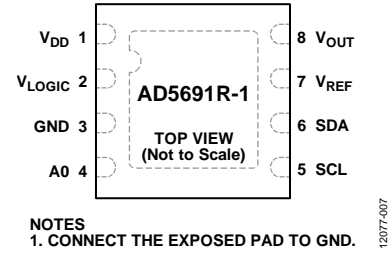


Figure 7. Pin Configuration, 8-Lead LFCSP, VLOGIC Option

Table 8. Pin Function Descriptions, 8-Lead LFCSP

Pin No.		Mnemonic	Description
LDAC	V <sub>LOGIC</sub>		
1	1	V <sub>DD</sub>	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V. Decouple the supply to GND.
2	N/A	$\overline{\text{LDAC}}$	Load DAC. Transfers the content of the input register to the DAC register. It can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. This pin can be tied permanently low and the DAC updates when new data is written to the input register.
N/A	2	V <sub>LOGIC</sub>	Digital Power Supply. Voltage ranges from 1.8 V to 5.5 V. Decouple the supply to GND.
3	3	GND	Ground Reference.
4	4	A0	Programmable Address for Multiple Package Decoding. The address pin can be updated on-the-fly.
5	5	SCL	Serial Clock Line.
6	6	SDA	Serial Data Input/Output.
7	7	V <sub>REF</sub>	Reference Input/Output. This is a reference output pin by default.
8	8	V <sub>OUT</sub>	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
		EPAD	Exposed Pad. Connect the exposed pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

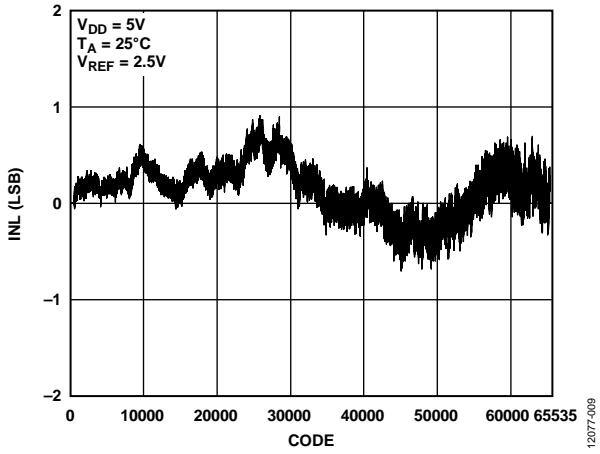


Figure 8. AD5693R INL

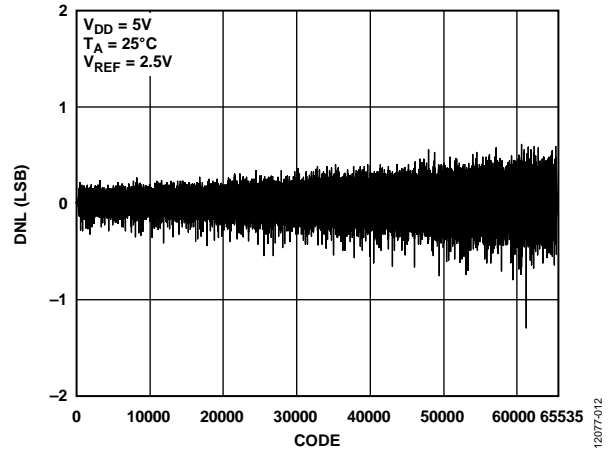


Figure 11. AD5693R DNL

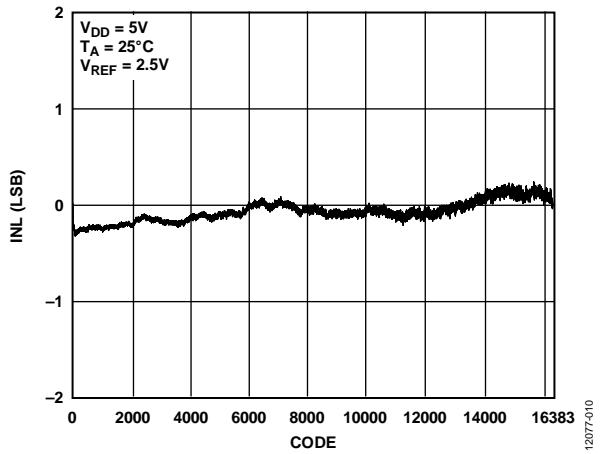


Figure 9. AD5692R INL

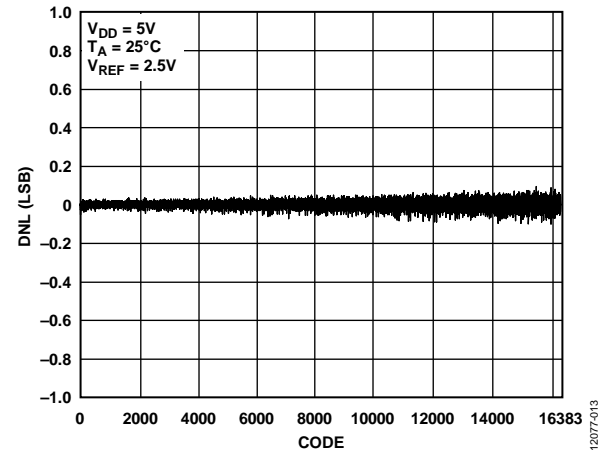


Figure 12. AD5692R DNL

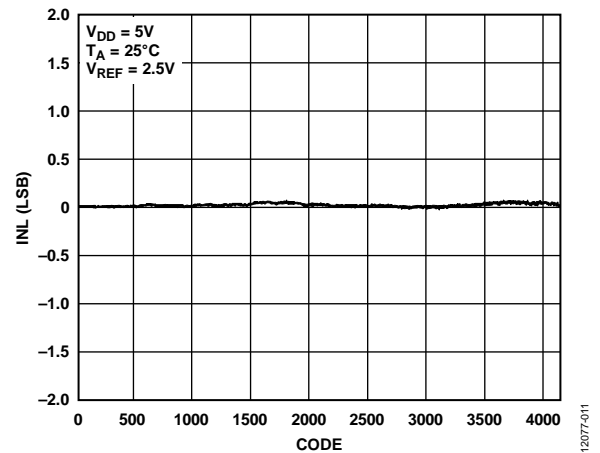


Figure 10. AD5691R INL

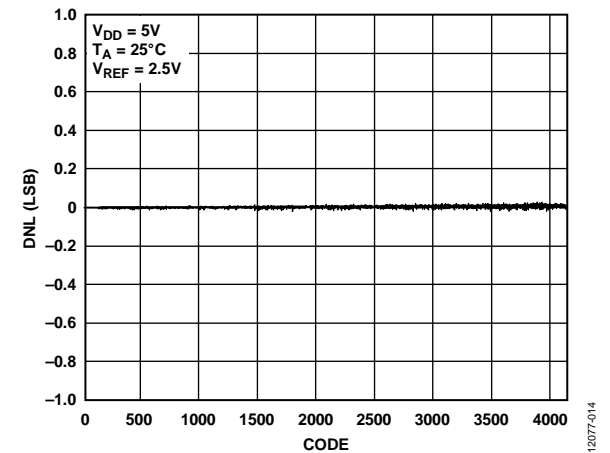


Figure 13. AD5691R DNL

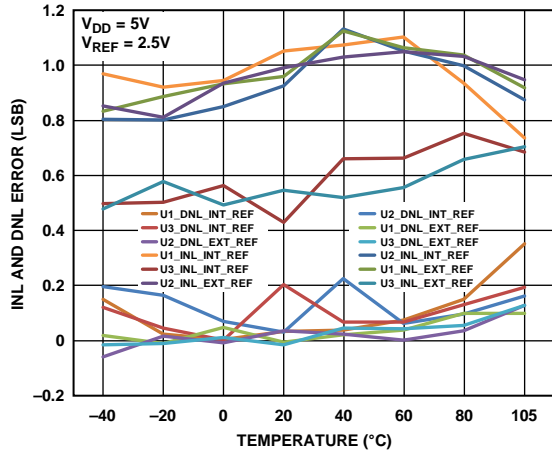


Figure 14. INL and DNL Error vs. Temperature (AD5693R)

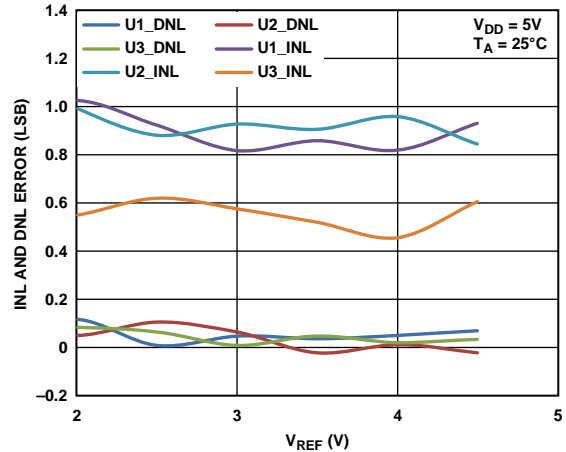


Figure 17. INL and DNL Error vs.  $V_{REF}$  (AD5693R)

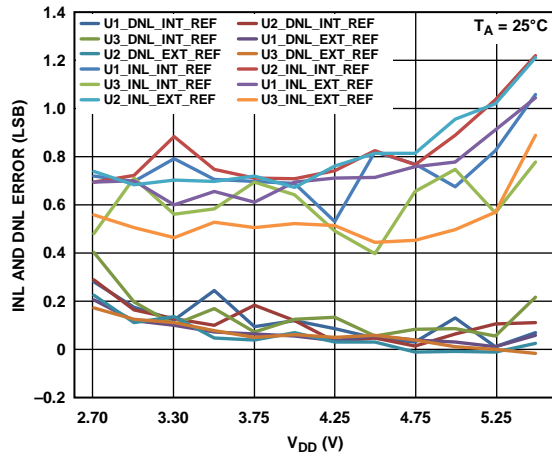


Figure 15. INL and DNL Error vs.  $V_{DD}$

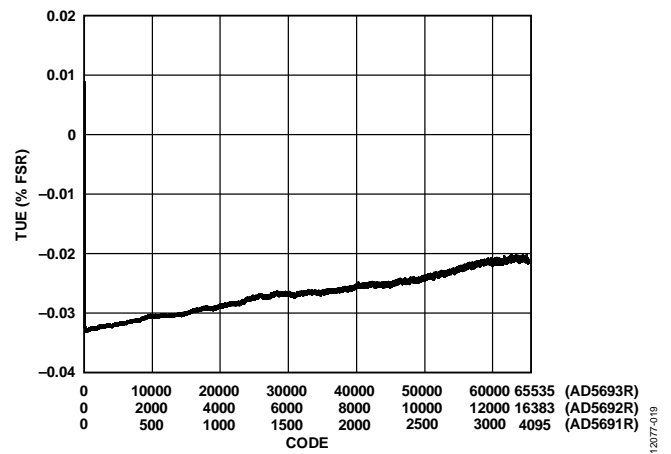


Figure 18. TUE vs. Code

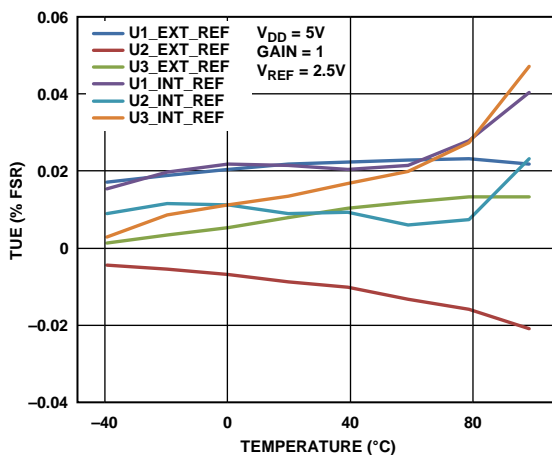


Figure 16. TUE vs. Temperature

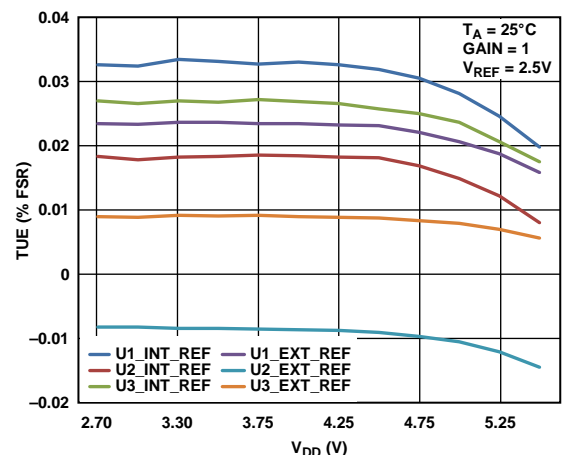


Figure 19. TUE vs.  $V_{DD}$

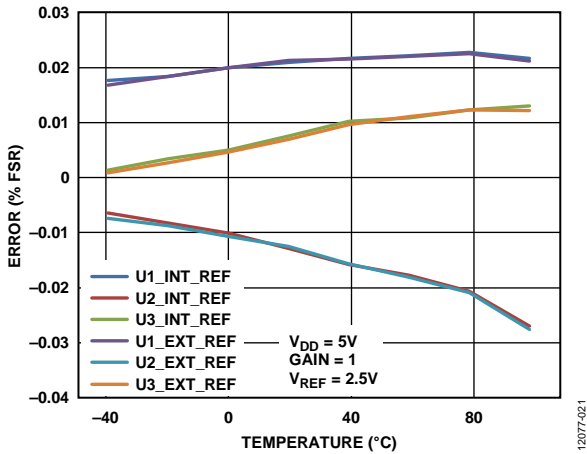


Figure 20. Gain Error and Full-Scale Error vs. Temperature

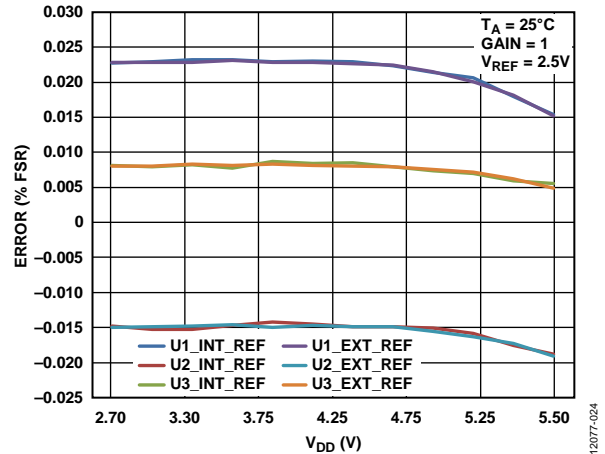


Figure 23. Gain Error and Full-Scale Error vs. V<sub>DD</sub>

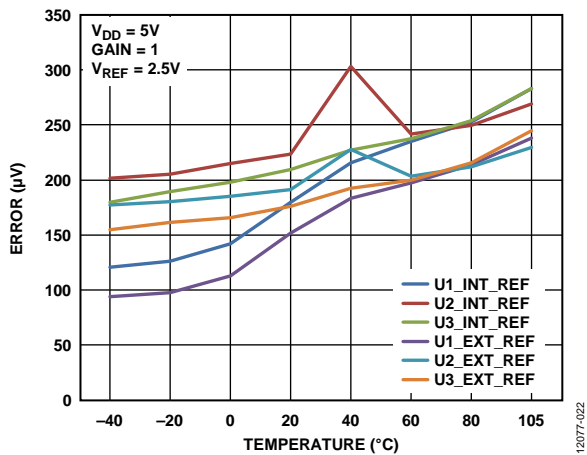


Figure 21. Zero Code Error and Offset Error vs. Temperature

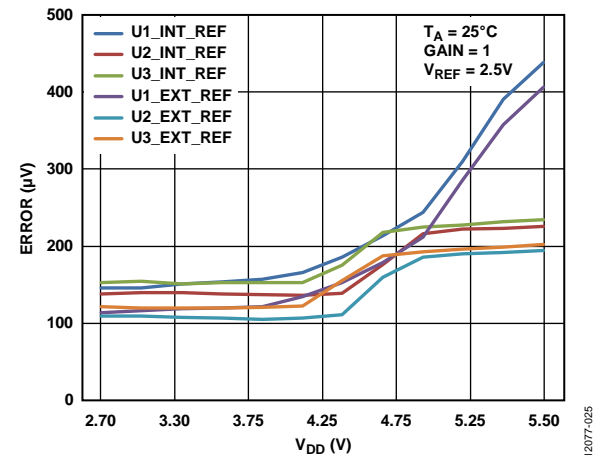


Figure 24. Zero Code Error and Offset Error vs. V<sub>DD</sub>

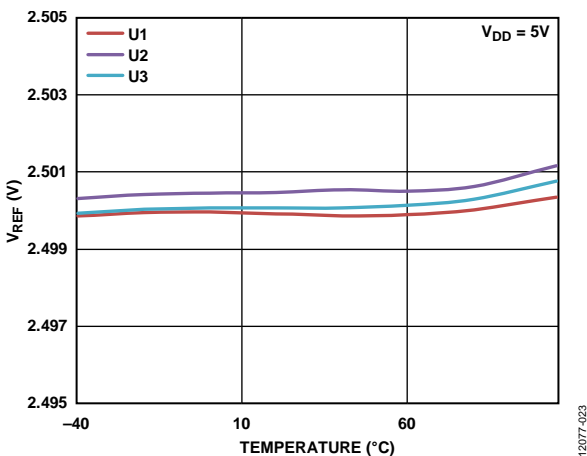


Figure 22. Internal Reference Voltage vs. Temperature (Grade B)

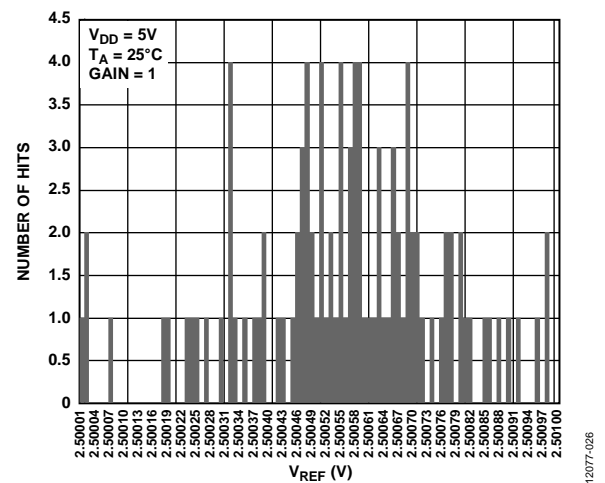


Figure 25. Reference Output Spread

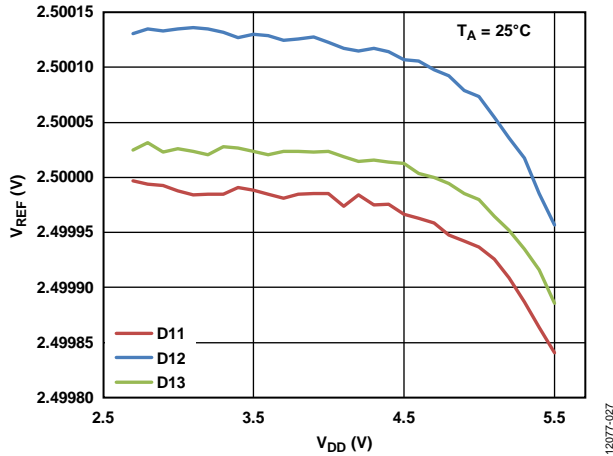


Figure 26. Internal Reference Voltage vs.  $V_{DD}$

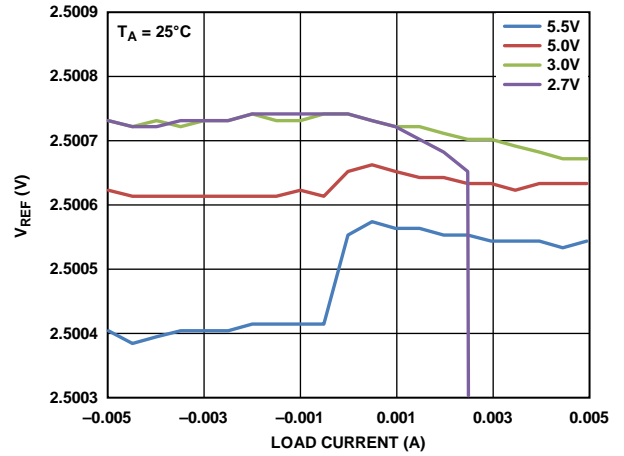


Figure 29. Internal Reference Voltage vs. Load Current

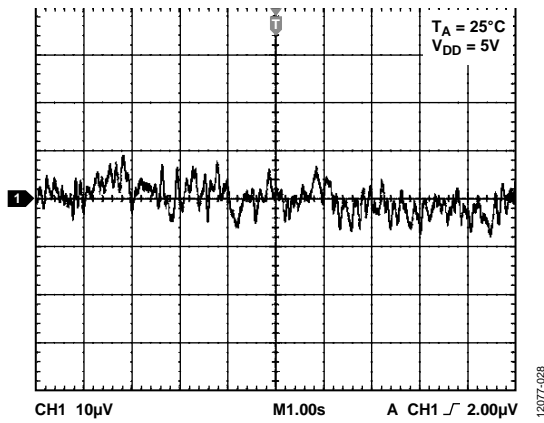


Figure 27. Internal Reference Noise, 0.1 Hz to 10 Hz

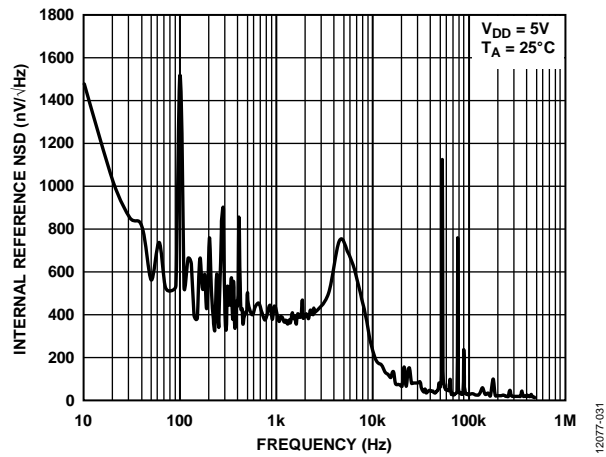


Figure 30. Internal Reference Noise Spectral Density vs. Frequency

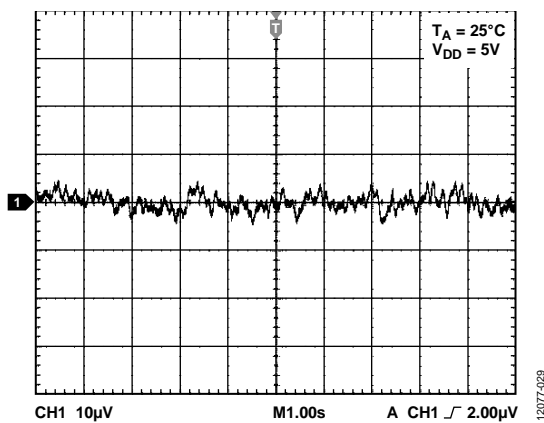


Figure 28. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference On

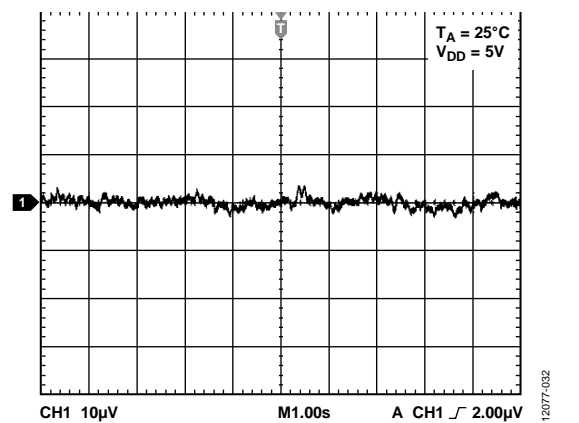


Figure 31. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

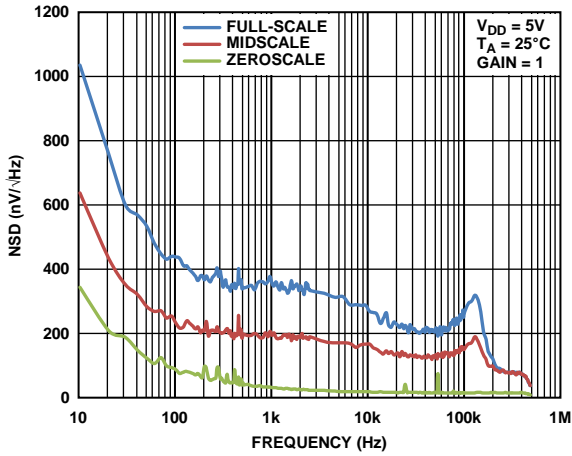


Figure 32. Noise Spectral Density vs. Frequency, Gain = 1

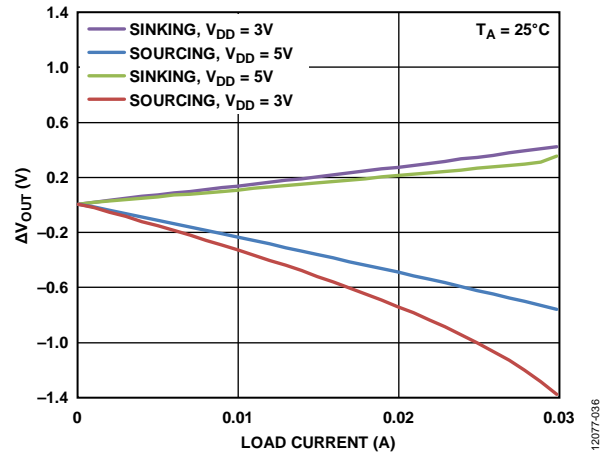


Figure 35. Headroom/Footroom vs. Load Current

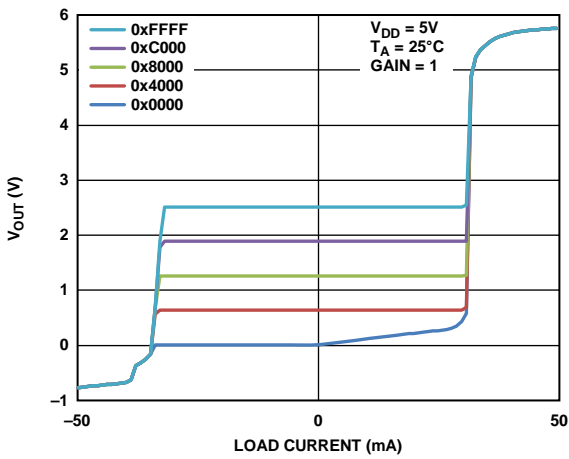


Figure 33. Source and Sink Capability, Gain = 1

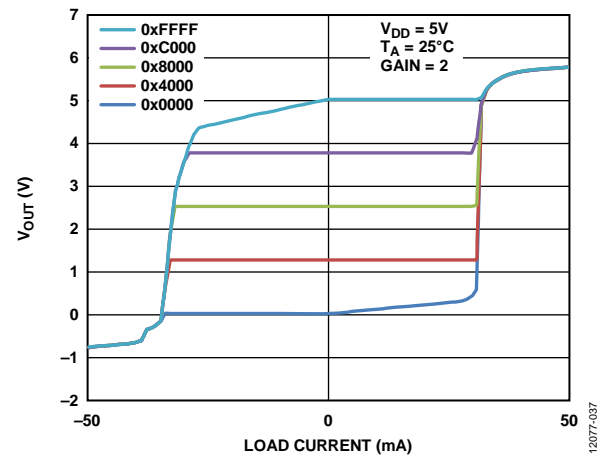


Figure 36. Source and Sink Capability, Gain = 2

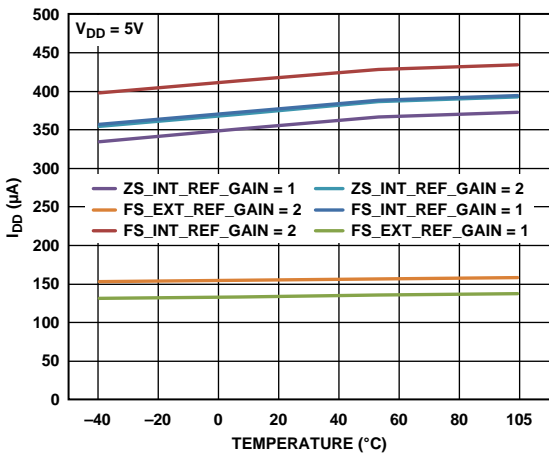


Figure 34.  $I_{DD}$  vs. Temperature

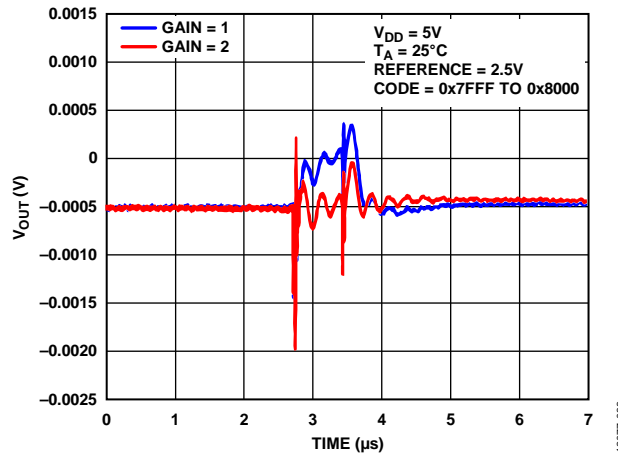


Figure 37. Digital-to-Analog Glitch Impulse

12077-033

12077-036

12077-034

12077-037

12077-035

12077-038

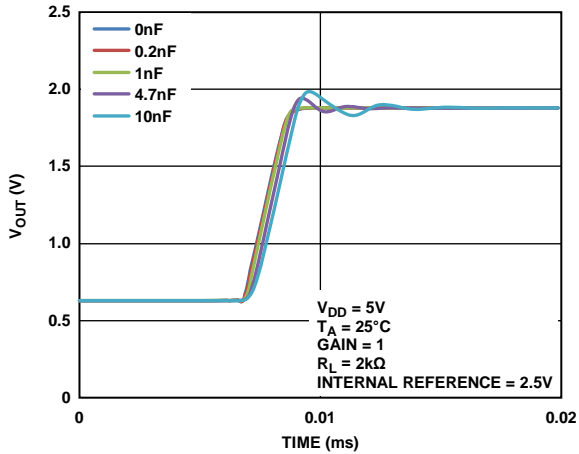


Figure 38. Capacitive Load vs. Settling Time, Gain = 1

12077-039

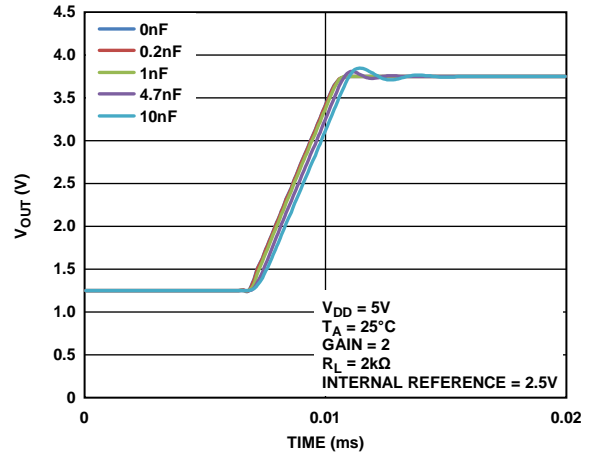


Figure 41. Capacitive Load vs. Settling Time, Gain = 2

12077-042

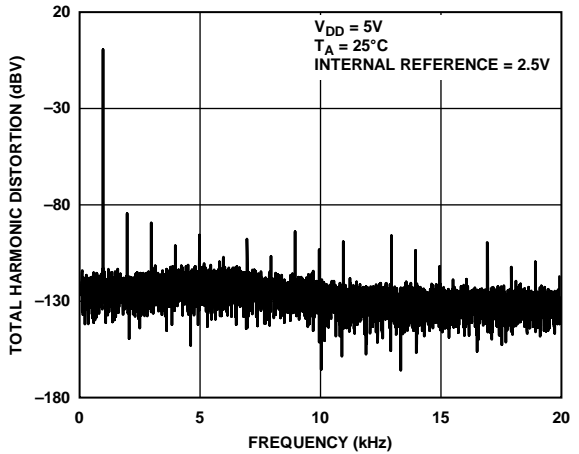


Figure 39. Total Harmonic Distortion at 1 kHz

12077-040

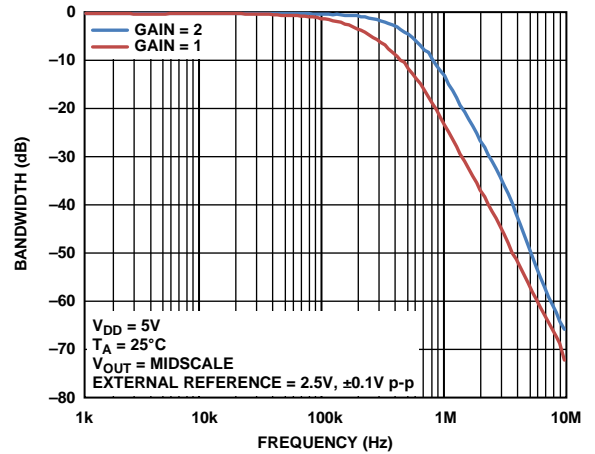


Figure 42. Multiplying Bandwidth, External Reference = 2.5 V, ± 0.1 V p-p, 10 kHz to 10 MHz

12077-043

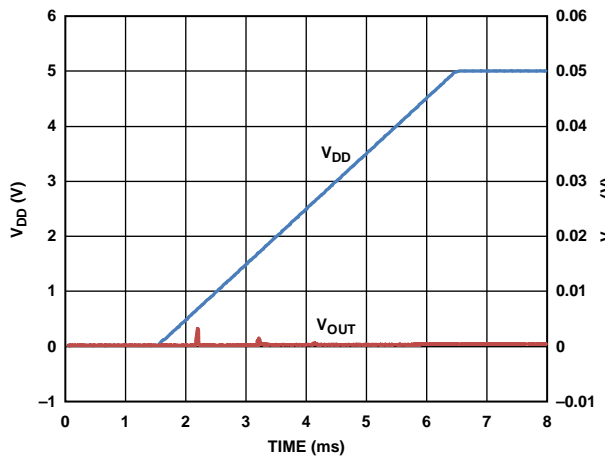


Figure 40. Power-On Reset to 0V

12077-041

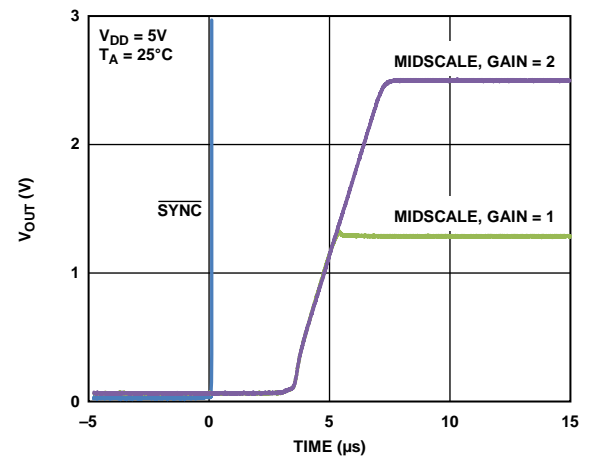


Figure 43. Exiting Power-Down to Midscale

12077-044

## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. For typical INL vs. code plots, see Figure 8, Figure 9, and Figure 10.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. For typical DNL vs. code plots, see Figure 11, Figure 12, and Figure 13.

### Zero Code Error

Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the [AD5693R/AD5692R/AD5691R](#) because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV. For plots of zero code error, see in Figure 21 and Figure 24.

### Full-Scale Error

Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be  $V_{DD} - 1$  LSB. Full-scale error is expressed in percent of full-scale range. For plots of full-scale error vs. temperature, see Figure 20 and Figure 23.

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

### Zero Code Error Drift

Zero code error drift is a measurement of the change in zero code error with a change in temperature. It is expressed in  $\mu\text{V}/^\circ\text{C}$ .

### Gain Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/ $^\circ\text{C}$ .

### Offset Error

Offset error is a measure of the difference between  $V_{OUT}$  (actual) and  $V_{OUT}$  (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the [AD5693R](#) with Code 512 loaded in the DAC register (Code 256 for the [AD5692R](#) and Code 128 for the [AD5693R](#)). It can be negative or positive.

### DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in  $V_{OUT}$  to a change in  $V_{DD}$  for full-scale output of the DAC. It is measured in mV/V.  $V_{REF}$  is held at 2 V, and  $V_{DD}$  is varied by  $\pm 10\%$ .

### Output Voltage Settling Time

This is the amount of time it takes for the output of a DAC to settle to a specified level for a  $\frac{1}{4}$  to  $\frac{3}{4}$  full-scale input change.

### Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000)

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

### Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/ $\sqrt{\text{Hz}}$ ). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/ $\sqrt{\text{Hz}}$ . For plots of noise spectral density, see Figure 28, Figure 31, and Figure 32. The noise spectral density for the reference is shown in Figure 27 and Figure 30.

### Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of these finite bandwidths. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

### Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

### Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/ $^\circ\text{C}$  as follows:

$$TC = \left[ \frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:

$V_{REFmax}$  is the maximum reference output measured over the total temperature range.

$V_{REFmin}$  is the minimum reference output measured over the total temperature range.

$V_{REFnom}$  is the nominal reference output voltage, 2.5 V.

$TempRange$  is the specified temperature range,  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .



## THEORY OF OPERATION

### DIGITAL-TO-ANALOG CONVERTER

The AD5693R/AD5692R/AD5691R are single 16-bit, 14-bit, and 12-bit, serial input, voltage output DACs with a 2.5 V internal reference. The devices operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5693R/AD5692R/AD5691R in a 24-bit word format via an I<sup>2</sup>C serial interface.

The AD5693R/AD5692R/AD5691R incorporate a power-on reset circuit that ensures that the DAC output powers up to zero scale. The devices also have a software power-down mode that reduces the current consumption to 2 μA maximum.

### TRANSFER FUNCTION

The internal reference is on by default. The input coding to the DAC is straight binary. The ideal output voltage is given by the following equations:

For the AD5693R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[ \frac{D}{65,536} \right]$$

For the AD5692R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[ \frac{D}{16,384} \right]$$

For the AD5691R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[ \frac{D}{4096} \right]$$

where:

*D* is the decimal equivalent of the binary code that is loaded to the DAC register.

*Gain* is the gain of the output amplifier and it is set to ×1 by default. The gain can also be set to ×2 using the gain bit in the control register.

### DAC ARCHITECTURE

The AD5693R/AD5692R/AD5691R implement a segmented string DAC architecture with an internal output buffer. Figure 44 shows the internal block diagram.

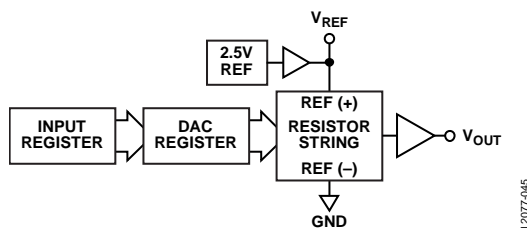


Figure 44. DAC Channel Architecture Block Diagram

The simplified segmented resistor string DAC structure is shown in Figure 45. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has same value, *R*, the string DAC is guaranteed monotonic.

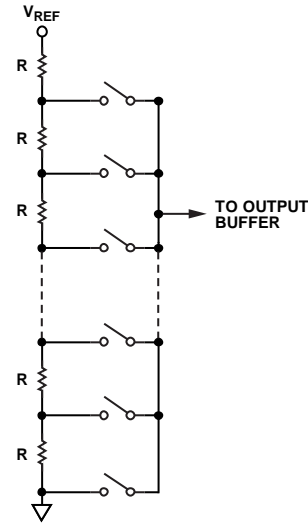


Figure 45. Simplified Resistor String Structure

### Internal Reference

The AD5693R/AD5692R/AD5691R on-chip reference is on at power-up but can be disabled via a write to the control register.

The AD5693R/AD5692R/AD5691R each have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V, depending on the state of the gain bit.

The internal reference is available at the *V<sub>REF</sub>* pin. It is internally buffered and capable of driving external loads of up to 5 mA.

### External Reference

The *V<sub>REF</sub>* pin can be con-figured as an input pin on the AD5693R/AD5692R/AD5691R, allowing the use of an external reference if the application requires it.

In the AD5693R/AD5692R/AD5691R, the default condition of the on-chip reference is on at power-up. Before connecting an external reference to the pin, disable the internal reference by writing to the REF bit (Bit DB12) in the control register.

**Output Buffer**

The output buffer is designed as an input/output rail-to-rail buffer, which gives a maximum output voltage range of up to  $V_{DD}$ . The gain bit sets the segmented string DAC gain to  $\times 1$  or  $\times 2$ , as shown in Table 12.

The output buffer voltage is determined by  $V_{REF}$ , the gain bit, and the offset and gain errors.

The output buffer can drive a 10 nF capacitance with a 2 k $\Omega$  resistor in parallel, as shown in Figure 38 and Figure 41. If a higher capacitance load is required, use the snubber method or a shunt resistor to isolate the load from the output amplifier. The slew rate is 0.7 V/ $\mu$ s with a  $\frac{1}{4}$  to  $\frac{3}{4}$  scale settling time of 5  $\mu$ s.

## SERIAL INTERFACE

The AD5693R/AD5692R/AD5691R have 2-wire, I<sup>2</sup>C-compatible serial interfaces. These devices can be connected to an I<sup>2</sup>C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD5693R/AD5692R/AD5691R support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

### I<sup>2</sup>C SERIAL DATA INTERFACE

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the 9th clock pulse (this is called the acknowledge (ACK) bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

### I<sup>2</sup>C ADDRESS

The AD5693R/AD5692R/AD5691R have a 7-bit slave address. The five MSBs are 10011. The second last bit set by the state of the A0 address pin and the LSB is 0. The ability to make hardwired changes to A0 lets the user have two of these devices on one bus, as outlined in Table 9. Additionally, the pin can be updated before starting the transmission, allowing multiple devices in the same bus by connecting the pin to a GPIO or a multiplexer.

Table 9. Device Address Selection

A0 Pin Connection	A0	I <sup>2</sup> C Address
GND	0	1001100
V <sub>LOGIC</sub> (V <sub>DD</sub> on LFCSP Package)	1	1001110

### WRITE OPERATION

When writing to the AD5693R/AD5692R/AD5691R, the user must begin with a start condition followed by an address byte (R/W = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low, as shown in Figure 46. The AD5693R/AD5692R/AD5691R require a command byte that controls various DAC functions (see Table 10) and two bytes of data for the DAC. All these data bytes are acknowledged by the AD5693R/AD5692R/AD5691R. A stop condition follows. The write sequence is shown in Figure 46.

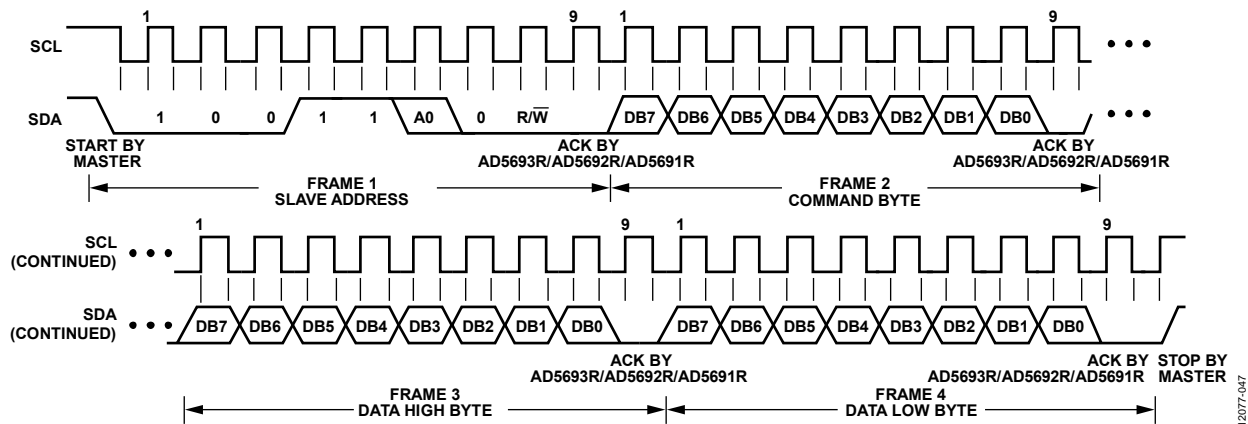


Figure 46. I<sup>2</sup>C Write Operation

1207-047

Table 10. Command Table<sup>1</sup>

Command Byte					Data High Byte		Data Low Byte				Operation	
DB7	DB6	DB5	DB4	[DB3:DB0]	[DB7:DB3]	[DB2:DB0]	[DB7:DB4]	DB3	DB2	DB1		DB0
0	0	0	0	XXXX	XXXXX	XXX	XXXX	X	X	X		NOP: do nothing.
0	0	0	1	XXXX	DB15:DB11	DB10:DB8	DB7:DB4	DB3 <sup>2</sup>	DB2 <sup>2</sup>	DB1 <sup>2,3</sup>	DB0 <sup>2,3</sup>	Write input register.
0	0	1	0	XXXX	XXXXX	XXX	XXXX	X	X	X	X	Update DAC register (LDAC software).
0	0	1	1	XXXX	DB15:DB11	DB10:DB8	DB7:DB4	DB3 <sup>2</sup>	DB2 <sup>2</sup>	DB1 <sup>2,3</sup>	DB0 <sup>2,3</sup>	Write DAC and input registers.
0	1	0	0	XXXX	DB15:DB11	000	0000	0	0	0	0	Write control register.

<sup>1</sup> X is don't care.

<sup>2</sup> This bit is a don't care for the AD5691R.

<sup>3</sup> This bit is a don't care for the AD5692R.

### Write Input Register

The input register allows the preloading of a new value for the DAC register. The transfer from the input register to the DAC register can be triggered by hardware, the  $\overline{\text{LDAC}}$  pin, or by software using Command 2.

If new data is loaded into the DAC register, the DAC register automatically overwrites the input register.

### Update DAC Register

This command transfers the contents of the input register to the DAC register and, consequently, the  $V_{\text{OUT}}$  pin is updated. The data contained in the serial write is ignored.

This operation is equivalent to a software  $\overline{\text{LDAC}}$ .

### Write DAC Register

This command updates the DAC output on completion of the write operation. The input register is refreshed automatically with the DAC register value.

### Write Control Register

The control register is used to set the power-down and gain functions. It is also used to enable/disable the internal reference and perform a software reset. See Table 11 for the control register functionality.

Table 11. Control Register Bits

D15	D14	D13	D12	D11
Reset	PD1	PD0	REF	Gain

### Gain Bit

The gain bit selects the gain of the output amplifier. Table 12 shows how the output voltage range corresponds to the state of the gain bit.

Table 12. Gain Bit

Gain	Output Voltage Range
0	0 V to $V_{\text{REF}}$ (default)
1	0 V to $2 \times V_{\text{REF}}$

### REF Bit

The on-chip reference is on at power-up by default. This reference can be turned on or off by setting a software programmable bit, DB12, in the control register. Table 13 shows how the state of the bit corresponds to the mode of operation.

To reduce the power consumption, it is recommended to disable the internal reference if the device is placed in power-down mode.

Table 13. Reference Bit

REF	Reference Function
0	Reference enabled (default)
1	Reference disabled

### PD0 and PD1 Bits

The AD5693R/AD5692R/AD5691R contain two separate modes of operation that are accessed by writing to the control register.

In normal mode, the output buffer is directly connected to the  $V_{\text{OUT}}$  pin.

In power-down mode, the output buffer is internally disabled and the  $V_{\text{OUT}}$  pin output impedance can be selected to a well known value, as shown in Table 14.

Table 14. Operation Modes

Operating Mode	PD1	PD0
Normal Mode	0	0
Power-Down Modes		
1 k $\Omega$ Output Impedance	0	1
100 k $\Omega$ Output Impedance	1	0
Three-State Output Impedance	1	1

In power-down mode, the device disables the output buffer but does not disable the internal reference. To achieve maximum power savings, it is recommended to disable the internal reference.

Disabling both the internal reference and the output buffer results in the supply current falling to 2  $\mu$ A at 5 V.

The output stage is shown in Figure 47.

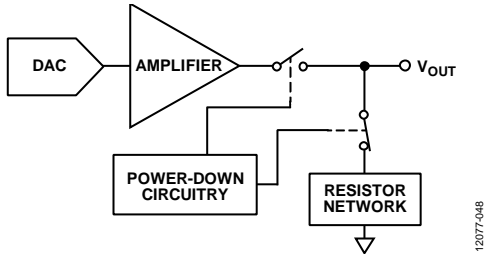


Figure 47. Output Stage During Power-Down

The output amplifier is shut down when the power-down mode is activated. However, unless the internal reference is powered down (using Bit DB12 in the control register), the bias generator, reference, and resistor string remain on. The supply current falls to 2  $\mu$ A at 5 V. The contents of the DAC register are

unaffected when in power-down mode, and the DAC register can continue to be updated. The time that is required to exit power-down is typically 4  $\mu$ s for  $V_{DD} = 5$  V, or 600  $\mu$ s if the reference is disabled.

**Reset Bit**

The AD5693R/AD5692R/AD5691R control register contains a software reset bit that resets the DAC to zero-scale and resets the input, DAC, and control registers to their default values. A software reset is initiated by setting the RESET bit in the control register to 1. When the software reset has completed, the reset bit is cleared to 0 automatically.

**READ OPERATION**

When reading the input register back from the AD5693R/AD5692R/AD5691R DACs, the user begins with an address byte ( $R/\bar{W} = 1$ ), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. Two bytes of data containing the contents of the input register are then read from the DAC, as shown in Figure 48. A NACK condition from the master followed by a STOP condition completes the read sequence.

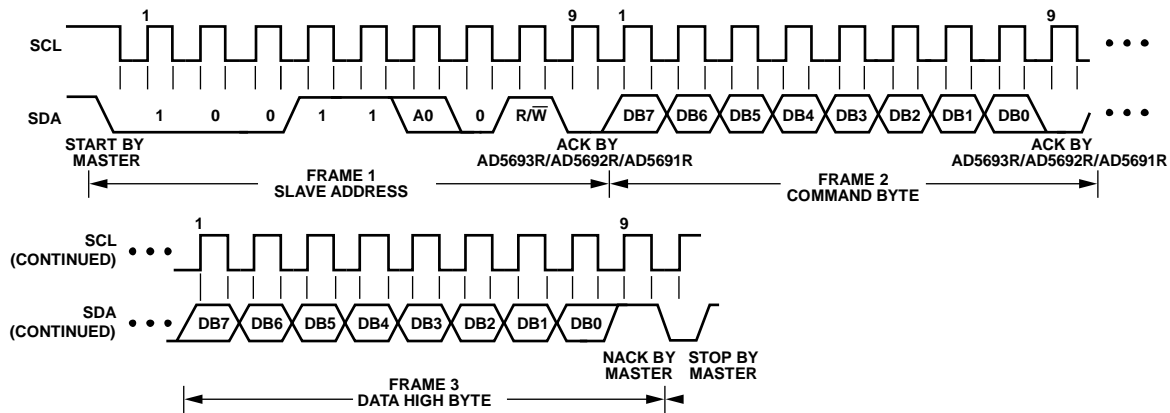


Figure 48. I<sup>2</sup>C Read Operation

## LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5693R/AD5692R/AD5691R DAC has a double buffered interface consisting of an input register and a DAC register. The  $\overline{\text{LDAC}}$  pin transfers data from the input register to the DAC register, and the output is updated.

### Synchronous DAC Update

If the  $\overline{\text{LDAC}}$  pin is held low while the input register is written, the DAC register, input register, and output are updated on the last SCL falling edge before the ACK bit, as shown in Figure 4.

### Asynchronous DAC Update

$\overline{\text{LDAC}}$  is held high while data is transmitted to the device. The DAC output is updated by taking  $\overline{\text{LDAC}}$  low after the stop condition has been generated. The output DAC is updated on the falling edge of the  $\overline{\text{LDAC}}$  pin. If  $\overline{\text{LDAC}}$  is pulsed while the device is accessed, the pulse is ignored.

## HARDWARE $\overline{\text{RESET}}$

$\overline{\text{RESET}}$  is an active low signal that resets the DAC output to zero-scale and sets the input, DAC, and control registers to their default values. It is necessary to keep  $\overline{\text{RESET}}$  low for 75 ns to complete the operation. When the  $\overline{\text{RESET}}$  signal is returned high, the output remains at zero scale until a new value is programmed. While the  $\overline{\text{RESET}}$  pin is low, the AD5693R/AD5692R/AD5691R ignore any new command. If the  $\overline{\text{RESET}}$  pin is held low at power-up, the internal reference is not initialized correctly until the  $\overline{\text{RESET}}$  pin is released.

## THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

The thermal hysteresis data is shown in Figure 49. It is measured by sweeping the temperature from ambient to  $-40^{\circ}\text{C}$ , then to  $+105^{\circ}\text{C}$ , and finally returning to ambient. The  $V_{\text{REF}}$  delta is measured between the two ambient measurements; the result is shown in solid lines in Figure 49. The same temperature sweep and measurements were immediately repeated; the results are shown in dashed lines in Figure 49.

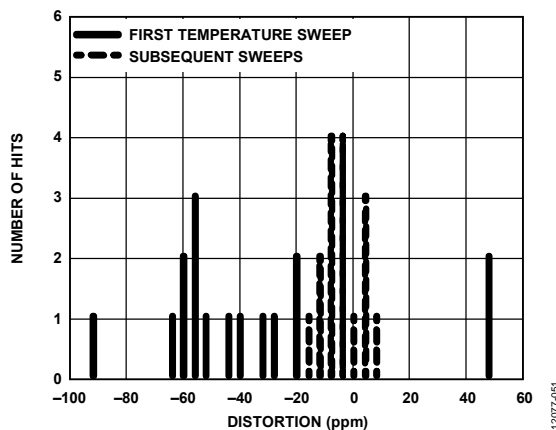


Figure 49. Thermal Hysteresis

## POWER-UP SEQUENCE

Because diodes limit the voltage compliance at the digital pins and analog pins, it is important to power GND first before applying any voltage to  $V_{\text{DD}}$ ,  $V_{\text{OUT}}$ , and  $V_{\text{LOGIC}}$ . Otherwise, the diode is forward-biased such that  $V_{\text{DD}}$  is powered unintentionally. The ideal power-up sequence is GND,  $V_{\text{DD}}$ ,  $V_{\text{LOGIC}}$ ,  $V_{\text{REF}}$ , followed by the digital inputs.

## LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the ADCs are mounted such that the AD5693R/AD5692R/AD5691R lie on the analog plane.

Ensure that the AD5693R/AD5692R/AD5691R have ample supply bypassing of 10  $\mu\text{F}$ , in parallel with a 0.1  $\mu\text{F}$  capacitor on each supply that is located as near the package as possible (ideally, right up against the device). The 10  $\mu\text{F}$  capacitors are of the tantalum bead type. Ensure that the 0.1  $\mu\text{F}$  capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where many devices are on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The LFCSP package of the AD5693R/AD5692R/AD5691R has an exposed pad beneath the device. Connect this pad to the GND supply of the device. For optimum performance, use special consideration when designing the motherboard and mounting the package. For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the package to the corresponding thermal land pad on the PCB. Design thermal vias into the PCB land pad area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 50) to provide a natural heat sinking effect.

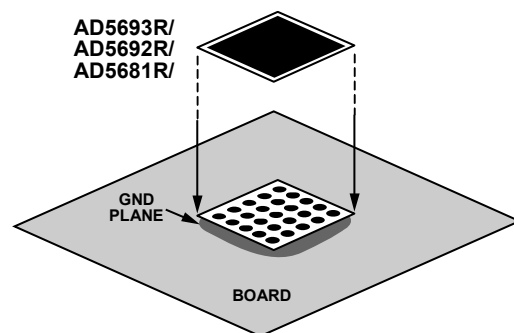


Figure 50. Pad Connection to Board

OUTLINE DIMENSIONS

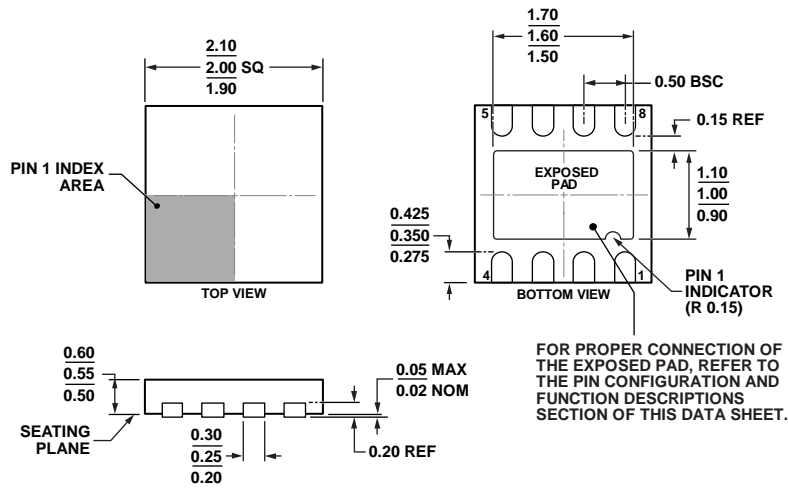
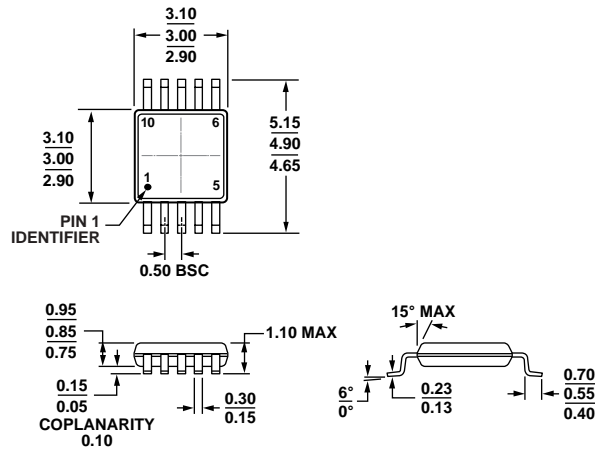


Figure 51. 8-Lead Lead Frame Chip Scale Package [LFCSP\_UD]  
 2.00 × 2.00 mm Body, Ultra Thin, Dual Lead  
 (CP-8-10)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA  
 Figure 52. 10-Lead Mini Small Outline Package [MSOP]  
 (RM-10)  
 Dimensions shown in millimeters

01-14-2013-C

081705-A

## ORDERING GUIDE

Model <sup>1</sup>	Resolution (Bits)	Pinout	Temperature Range	Performance	Package Description	Package Option	Branding
AD5693RACPZ-RL7	16	LDAC	-40°C to +105°C	A-Grade	8-Lead LFCSP_UD	CP-8-10	AB
AD5693RARMZ	16		-40°C to +105°C	A-Grade	10-Lead MSOP	RM-10	DJU
AD5693RARMZ-RL7	16		-40°C to +105°C	A-Grade	10-Lead MSOP	RM-10	DJU
AD5693RBRMZ	16		-40°C to +105°C	B-Grade	10-Lead MSOP	RM-10	DJV
AD5693RBRMZ-RL7	16		-40°C to +105°C	B-Grade	10-Lead MSOP	RM-10	DJV
AD5692RACPZ-RL7	14	LDAC	-40°C to +105°C	A-Grade	8-Lead LFCSP_UD	CP-8-10	4M
AD5691RACPZ-1RL7	12	V <sub>LOGIC</sub>	-40°C to +105°C	A-Grade	8-Lead LFCSP_UD	CP-8-10	5W
AD5691RBCPZ-RL7	12	LDAC	-40°C to +105°C	B-Grade	8-Lead LFCSP_UD	CP-8-10	6M
AD5691RBRMZ	12		-40°C to +105°C	B-Grade	10-Lead MSOP	RM-10	DK2
AD5691RBRMZ-RL7	12		-40°C to +105°C	B-Grade	10-Lead MSOP	RM-10	DK2
EVAL-AD5693RSDZ					Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



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[AD5693RARMZ](#) [AD5693RBRMZ](#)