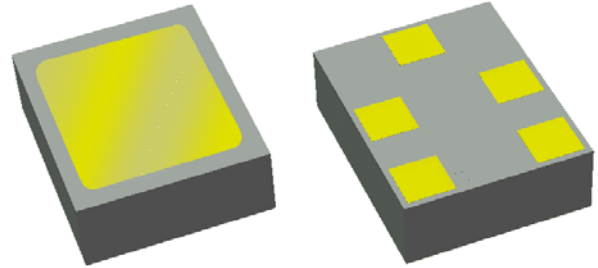


Preliminary Data Sheet

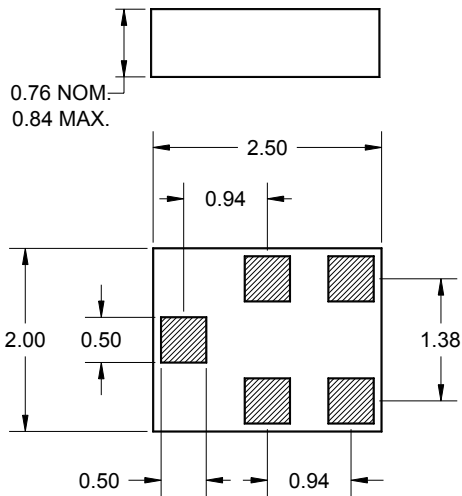
Features

- For KPCS applications
- Usable bandwidth 30 MHz
- No impedance matching required
- Single-ended input
- Balanced output
- Superior amplitude and phase balance
- Ceramic Surface Mount Package (SMP)
- Small size



Package

Surface Mount 2.50 x 2.00 x 0.76 mm

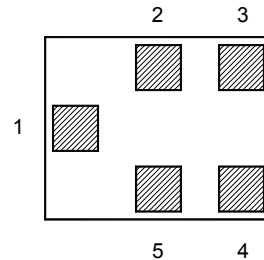


Dimensions shown are nominal in millimeters
 All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
 Lid: Kovar or Alloy 42, Au over Ni plated
 Terminations: Au plating 0.5 - 1.0 μ m,
 over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



Pin No.	Description
1	Input unbalanced
3,4	Output balanced
2,5	Case ground

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

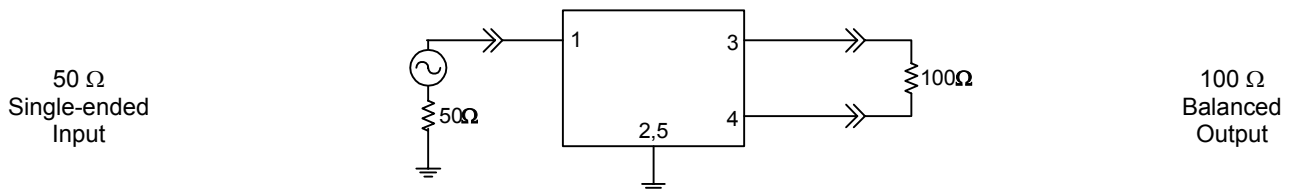
Operating Temperature Range: ⁽²⁾ -30 to +85 °C

Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	1855	-	MHz
Maximum Insertion Loss 1840 - 1870 MHz	-	3	3.5	dB
Absolute Attenuation				
100 - 1025 MHz	45	50	-	dB
1025 - 1750 MHz	40	50	-	dB
1750 - 1780 MHz	35	45	-	dB
1930 - 2220 MHz	25	30	-	dB
2220 - 6000 MHz	40	50	-	dB
Output Amplitude Balance (S₃₁/S₂₁) 1840 - 1870 MHz	-1.5	±1.2	1.5	dB
Output Phase Balance [φ(S₃₁) - φ(S₂₁) + 180] 1840 - 1870 MHz	-8	±5	8	degree
Input/Output VSWR 1840 - 1870 MHz	-	1.9	2.5	-
Optimal Source Impedance ⁽⁴⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁴⁾	-	100	-	Ω

Notes:

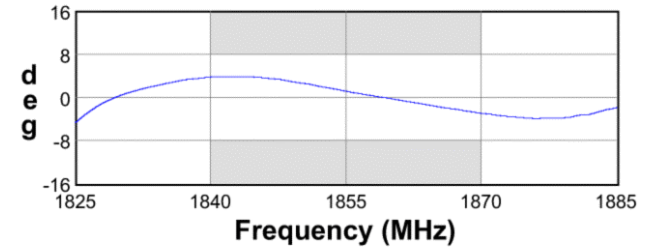
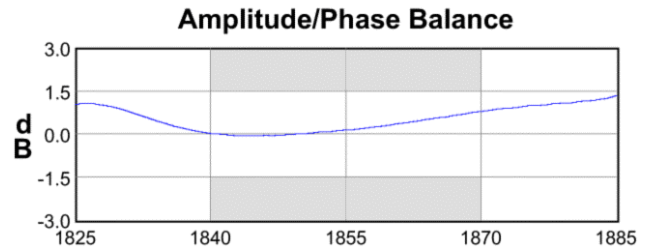
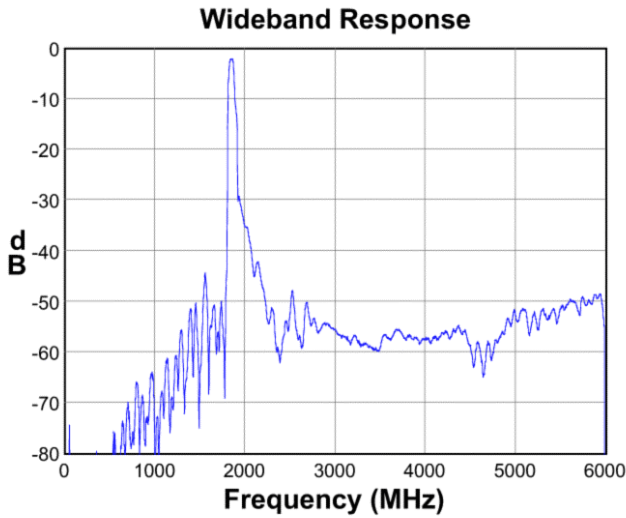
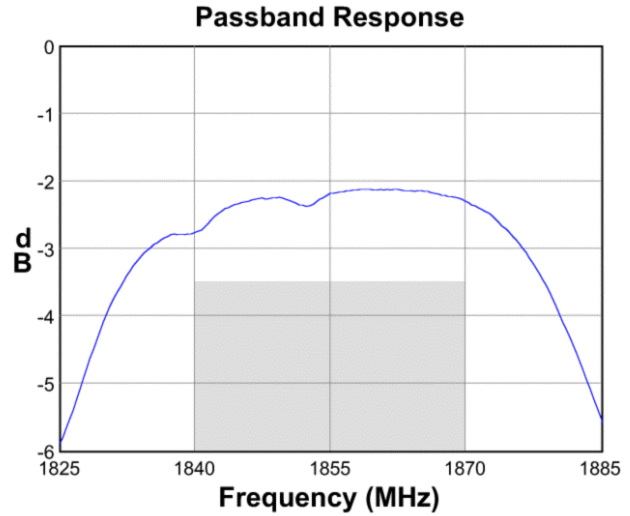
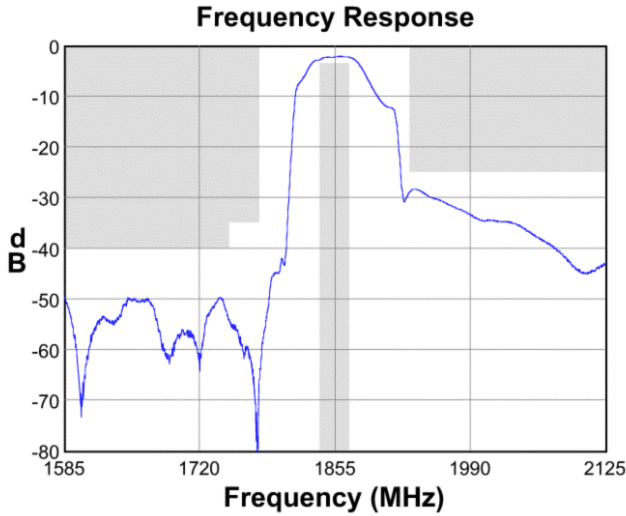
1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

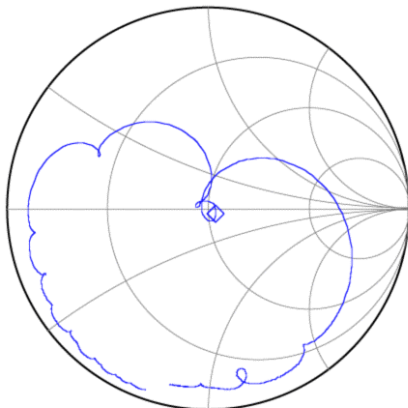


Preliminary Data Sheet

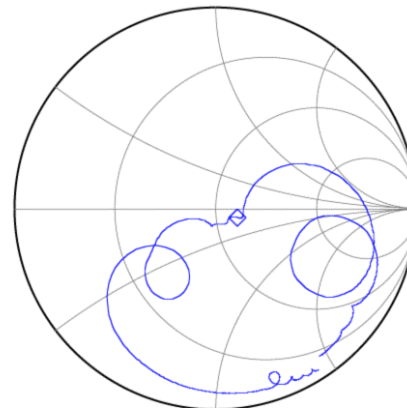
Typical Performance (at +25°C)



Input Smith Chart



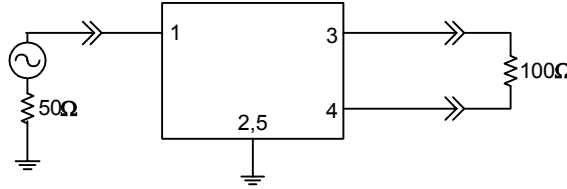
Output Smith Chart



Preliminary Data Sheet

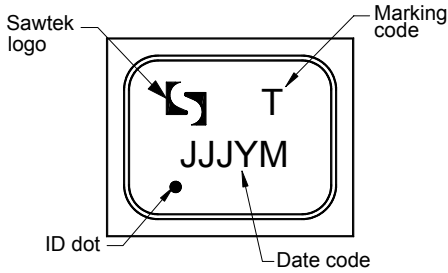
Matching Schematics

50 Ω
Single-ended
Input

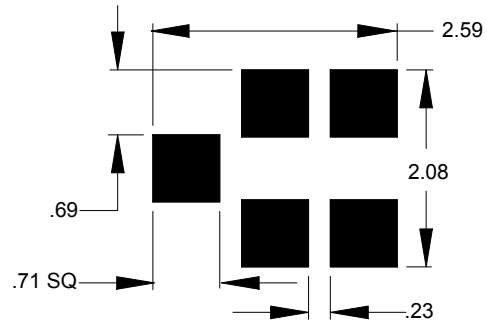


100 Ω
Balanced
Output

Marking PCB Footprint

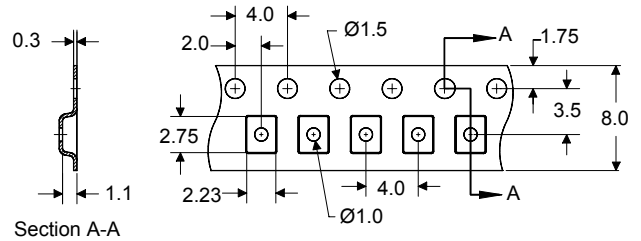
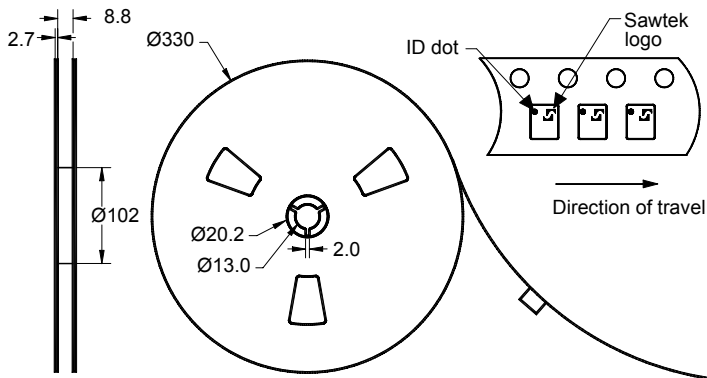


The date code consists of: JJJ = Julian day,
Y = last digit of year, M = manufacturing site code



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

Preliminary Data Sheet

Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[Other Technical Information](#)

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