AH115 / ECP050G

½ Watt, High Linearity InGaP HBT Amplifier

The Communications Edge ™

Product Information

Product Features

- 1800 – 2300 MHz
- +28.5 dBm P1dB
- +44 dBm Output IP3
- 14 dB Gain @ 1960 MHz
- +5V Single Positive Supply
- MTTF > 100 Years
- Lead-free/green/RoHS-compliant SOIC-8 SMT Pkg.

Applications

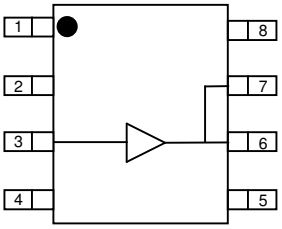
- Mobile Infrastructure
- Final Stage Amplifier for Repeaters

Product Description

The AH115 / ECP050 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrow-band tuned application circuits with up to +44 dBm OIP3 and +28.5 dBm of compressed 1-dB power. All devices are 100% RF and DC tested. The AH115 / ECP050 is available in lead-free/green/RoHS-compliant SOIC-8 package.

The product is targeted for use as driver amplifiers for wireless infrastructure where high linearity and medium power is required. The internal active bias allows the AH115 / ECP050 to maintain high linearity over temperature and operate directly off a +5 V supply. This combination makes the device an excellent fit for transceiver line cards and power amplifiers in current and next generation multi-carrier 3G base stations.

Functional Diagram



Function	Pin No.
Vref	1
Input / Base	3
Output / Collector	6, 7
Vbias	8
GND	Backside Paddle
N/C or GND	2, 4, 5

Specifications (1)

Parameters	Units	Min	Typ	Max
Operational Bandwidth	MHz	1800		2300
Test Frequency	MHz		2140	
Gain	dB	12.5	14.4	
Input Return Loss	dB		23	
Output Return Loss	dB		8	
Output P1dB	dBm	+26.5	+28.5	
Output IP3 (2)	dBm	+41	+42	
IS-95A Channel Power @ -45 dBc ACPR, 1960 MHz	dBm		+22.5	
W-CDMA Channel Power @ -45 dBc ACLR, 2140 MHz	dBm		+20	
Noise Figure	dB		5.3	
Operating Current Range (3)	mA	200	250	300
Device Voltage	V		+5	

1. Test conditions unless otherwise noted. 25ºC, Vsupply = +5 V in tuned application circuit.
2. 3OIP measured with two tones at an output power of +11 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. This corresponds to the quiescent current or operating current under small-signal conditions. It is expected that the current can increase up to 300mA at P1dB.

Typical Performance (1)

Parameters	Units	Typical	
Frequency	MHz	1960	2140
Gain	dB	14.3	14.4
S11	dB	-12	-23
S22	dB	-8	-8
Output P1dB	dBm	+28.3	+28.5
Output IP3 (2)	dBm	+44	+42
IS-95A Channel Power @ -45 dBc ACPR,	dBm	+22.5	
W-CDMA Channel Power @ -45 dBc ACLR	dBm		+20
Noise Figure	dB	5	5.3
Supply Bias		+5 V @ 250 mA	

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-65 to +150 °C
RF Input Power (continuous)	+22 dBm
Device Voltage	+8 V
Device Current	400 mA
Device Power	2 W
Junction Temperature	+250 °C

Operation of this device above any of these parameters may cause permanent damage.

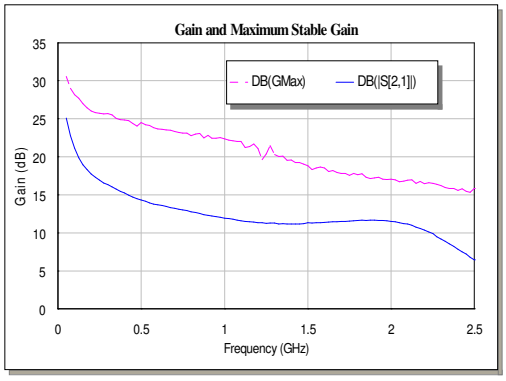
Ordering Information

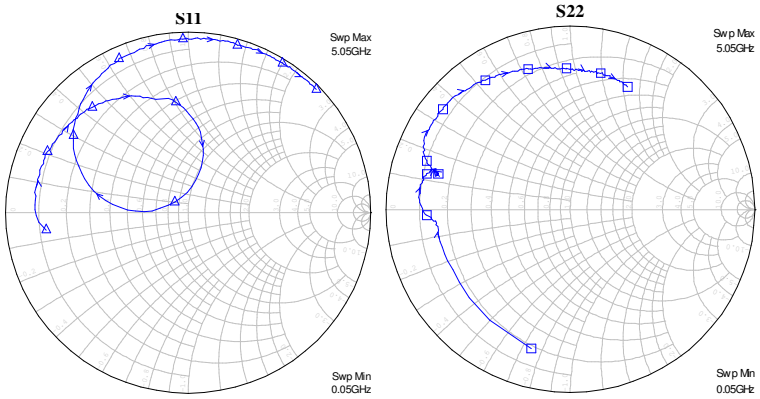
Part No.	Description
AH115-S8	½ Watt, High Linearity InGaP HBT Amplifier (lead-tin SOIC-8 Pkg)
ECP050G	½ Watt, High Linearity InGaP HBT Amplifier (lead-tin SOIC-8 Pkg)
AH115-S8G	½ Watt, High Linearity InGaP HBT Amplifier (lead-free/green/RoHS-compliant SOIC-8 Pkg)
AH115-S8PCB1960	1960 MHz Evaluation Board
AH115-S8PCB2140	2140 MHz Evaluation Board

Specifications and information are subject to change without notice

Typical Device Data

S-Parameters (V_{cc} = +5 V, I_{cc} = 250 mA, T = 25°C, unmatched 50 ohm system)



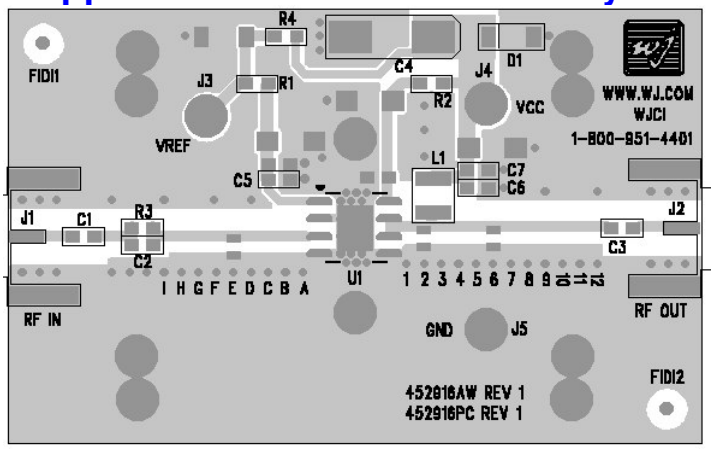


Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The return loss plots are shown from 50 – 5050 MHz, with markers placed at 0.5 – 5.05 GHz in 0.5 GHz increments.

S-Parameters (V_{cc} = +5 V, I_{cc} = 250 mA, T = 25°C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-2.11	-172.90	25.10	133.84	-36.03	31.44	-2.06	-105.55
100	-1.59	-178.94	21.15	126.67	-35.22	15.04	-2.73	-138.75
200	-1.51	173.71	17.75	124.19	-34.29	7.30	-2.80	-160.44
400	-1.45	163.84	15.23	111.50	-34.45	-2.16	-2.73	-174.00
600	-1.58	153.68	13.69	98.94	-33.58	-2.99	-1.96	-179.13
800	-1.78	144.31	12.77	84.57	-32.84	-12.80	-1.68	172.00
1000	-1.96	134.21	11.94	69.70	-32.77	-18.76	-1.85	166.98
1200	-2.46	123.44	11.36	55.57	-31.79	-30.73	-2.14	164.05
1400	-3.30	111.21	11.17	40.93	-31.12	-45.14	-2.30	163.07
1600	-4.70	92.57	11.39	22.80	-30.30	-61.92	-2.52	164.84
1800	-8.15	78.58	11.64	1.64	-29.47	-83.99	-2.43	164.25
2000	-19.01	93.29	11.51	-25.24	-29.31	-112.79	-1.84	162.38
2200	-9.59	177.56	10.35	-55.97	-30.51	-150.45	-1.22	155.68
2400	-4.09	159.30	7.87	-83.78	-32.59	177.62	-1.06	147.58
2600	-1.99	141.65	4.95	-105.90	-33.96	137.14	-1.07	139.74
2800	-1.12	127.57	1.97	-122.86	-34.68	109.27	-1.19	132.15
3000	-0.72	116.11	-0.88	-136.93	-35.64	81.83	-1.44	125.05

Application Circuit PC Board Layout

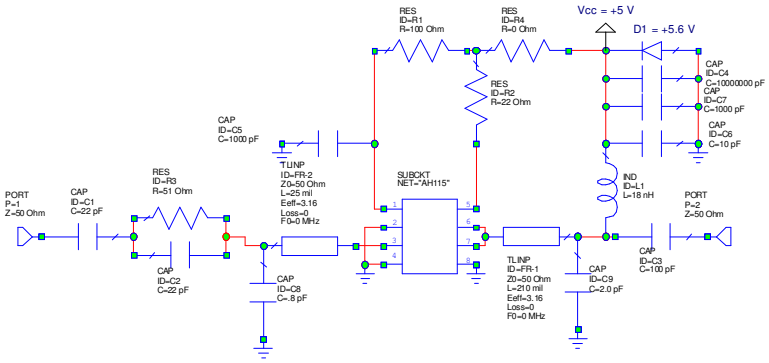


Circuit Board Material: .014" Getek, 4 - layer, 1 oz copper, Microstrip line details: width = .026", spacing = .026"
The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050" increments.

1960 MHz Application Circuit (AH115-S8PCB1960)

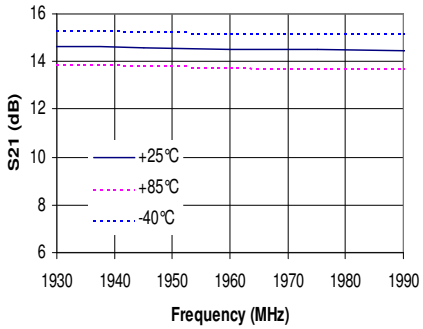
Typical RF Performance at 25°C

Frequency	1960 MHz
S21 – Gain	14.3 dB
S11 – Input Return Loss	-12 dB
S22 – Output Return Loss	-8 dB
Output P1dB	+28.3 dBm
Output IP3 (+11 dBm / tone, 1 MHz spacing)	+44 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+22.5 dBm
Noise Figure	5 dB
Device / Supply Voltage	+5 V
Quiescent Current	250 mA

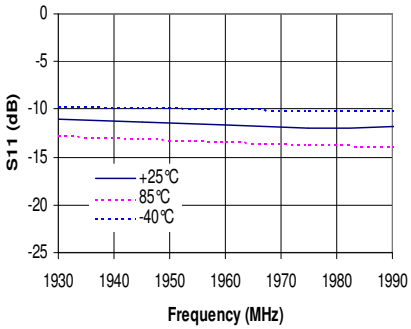


C8 is placed at silkscreen marker 'A' or center of component placed at 1.8 deg. @ 1960 MHz away from pin 3. C9 is placed at the silkscreen marker '4' or center of component placed at 20 deg. @1960 MHz away from pin 6.

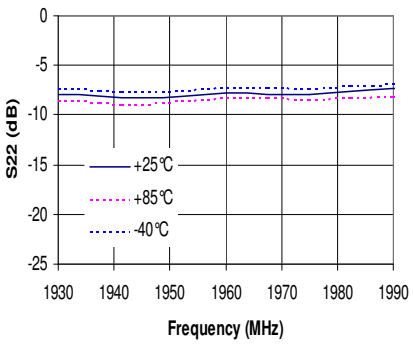
S21 vs. Frequency



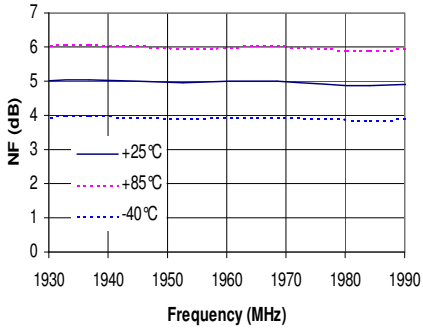
S11 vs. Freqency



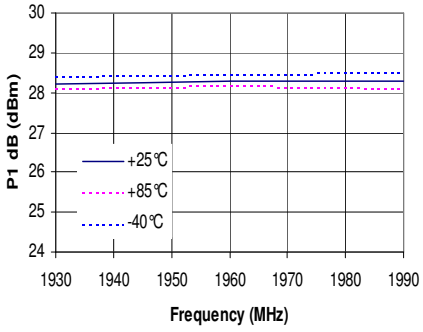
S22 vs. Frequency



Noise Figure vs. Frequency

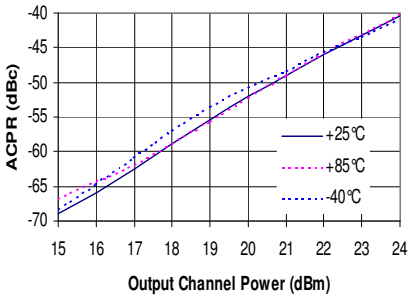


P1 dB vs. Frequency



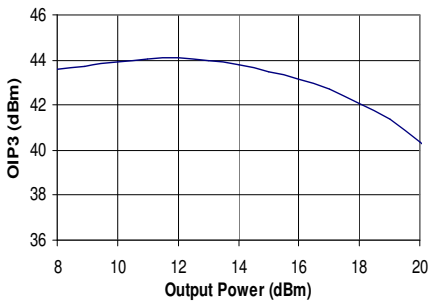
ACPR vs. Channel Power

IS-95, 9 ch,Fwd, ±885 KHz offset, 30 KHz Meas BW, 1960 MHz



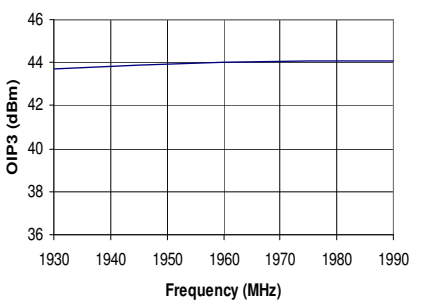
OIP3 vs. Output Power

freq=1960, 1961 MHz,+ 25℃



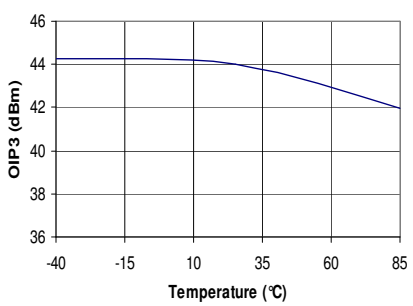
OIP3 vs. Frequency

+25℃, +11 dBm / tone



OIP3 vs. Temperature

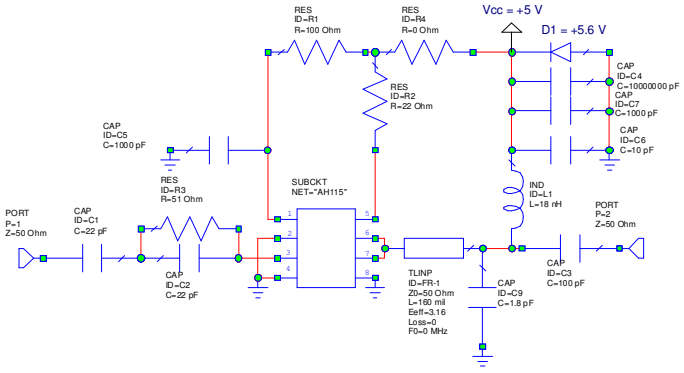
freq=1960,1961 MHz, +11 dBm / tone



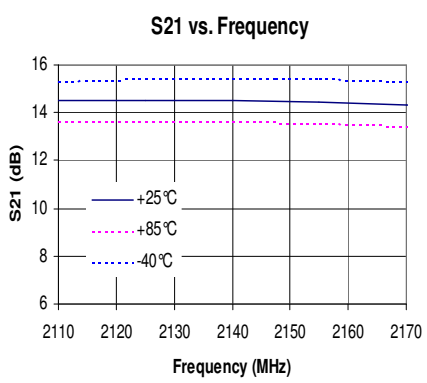
2140 MHz Application Circuit (AH115-S8PCB2140)

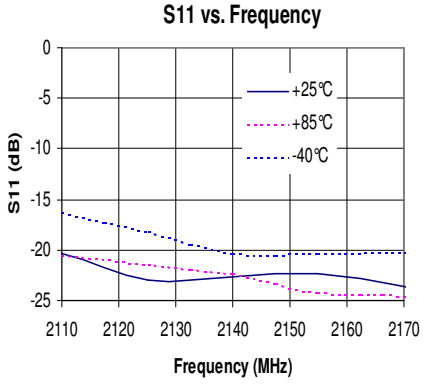
Typical RF Performance at 25°C

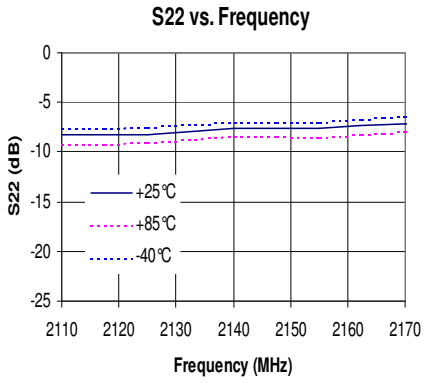
Frequency	2140 MHz
S21 – Gain	14.4 dB
S11 – Input Return Loss	-23 dB
S22 – Output Return Loss	-8 dB
Output P1dB	+28.5 dBm
Output IP3 (+11 dBm / tone, 1 MHz spacing)	+42 dBm
W-CDMA Channel Power (@-45 dBc ACLR)	+20 dBm
Noise Figure	5.3 dB
Device / Supply Voltage	+5 V
Quiescent Current	250 mA

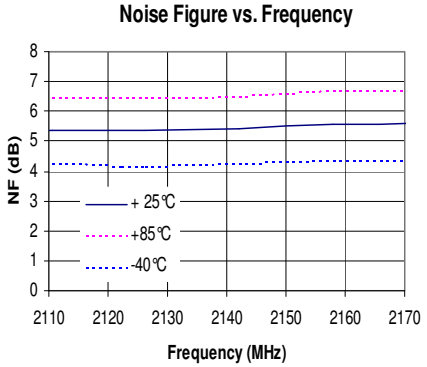


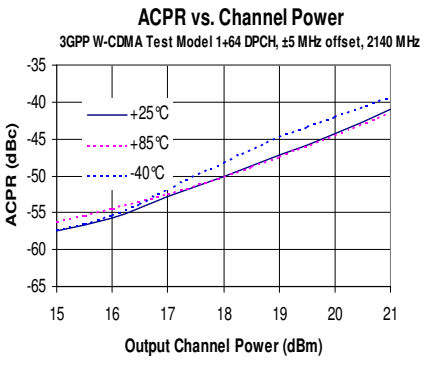
C9 is placed at the silkscreen marker '3' or center of component placed at 13 deg. @2140 MHz away from pin 6.

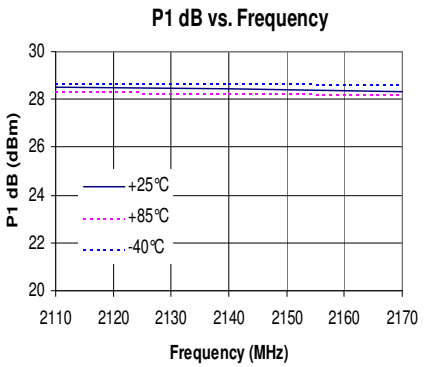


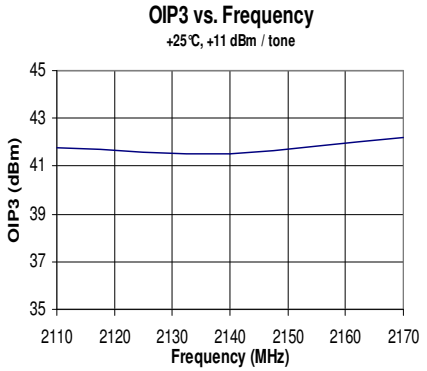


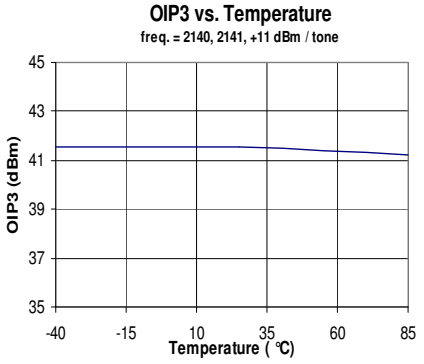


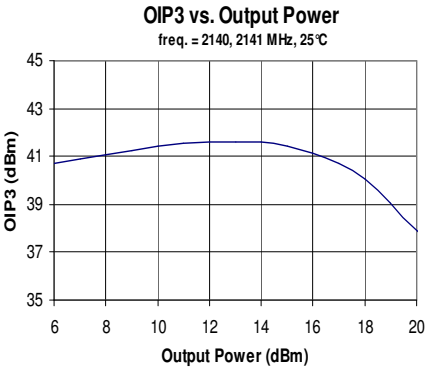










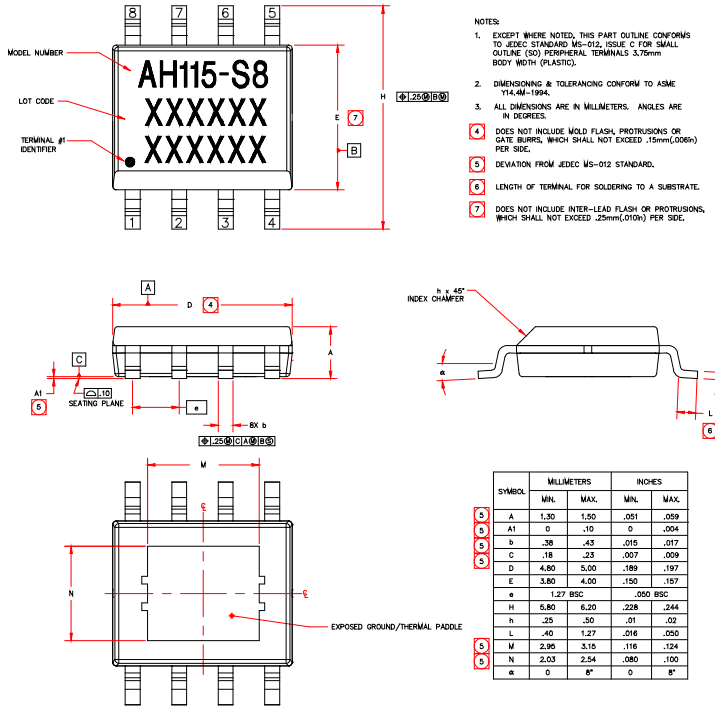


Specifications and information are subject to change without notice

AH115-S8 (SOIC-8 Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing

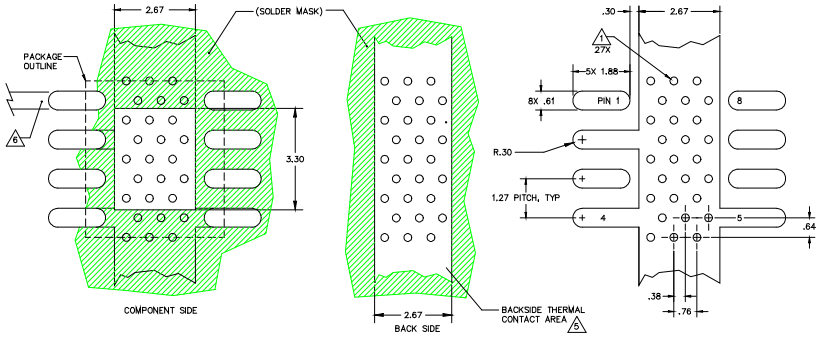


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.30	1.50	.051	.059
A1	0	.10	0	.004
b	.38	.43	.015	.017
C	.18	.23	.007	.009
D	4.80	5.00	.189	.197
E	3.80	4.00	.150	.157
e	1.27 BSC		.050 BSC	
H	5.80	6.20	.228	.244
h	.25	.50	.01	.02
L	.40	1.27	.016	.050
M	2.95	3.15	.116	.124
N	2.03	2.54	.080	.100
α	0	8°	0	8°

Land Pattern



Product Marking

The component will be marked with an "AH115-S8" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ⩾ 500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 3 at +235° C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

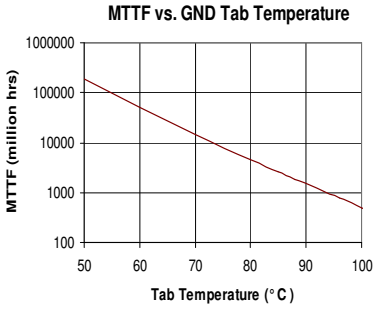
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance (1), Rth	62° C / W
Junction Temperature (2), Tjc	162° C

Notes:

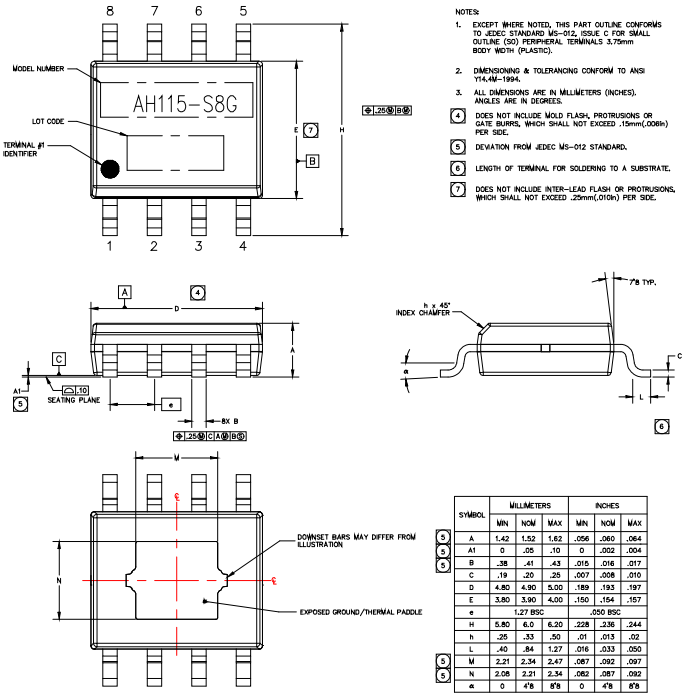
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to the typical biasing condition of +5V, 250 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



AH115-S8G (Green / Lead-free SOIC-8 Package) Mechanical Information

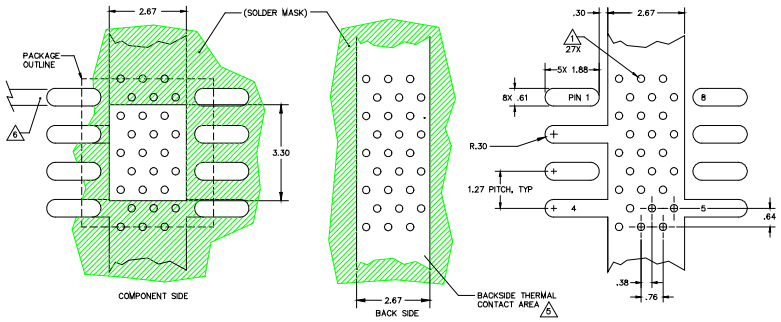
This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

Outline Drawing



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°8	8°8	0	4°8	8°8

Land Pattern



Product Marking

The component will be marked with an "AH115-S8G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ≥ 500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 2 at +260° C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

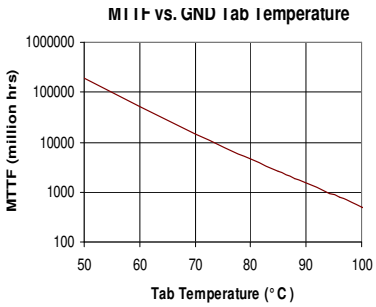
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance (1), Rth	62° C / W
Junction Temperature (2), Tjc	162° C

Notes:

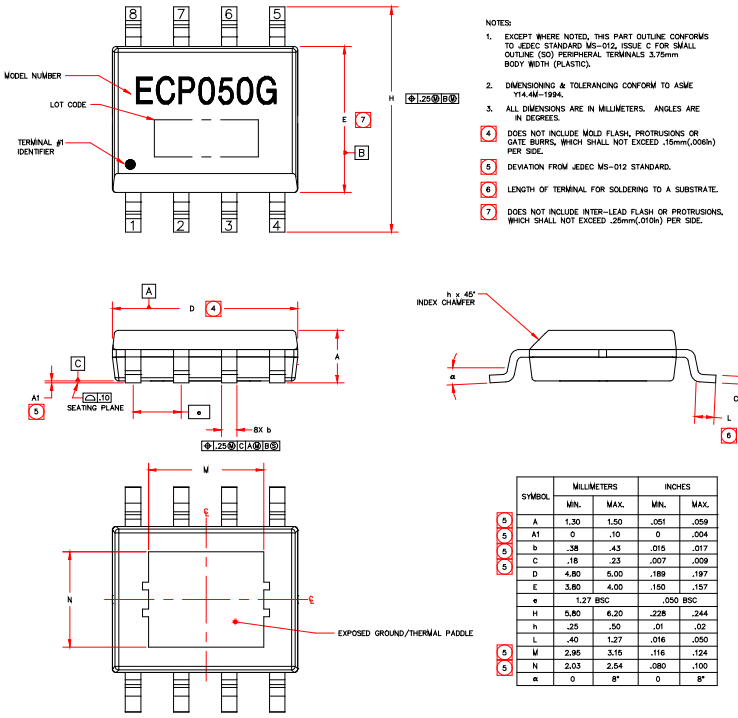
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to the typical biasing condition of +5V, 250 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



ECP050G (SOIC-8 Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

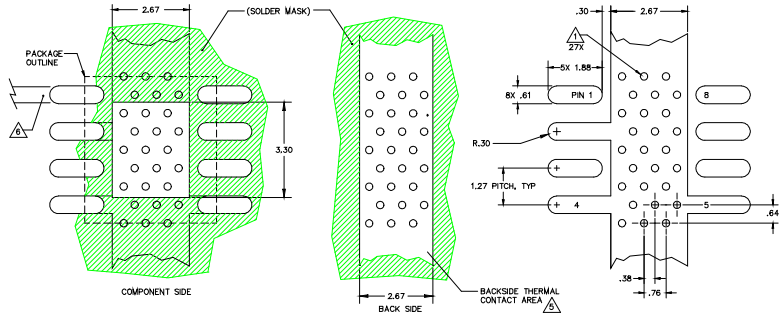
Outline Drawing



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.30	1.50	.051	.059
A1	0	.10	0	.004
b	.38	.43	.015	.017
c	.18	.23	.007	.009
D	4.80	5.00	.189	.197
E	3.80	4.00	.150	.157
e	1.27 BSC		.050 BSC	
H	5.80	6.20	.228	.244
h	.25	.50	.01	.02
L	.40	1.27	.016	.050
M	2.95	3.15	.116	.124
N	2.03	2.54	.080	.100
α	0	8°	0	8°

Land Pattern



Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance, Rth (1)	62° C / W
Junction Temperature, Tjc (2)	162° C

Notes:
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85 °C. Tjc is a function of the voltage at pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
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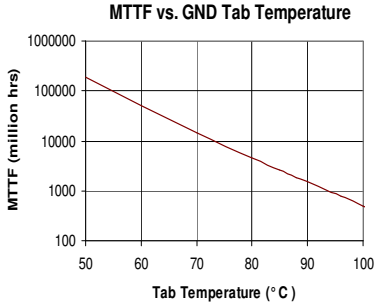

Product Marking

The component will be marked with an "ECP050G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes between 500 and 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 3 at +235° C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

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2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
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