



**Synchronous DRAM Module 64Mbyte(16Mx32-Bit), 100pin DIMM,  
4Banks, 8K Ref., 3.3V**

**Part No. HSD16M32D4**

## GENERAL DESCRIPTION

The HSD16M32D4 is a 16M x 32 bit Synchronous Dynamic RAM high density memory module. The module consists of four CMOS 2M x 16 bit x 4banks Synchronous DRAMs in TSOP-II 400mil packages on a 100-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD16M32D4 is a DIMM( Dual in line Memory Module) and is intended for mounting into 100-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTTL-compatible.

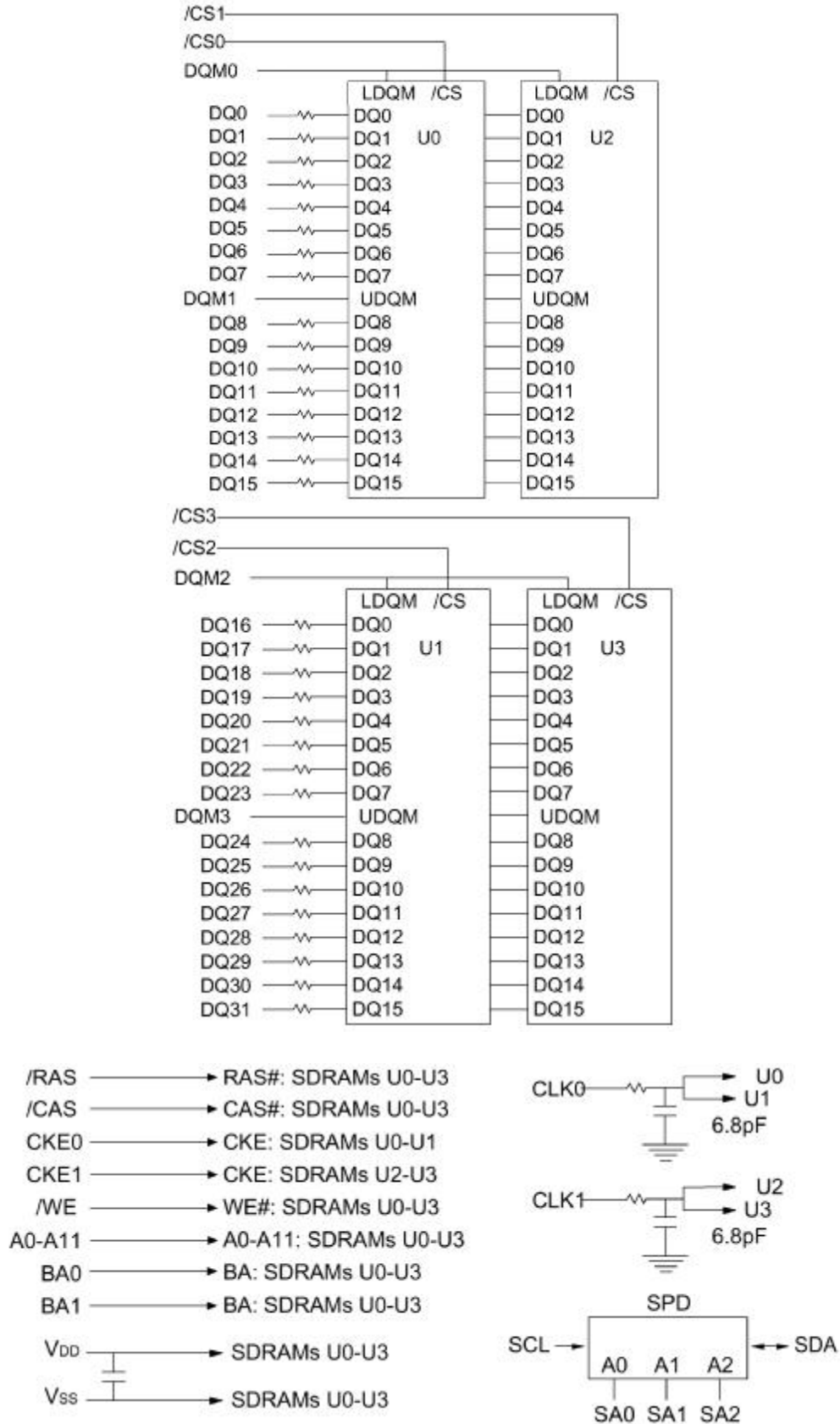
## FEATURES

- Part Identification
  - HSD16M32D4-10 : 100MHz (CL=2)
  - HSD16M32D4-10L : 100MHz (CL=3)
  - HSD16M32D4-12 : 125MHz (CL=3)
  - HSD16M32D4-13 : 133MHz (CL=3)
- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V  $\pm 0.3V$  power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- The used device is 4M x 16bit x 4Banks SDRAM

## PIN ASSIGNMENT

PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	26	VSS	51	VSS	76	VSS
2	DQ0	27	CKE0	52	DQ8	77	CKE1
3	DQ1	28	/WE	53	DQ9	78	NC
4	DQ2	29	/CS0	54	DQ10	79	/CS1
5	DQ3	30	/CS2	55	DQ11	80	/CS3
6	Vcc	31	VCC	56	VCC	81	VCC
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQM0	36	VSS	61	DQM1	86	VSS
12	Vss	37	DQM2	62	VSS	87	DQM3
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VCC	67	A9	92	VCC
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VCC	46	DQ23	71	VCC	96	DQ31
22	NC	47	VSS	72	/RAS	97	VSS
23	NC	48	SDA	73	/CAS	98	SA0
24	NC	49	SCL	74	NC	99	SA1
25	CLK0	50	VCC	75	CLK1	100	SA2

FUNCTIONAL BLOCK DIAGRAM



**PIN FUNCTION DESCRIPTION**

PIN	NAME	INPUT FUNCTION
CLK	System clock	Active on the positive going edge to sample all inputs.
/CS 0~3	Chip enable	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 3	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~DQ 32	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN\_OUT}$	-1V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 4.6V
Power Dissipation	$P_D$	4W
Storage Temperature	$T_{STG}$	-55°C to 150°C
Short Circuit Output Current	$I_{OS}$	400mA

**Notes:**

Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70°C))

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	V <sub>CC</sub> +0.3	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output High Voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output Low Voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-12	-	12	uA	3

### Notes :

- V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
- V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
- Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

(VCC = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock	C <sub>CLK</sub>	20	32	pF
/RAS, /CAS, /WE, /CS, CKE, DQM	C <sub>IN</sub>	20	40	pF
Address	C <sub>ADD</sub>	20	40	pF
DQ (DQ0 ~ DQ63)	C <sub>OUT</sub>	32	52	pF

## DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	VERSION				UNIT	NOTE
			-13	-12	-10	-10L		
Operating current (One bank active)	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC</sub> (min) I <sub>O</sub> = 0mA	600	600	560	560	mA	1
Precharge standby current in power-down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL</sub> (max) t <sub>CC</sub> =10ns	8				mA	
	I <sub>CC2PS</sub>	CKE & CLK ≤ V <sub>IL</sub> (max) t <sub>CC</sub> =∞	8				mA	
Precharge standby current in non power-down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH</sub> (min) CS* ≥ V <sub>IH</sub> (min), t <sub>CC</sub> =10ns Input signals are changed one time during 20ns	64				mA	

	$I_{CC2NS}$	$CKE \geq V_{IH(min)}$ $CLK \leq V_{IL(max)}, t_{CC}=\infty$ Input signals are stable	56					
Active standby current in power-down mode	$I_{CC3P}$	$CKE \leq V_{IL(max)}, t_{CC}=10ns$	24				mA	
	$I_{CC3PS}$	$CKE\&CLK \leq V_{IL(max)}$ $t_{CC}=\infty$	24					
Active standby current in non power-down mode (One bank active)	$I_{CC3N}$	$CKE \geq V_{IH(min)}$ , $CS^* \geq V_{IH(min)}, t_{CC}=10ns$ Input signals are changed one time during 20ns	240				mA	
	$I_{CC3NS}$	$CKE \geq V_{IH(min)}$ $CLK \leq V_{IL(max)}, t_{CC}=\infty$ Input signals are stable	140					
Operating current (Burst mode)	$I_{CC4}$	$I_O = 0$ mA Page burst 4Banks Activated $t_{CCD} = 2CLKs$	720	720	560	560	mA	1
Refresh current	$I_{CC5}$	$t_{RC} \geq t_{RC(min)}$	840	840	800	800	mA	2
Self refresh current	$I_{CC6}$	$CKE \leq 0.2V$	20				mA	
			8				mA	

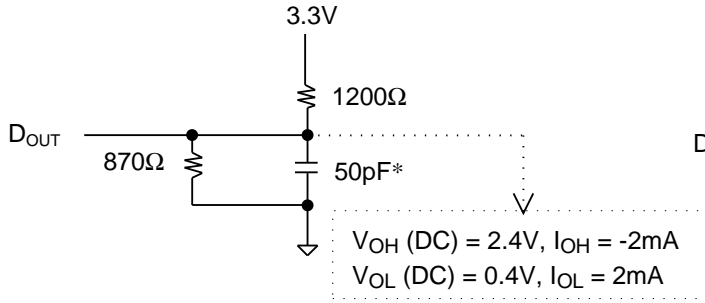
**Notes :**

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS( $V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$ ).

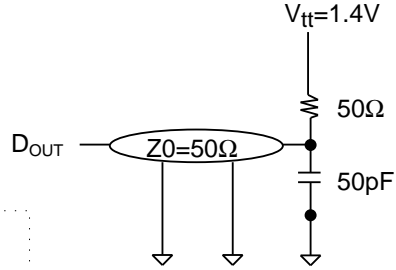
**AC OPERATING TEST CONDITIONS**

( $V_{CC} = 3.3V \pm 0.3V, TA = 0$  to  $70^{\circ}C$ )

PARAMETER	Value	UNIT
AC Input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	Ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

PARAMETER	SYMBOL	VERSION				UNIT	NOTE
		-13	-12	-10	-10L		
Row active to row active delay	$t_{RRD}(\min)$	15	16	20	20	ns	1
RAS to CAS delay	$t_{RP}(\min)$	20	20	20	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	20	20	20	ns	1
Row active time	$t_{RAS}(\min)$	45	48	50	50	ns	1
	$t_{RAS}(\max)$	100				ns	
Row cycle time	$t_{RC}(\min)$	65	68	70	70	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2				CLK	2.5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns					
Last data in to new col. address delay	$t_{CDL}(\min)$	1				CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1				CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1				CLK	3
Number of valid output data	CAS latency=3	2				ea	4
	CAS latency=2	-		1			

**Notes :**

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

## AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-13		-12		-10		-10L		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency=3	$t_{CC}$	7.5		8		10		10		ns	1
	CAS latency=2		-	1000	-	1000	10	1000	12	1000		
CLK to valid output delay	CAS latency=3	$t_{SAC}$		5.4		6		6		6	ns	1,2
	CAS latency=2			-		-		6		7		
Output data hold time	CAS latency=3	$t_{OH}$	2.7		3		3		3		ns	2
	CAS latency=2			-		-		3		3		
CLK high pulse width		$t_{CH}$	2.5		3		3		3		ns	3
CLK low pulse width		$t_{CL}$	2.5		3		3		3		ns	3
Input setup time		$t_{SS}$	1.5		2		2		2		ns	3
Input hold time		$t_{SH}$	0.8		1		1		1		ns	3
CLK to output in Low-Z		$t_{SLZ}$	1		1		1		1		ns	3
CLK to output in Hi-Z	CAS latency=3	$t_{SHZ}$		5.4		6		6		6	ns	2
	CAS latency=2			-		-		6		7	ns	

**Notes :**

- Parameters depend on programmed CAS latency.
- If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
- Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, ie.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.



**SIMPLIFIED TRUTH TABLE**

COMMAND		CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DQM	BA 0,1	A10/AP	A11 A9~A0	NOTE					
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2					
Refresh	Auto refresh	H	H	L	L	L	H	X	X	X	X	3					
	Self refresh		Entry										L	L	H	H	H
		Exit	L	H	L	H	H	X	X	3							
			H		X						X	X	3				
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address							
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A8)	4					
	Auto precharge disable									H		4,5					
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column Address (A0 ~ A8)	4					
	Auto precharge disable									H		4,5					
Burst Stop		H	X	L	L	H	L	X	X			6					
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X						
	All banks								X	H							
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X	X	X						
				L	V	V	V										
Precharge power down mode	Entry	H	L	H	X	X	X	X	X	X	X						
				L	H	H	H										
	Exit	L	H	H	X	X	X	X	X	X	X						
				L	V	V	V										
DQM		H	X					V	X		7						
No operation command		H	X	H	X	X	X	X	X	X	X						
				L	H	H	H										

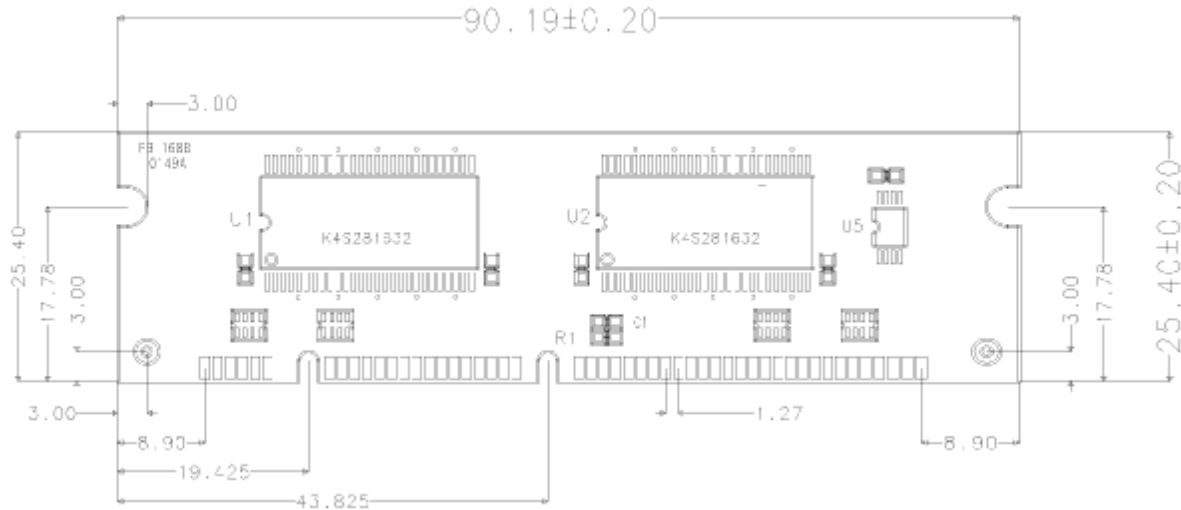
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :**

- OP Code : Operand code  
A0 ~ A12& BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.  
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.  
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.  
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

**PACKAGING INFORMATION**

Unit : mm



Tolerances : ± 0.20 mm

PCB Thickness: 1.27mm ± 0.10mm

**ORDERING INFORMATION**

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX. frq
HSD16M32D4-10	64MByte	16M x 32	100 Pin-DIMM	8K	3.3V	SDRAM	CL2 100MHz
HSD16M32D4-10L	64MByte	16M x 32	100 Pin	8K	3.3V	SDRAM	CL3 100MHz
HSD16M32D4-12	64MByte	16M x 32	100 Pin	8K	3.3V	SDRAM	CL3 125MHz
HSD16M32D4-13	64MByte	16M x 32	100 Pin	8K	3.3V	SDRAM	CL 3 133MHz