

HIGH SPEED 2K X 16 DUAL-PORT SRAM

IDT7133SA/LA IDT7143SA/LA

Features

- High-speed access
 - Military: 25/35/45/55/70/90ns (max.)
 - Industrial: 25/35/55ns (max.)
 - Commercial: 20/25/35/45/55/70/90ns (max.)
- Low-power operation
 - IDT7133/43SA

Active: 1150mW (typ.)

Standby: 5mW (typ.)

IDT7133/43LA

Active: 1050mW (tvp.)

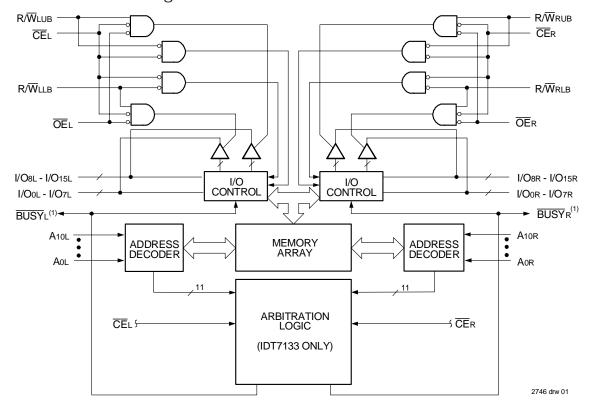
- Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)

- ◆ BUSY output flag on IDT7133; BUSY input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- ◆ TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic PGA, Flatpack, PLCC and 100-
- Military product compliant to MIL-PRF-38535 QML
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Description

The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port

Functional Block Diagram



NOTF:

1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor. IDT7143 (SLAVE): BUSY is input.

OCTOBER 2008

DSC 2746/13 ©2008 Integrated Device Technology, Inc.

RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

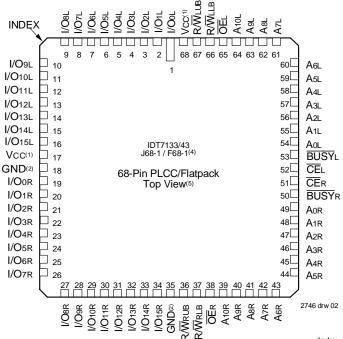
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each

port to enter a very low standby power mode.

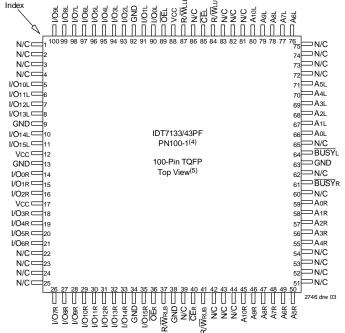
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 1,150mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming $200\mu W$ for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, 68-pin PLCC and 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations(1,2,3)



- Both Vcc pins must be connected to the power supply to ensure reliable operation.
- Both GND pins must be connected to the ground supply to ensure reliable operation
- J68-Package body is approximately 0.95 in x 0.95 in x 0.17 in. F68-Package body is approximately 1.18 in x 1.18 in x 0.16 in. PN100-Package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking.



Pin Configurations^(1,2,3) (con't.)

11		51 A6L	50 A5L	48 A3L	46 A1L	44 BUSYL	42 CE R	40 Aor	38 A2R	36 A4R	
11		A6L	A5L	A3L	A1L	DUSTL	CER	AUR	A2R	A4R	
	53	52	49	47	45	43	41	39	37	35	34
10	A8L	A7L	A4L	A2L	Aol	CEL	BUSYR	A1R	АзR	A5R	A6R
	55	54								32	33
09	A10L	A9L								A8R	A7R
	57	56								30	31
80	R/WLLB	ŌĒL								A10R	A9R
	59	58								28	29
07	Vcc ⁽¹⁾	R/WLUB			וחו	Γ7133/4	13G			R/WRLB	OE R
	61	60				SU68-1				26	27
06	I/O1L	I/Ool				GND(2)	R/WRUB				
	63	62			To	op Viev	y (5)			24	25
05	I/O3L	I/O ₂ L								I/O14R	I/O15R
	65	64								22	23
04	I/O5L	I/O4L								I/O12R	I/O13R
	67	66								20	21
03	I/O7L	I/O6L								I/O10R	I/O11R
	68	1	3	5	7	9	11	13	15	18	19
02	I/O ₈ L	I/O ₉ L	I/O11L	I/O13L	I/O15L	GND ⁽²⁾	I/O1R	I/O3R	I/O ₅ R	I/O8R	I/O9R
		2	4	6	8	10	12	14	16	17	
01	/•	I/O10L	I/O12L	I/O14L	Vcc ⁽¹⁾	I/O ₀ R	I/O ₂ R	I/O4R	I/O6R	I/O7R	
Pin 1/ Designate	or A	В	С	D	E	F	G	Н	J	К	L

NOTES:

- 1. Both Vcc pins must be connected to the power supply to ensure reliable operation.
- 2. Both GND pins must be connected to the ground supply to ensure reliable operation.
- 3. Package body is approximately 1.18 in x 1.18 in x 0.16 in.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names			
CEL	ՇĒ R	Chip Enable			
R/WLUB	R/WRUB	Upper Byte Read/Write Enable			
R/WLLB	R/WRLB	Lower Byte Read/Write Enable			
ŌĒL	OE R	Output Enable			
A0L - A10L	AOR - A10R	Address			
I/O0L - I/O15L	VO0R - I/O15R	Data Input/Output			
BUSYL	BUSYR	Busy Flag			
V	СС	Power			
G	ND	Ground			

2746 drw 04

2746 tbl 01

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
Tstg	Storage Temperature	-65 to +150	-65 to +150	°C
PT ⁽³⁾	Power Dissipation	2.0	2.0	W
ЮИТ	DC Output Current	50	50	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may
 cause permanent damage to the device. This is a stress rating only and functional
 operation of the device at these or any other conditions above those indicated in
 the operational sections of this specification is not implied. Exposure to absolute
 maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

Capacitance (TA = +25°C, f = 1.0mhz)

Symbol	Parameter ⁽¹⁾	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	11	pF
Соит	Output Capacitance	Vout = 3dV	11	pF

NOTES

- 1. This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage^(1,2)

		- - · <i>J</i>	
Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES:

2746 tbl 02

2746 tbl 04

1. This is the parameter Ta. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
Vн	Input High Voltage	2.2	_	6.0(2)	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾		0.8	V

2746 tbl 05

NOTES:

- 1. VIL (min.) = -1.5V for pulse width less than 10ns.
- VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Either port, $Vcc = 5.0V \pm 10\%$)

2746 tbl 03

			7133SA 7143SA		713 714		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
lu	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, ViN = 0V to Vcc	-	10	-	5	μΑ
ILO	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0V$ to V_{CC}	-	10	-	5	μΑ
Vol	Output Low Voltage (VOo-VO15)	IoL = 4mA		0.4	_	0.4	V
Vol	Open Drain Output Low Voltage (BUSY)	IOL = 16mA		0.5	_	0.5	V
Voh	Output High Voltage	IOH = -4mA	2.4	_	2.4	_	V

NOTE:

1. At Vcc ≤ 2.0V, input leakages are undefined.

2746 tbl 06

DC Electrical Characteristics Operating Temperature and Supply Voltage Range ($^{(2)}$) (Vcc = 5.0V \pm 10%)

			7133X20 7143X20 Com'l Only		X20	7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military			
Symbol	Parameter	Test Condition	Versio	n	Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	Unit
Icc	Dynamic Operating Current (Roth Ports Active)	$\overline{CE} = VIL$, Outputs Disabled $f = MAX^{(2)}$	COM'L	S L	250 230	310 280	250 230	300 270	240 210	295 250	mA
	(Both Ports Active)	I = MAX*	MIL & IND	S L			250 230	330 300	240 220	325 295	
ISB1	Standby Current (Both Ports - TTL	CEL and CER = VIH	COM'L	S L	25 25	80 70	25 25	80 70	25 25	70 60	mA
	Level Inputs)	$f = f_{MAX}^{(3)}$	MIL & IND	S L		11	25 25	90 80	25 25	75 65	
ISB2	Standby Current (One Port - TTL	CE'A" = VL and CE"B" = VH ⁽⁴⁾ f=fMAX ⁽³⁾	COM'L	S L	140 120	200 180	140 100	200 170	120 100	180 160	mA
	Level Inputs)	Active Port Outputs disabled	COM'L S 250 310 250 300 240 295 100 250								
ISB3	Full Standby Current (Both Ports -	Both Ports CEL and CER > Vcc - 0.2V	COM'L	S L							mA
	CMOS Level Inputs)	$VIN > VCC - 0.2V$ or $VIN < 0.2V$, $f = 0^{(4)}$		S L	_						
ISB4	(One Port -	<u>CE</u> 'A" < 0.2V and <u>CE</u> 'B" > Vcc - 0.2V ⁽⁵⁾	COM'L	S L							mA
	CMOS Level Inputs)	$ \begin{array}{l} \text{Vin} > \text{Vcc - 0.2V or Vin} < 0.2\text{V} \\ \text{Active Port Outputs Disabled} \\ \text{f} = \text{IMAX}^{(S)} \\ \end{array} $		S L		_					

2746 tbl 07a

			7133X45 7143X45 Com'l & Military		X45 'I &	7133 7143 Com'l & Mili	X55 , Ind	7133X70/90 7143X70/90 Com'l & Military			
Symbol	Parameter	Test Condition	Versio	on	Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Мах.	Typ. ⁽¹⁾	Max.	Unit
Icc	Current	$\overline{CE} = VIL$, Outputs Disabled $f = IMAX^{(2)}$	COM'L	S L	230 210	290 250	230 210	285 250	230 210	280 250	mA
	(Both Ports Active)	I = IMAX ^{ey}	MIL & IND	S L	230 210	320 290	230 210	315 285	230 210	310 280	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	\overline{CEL} and $\overline{CER} = VIH$ $f = f(AXX^G)$	COM'L	S L	25 25	75 65	25 25	70 60	25 25	70 60	mA
	Lever inputs)	I = IMAX*	MIL & IND	S L	25 25	80 70	25 25	80 70	25 25	75 65	
ISB2	(One Port - TTL f=fMA	CE'A" = VIL and CE'B" = VIH ⁽⁴⁾	COM'L	S L	120 100	190 170	120 100	180 160	120 100	180 160	mA
	Level Inputs)	Active Port Outputs Disabled	MIL & IND	S L	120 100	210 190	120 100	210 190	120 100	200 180	
ISB3	Full Standby Current (Both Ports -	Both Ports CEL and CER > VCC - 0.2V	COM'L	S L	1.0 0.2	15 4	1.0 0.2	15 4	1.0 0.2	15 4	mA
CMOS Level Inputs) VIN > VCC - 0.2V or VIN < 0.2V, f = 0 ⁽⁴⁾ MIL & S 1.0 30 1.0 IND L 0.2 10 0.2	1.0 0.2	30 10	1.0 0.2	30 10							
ISB4	(One Port - CE CMOS Level Inputs) VIII Ac	<u>CE</u> 'A" < 0.2V and <u>CE</u> 'B" > VCC - 0.2V ⁽⁶⁾	COM'L	S L	120 100	180 160	120 100	170 150	120 100	170 150	mA
		Vin > Vcc - 0.2V or Vin < 0.2V Active Port Outputs Disabled f = fimax ^(S)	MIL & IND	S L	120 100	200 180	120 100	200 180	120 100	190 170	

NOTES

2746 tbl 07b

- 1. Vcc = 5V, $TA = +25^{\circ}C$ for Typ., and are not production tested. Iccdc = 180mA (typ.)
- 2. 'X' in part number indicates power rating (SA or LA)
- 3. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ trc, and using "AC Test Conditions" of input levels of GND to 3V.
- 4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- 5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2746 tbl 08

Data Retention Characteristics

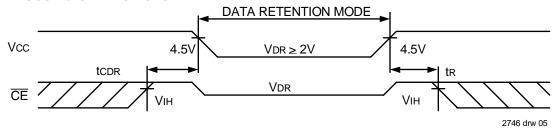
(LA Version Only) VLC = 0.2V, VHC = VCC - 0.2V

				7			
Symbol	Parameter	Test Cond	ition	Min.	Typ. ⁽¹⁾	Max.	Unit
V DR	Vcc for Data Retention	Vcc = 2V		2.0	-	_	V
ICCDR	Data Retention Current	CE ≥ VHC	MIL. & IND.	_	100	4000	μA
		VIN > VHC Or < VLC	COM'L.	_	100	1500	
tcdr ⁽³⁾	Chip Deselect to Data Retention Time			0	-	1	V
tR ⁽³⁾	Operation Recovery Time			trc ⁽²⁾	_		V

NOTES:

- 1. Vcc = 2V, TA = +25°C, and are not production tested.
- 2. trc = Read Cycle Time
- 3. This parameter is guaranteed by device characterization but is not production tested.

Data Retention Waveform



AC Test Conditions

70 rest conditions								
Input Pulse Levels	GND to 3.0V							
Input Rise/Fall Times	5ns Max.							
Input Timing Reference Levels	1.5V							
Output Reference Levels	1.5V							
Output Load	Figures 1, 2 and 3							

2746 tbl 09

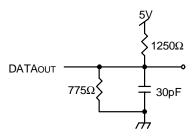


Figure 1. AC Output Test Load

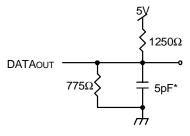


Figure 2. Output Load (for tLz, tHz, twz, tow) *Including scope and jig

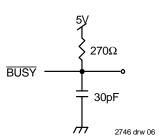


Figure 3. BUSY Output Load (IDT7133 only)

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽³⁾

		714	3X20 3X20 I Only	714: Com	3X25 3X25 'I, Ind litary	7133X35 7143X35 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
trc	Read Cycle Time	20	_	25	_	35	_	ns
taa	Address Access Time	_	20		25	_	35	ns
tace	Chip Enable Access Time		20		25		35	ns
taoe	Output Enable Access Time		12	_	15		20	ns
tон	Output Hold from Address Change	0	_	0	_	0	_	ns
t LZ	Output Low-Z Time ^(1,2)	0	_	0	-	0	_	ns
tHZ	Output High-Z Time ^(1,2)	_	12		15	_	20	ns
tpu	Chip Enable to Power Up Time (2)	0	_	0	_	0	_	ns
tpD	Chip Disable to Power Down Time (2)		20		50		50	ns

2746 tbl 10a

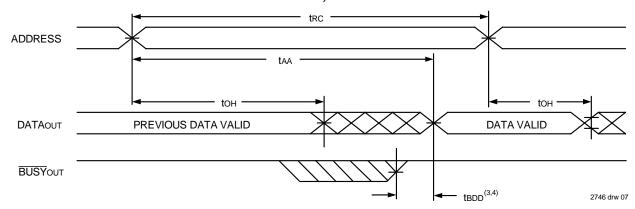
		714 Cor	3X45 3X45 n'l & itary	714: Com	3X55 3X55 'I, Ind litary	7133X70/90 7143X70/90 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE	•							
trc	Read Cycle Time	45	_	55	_	70/90	_	ns
taa	Address Access Time	_	45	_	55	_	70/90	ns
tace	Chip Enable Access Time	_	45	_	55		70/90	ns
taoe	Output Enable Access Time	_	25	_	30	_	40/40	ns
tон	Output Hold from Address Change	0	_	0	_	0/0	_	ns
tLZ	Output Low-Z Time ^(1,2)	0	_	5	_	5/5		ns
tHZ	Output High-Z Time ^(1,2)	_	20	_	20	_	25/25	ns
tpu	Chip Enable to Power Up Time (2)	0	_	0	_	0/0	_	ns
tpd	Chip Disable to Power Down Time (2)		50		50		50/50	ns

NOTES:

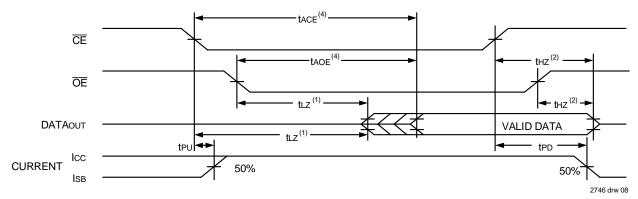
2746 tbl 10b

- 1. Transition is measured 0mV fromLow or High-impedance voltage with load (Figure 2).
- This parameter is guaranteed by device characterization, but is not production tested.
 'X' in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE⁽⁵⁾



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(5)



- Timing depends on which signal is asserted last, OE or CE.
 Timing depends on which signal is deasserted first, OE or CE.
- 3. tbbb delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, BUSY has no relationship to valid output data.
- 4. Start of valid data depends on which timing becomes effective last, taoe, tace, taa, or tbdd.
- 5. R/W = VIH, and the address is valid prior to or coincidental with \overline{CE} transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

	9 - 1	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time ⁽³⁾	20	_	25	-	35		ns
tew	Chip Enable to End-of-Write	15	_	20	-	25		ns
taw	Address Valid to End-of-Write	15	_	20	_	25		ns
tas	Address Set-up Time	0	_	0	-	0		ns
twp	Write Pulse Width	15	_	20	_	25	-	ns
twr	Write Recovery Time	0	_	0	-	0		ns
tow	Data Valid to End-of-Write	15	_	15	_	20	_	ns
tHZ	Output High-Z Time ^(1,2)	_	12	_	15	_	20	ns
tон	Data Hold Time ⁽⁴⁾	0	_	0	_	0	_	ns
twz	Write Enable to Output in High-Z ^(1,2)		12	_	15		20	ns
tow	Output Active from End-of-Write (1,2,4)	0	_	0		0	_	ns

2746 tbl 11a

		7133X45 7143X45 Com'l & Military		7143 Com'	3X55 3X55 I, Ind litary	7133X70/90 7143X70/90 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time ⁽³⁾	45	-	55	-	70/90	-	ns
tew	Chip Enable to End-of-Write	30	_	40	_	50/50	_	ns
taw	Address Valid to End-of-Write	30	-	40	_	50/50	_	ns
tas	Address Set-up Time	0	_	0	-	0/0	_	ns
twp	Write Pulse Width	30	-	40	_	50/50	_	ns
twr	Write Recovery Time	0	_	0	-	0/0	_	ns
tow	Data Valid to End-of-Write	20	-	25	_	30/30	_	ns
tHZ	Output High-Z Time ^(1,2)	_	20	_	20		25/25	ns
tон	Data Hold Time ⁽⁴⁾		-	5	_	5/5	_	ns
twz	Write Enable to Output in High-Z ^(1,2)	_	20	_	20	_	25/25	ns
tow	Output Active from End-of-Write (1,2,4)	5	_	5	_	5/5	_	ns

NOTES:

2746 tbl 11b

- 1. Transition is measured 0mV from Low or High-impedance voltage from the Output Test Load (Figure 2).
- 2. This parameter is guaranteed by device characterization but not production tested.
- 3. For MASTER/SLAVE combination, two = tbaa + twr + twp, since $R\overline{W}$ = VIL must occur after tbaa.
- 4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tow values will very over voltage and temperature, the actual tDH will always be smaller than the actual tow.
- 5. 'X' in part number indicates power rating (SA or LA).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁶⁾

		7133X20 7143X20 Com'l Only		7143 Com	3X25 3X25 1, Ind litary	7133X35 7143X35 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
BUSY TIMING	(For MASTER 71V33)							
tbaa	BUSY Access Time from Address		20		20	_	30	ns
TBDA	BUSY Disable Time from Address		20	-	20	1	30	ns
TBAC	BUSY Access Time from Chip Enable	I	20		20	1	25	ns
tBDC	BUSY Disable Time from Chip Enable	_	17	_	20	_	25	ns
twdd	Write Pulse to Data Delay ⁽¹⁾	_	40	_	50	_	60	ns
todo	Write Data Valid to Read Data Delay ⁽¹⁾	_	30	_	35	_	45	ns
tBDD	BUSY Disable to Valid Data ⁽²⁾	I	25	_	30	-	35	ns
taps	Arbitration Priority Set-up Time ⁽³⁾	5		5	_	5	_	ns
twн	Write Hold After BUSY ⁽⁵⁾	20		20	_	25	_	ns
BUSY INPUT TIMING (For SLAVE 71V43)								
twB	BUSY Input to Write ⁽⁴⁾	0		0	_	0		ns
twн	Write Hold After BUSY ⁽⁵⁾	20	_	20	_	25	_	ns
twdd	Write Pulse to Data Delay ⁽¹⁾	-	40	_	50	-	60	ns
todd	Write Data Valid to Read Data Delay ⁽¹⁾	_	30	_	35		45	ns

27	746	tbl	12a

		7133X45 7143X45 Com'l & Military		714: Com	3X55 3X55 'I, Ind litary	7133X70/90 7143X70/90 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
BUSY TIMING	(For MASTER 71V33)							
tbaa	BUSY Access Time from Address		40		40	_	45/45	ns
TBDA	BUSY Disable Time from Address		40	-	40	1	45/45	ns
tbac .	BUSY Access Time from Chip Enable	_	30	_	35	_	35/35	ns
tBDC	BUSY Disable Time from Chip Enable		25	_	30	_	30/30	ns
twdd	Write Pulse to Data Delay ⁽¹⁾	_	80	_	80	-	90/90	ns
todo	Write Data Valid to Read Data Delay ⁽¹⁾	_	55	-	55	1	70/70	ns
tBDD	BUSY Disable to Valid Data ⁽²⁾	_	40		40	_	40/40	ns
taps	Arbitration Priority Set-up Time ⁽³⁾	5		5	_	5/5		ns
twн	Write Hold After BUSY ⁽⁵⁾	30		30	_	30/30		ns
BUSY INPUT	TIMING (For SLAVE 71V43)							
twB	BUSY Input to Write ⁽⁴⁾	0	_	0	_	0/0	_	ns
twн	Write Hold After BUSY ⁽⁵⁾	30	_	30	_	30/30	_	ns
twdd	Write Pulse to Data Delay ⁽¹⁾	_	80	_	80	-	90/90	ns
todd	Write Data Valid to Read Data Delay ⁽¹⁾		55	-	55	_	70/70	ns

NOTES:

- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".

 To ensure that the earlier of the two ports wins.

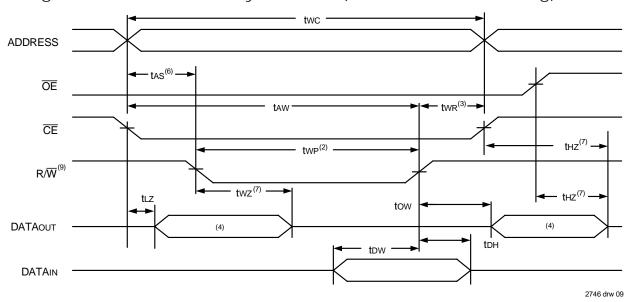
 To ensure that the write cycle is inhibited on port "B" during contention on port "A".

 To ensure that a write cycle is completed on port "B" after contention on port "A".

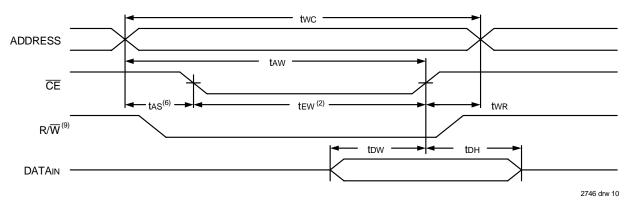
 'X' in part number indicates power rating (SA or LA).

2746 tbl 12b

Timing Waveform of Write Cycle No. 1 (R/W Controlled Timing)(1,5,8)

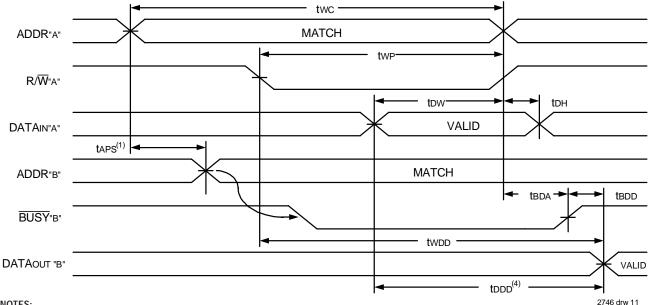


Write Cycle No. 2 (CE Controlled Timing)(1,5)



- 1. R/\overline{W} or \overline{CE} must be HIGH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of a $\overline{\text{CE}}$ = VIL and a R/ $\overline{\text{W}}$ = VIL.
- 3. two is measured from the earlier of $\overline{\text{CE}}$ or R/\overline{W} going HIGH to the end of the write cycle.
- 4. During this period, the I/O pins are in the output state, and input signals must not be applied.
- 5. If the CE LOW transition occurs simultaneously with or after the RW LOW transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal $(\overline{CE} \text{ or } R/\overline{W})$ is asserted last.
- 7. Timing depends on which enable signal is de-asserted first, $\overline{\sf CE}$ or $\overline{\sf OE}$.
- 8. If $\overline{\sf OE}$ is LOW during a R $\overline{\sf NW}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tbw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tbw. If $\overline{\sf OE}$ is HIGH during an R $\overline{\sf NW}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 9. $\dot{R/W}$ for either upper or lower byte.

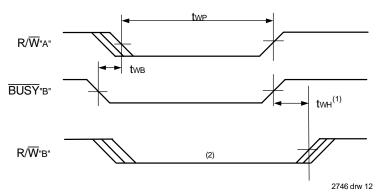
Timing Waveform of Write with Port-to-Port Read and **BUSY**(1,2,3)



NOTES:

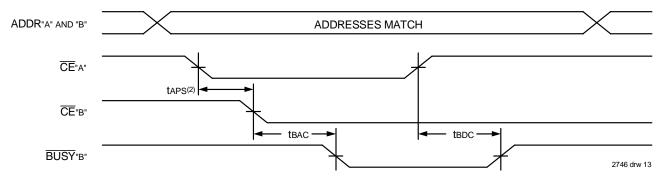
- 1. To ensure that the earlier of the two ports wins, taps is ignored for Slave (IDT7143).
- 2. $\overline{CE}L = \overline{CE}R = VIL$
- 3. $\overline{OE} = V_{IL}$ for the reading port.
- 4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with **BUSY**(3)

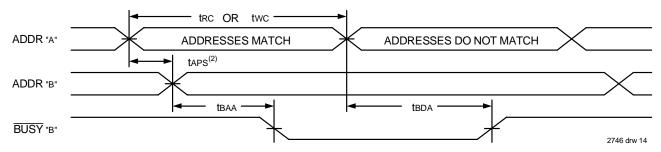


- 1. twn must be met for both BUSY input (IDT7143, slave) and output (IDT7133, master).
- 2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking R/\overline{W} "B", until $\overline{\text{BUSY}}$ "B" goes HIGH.
- 3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Timing Waveform of **BUSY** Arbitration Controlled by **CE** Timing⁽¹⁾



Timing Waveform of **BUSY** Arbitration Controlled by Addresses⁽¹⁾



- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
- 2. If taps is not satisfied, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (IDT7133 only).

Functional Description

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table 1.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the \overline{BUSY} logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. If desired, unintended write operations can be prevented to a port by tying the \overline{BUSY} pin for that port LOW. The \overline{BUSY} outputs on the IDT 7133 RAM are open drain and require pullup resistors.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7133/43 RAM array in width while using $\overline{\text{BUSY}}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{\text{BUSY}}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{\text{BUSY}}$ signal as a write inhibit signal. Thus on the IDT7133 RAM the $\overline{\text{BUSY}}$ pin is an output and on the IDT7143 RAM, the $\overline{\text{BUSY}}$ pin is an input (see Figure 3).

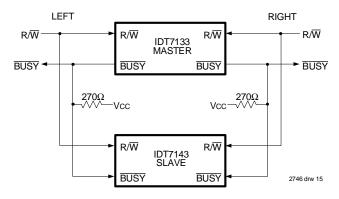


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its BUSYL while another activates its BUSYR signal. Both sides are now BUSY and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{\text{BUSY}}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{\text{BUSY}}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{\text{BUSY}}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{\text{BUSY}}$ from the MASTER.

Truth Table I - Non-Contention Read/Write Control⁽⁴⁾

		LEFT OF	R RIGHT PO	ORT ⁽¹⁾		
R/₩LB	R/Wub	CE	ŌĒ	I/O ₀₋₇	I/O8-15	Function
Х	Х	Н	Х	Z	Z	Port Disabled and in Power Down Mode, ISB2, ISB4
Х	Х	Н	Х	Z	Z	CER = CEL = VIH, Power Down Mode, ISB1 or ISB3
L	L	L	Х	DATAIN	DATAIN	Data on Lower Byte and Upper Byte Written into Memory ⁽²⁾
L	Н	L	L	DATAIN	DATAout	Data on Lower Byte Written into Memory ⁽²⁾ , Data in Memory Output on Upper Byte ⁽³⁾
Н	L	L	L	DATAout	DATAIN	Data in Memory Output on Lower Byte ⁽³⁾ , Data on Upper Byte Written into Memory ⁽²⁾
L	Н	L	Н	DATAIN	Z	Data on Lower Byte Written into Memory ⁽²⁾
Н	L	L	Н	Z	DATAIN	Data on Upper Byte Written into Memory (2)
Н	Н	L	L	DATAout	DATAout	Data in Memory Output on Lower Byte and Upper Byte
Н	Н	L	Н	Z	Z	High Impedance Outputs

NOTES: 2746 tbl 13

- 1. Aol A10L≠A0R A10R
- 2. If $\overline{\text{BUSY}} = \text{LOW}$, data is not written.
- 3. If $\overline{\text{BUSY}} = \text{LOW}$, data may not be valid, see two and too timing.
- 4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High-Impedance, "LB" = Lower Byte, "UB" = Upper Byte

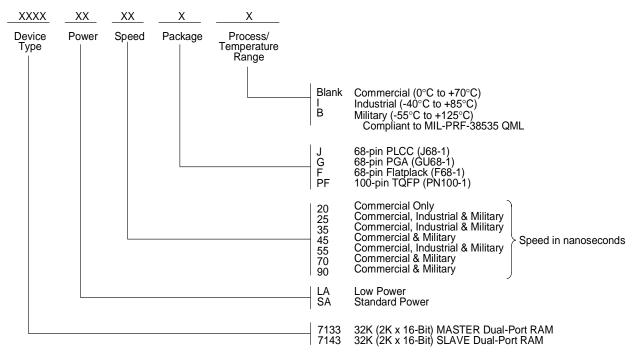
Truth Table II — Address **BUSY** Arbitration

	In	puts	Out	puts	
ΕĒL	CER	Aol-A1ol Aor-A1or	BUSY _L (1)	BUSY _R (1)	Function
Χ	Χ	NO MATCH	Н	Н	Normal
Н	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

2746 tbl 14

- Pins BUSY_L and BUSY_R are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the BUSY input internally inhibits writes.
- "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If taps is not met, either BUSYL or BUSYR = VIL will result BUSYL and BUSYR outputs can not be LOW simultaneously.
- Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

Ordering Information



NOTES: 2746 drw 16

- 1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
- 2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

12/18/98:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
	Page 2	corrected PN100 pinout
02/17/99:		Corrected PF ordering code
030/9/99:		Cosmetic and typographical corrections
06/09/99:		Changed drawing format
10/01/99:		Added Industrial Temperature Ranges and removed corresponding notes
11/10/99:		Replaced IDT logo
04/01/00:		Changed ±500mV to 0mV in notes
	Page 2	Fixed overbar in pinout
06/26/00:	Page 4	Increased storage temperature parameters
		Clarified TA parameter
	Page 5	DC Electrical parameters–changed wording from "open" to "disabled"
01/31/06:	Page 1	Added green availability to features
	Page 16	Added green indicator for ordering information
10/21/08:	Page 16	Removed "IDT" from orderable part number



CORPORATE HEADQUARTERS

6024 Silver Creek Valley Road San Jose, CA 95138

for SALES:

800-345-7015 or 408-284-8200 fax: 408-284-2775

tax: 408-284-2775 www.idt.com for Tech Support: 408-284-2794 DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.