VOICE OTP IC

aP8842 – 42" VOICE OTP

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42 sec VOICE OTP

Features

- 42 Sec Voice Length at 6 KHz
- Combination of voice building blocks extends the duration of playback
- Voice data re-use saves memory space
- Maximum 30 voice groups
- 8 trigger pins, S1 to S8 for the 8 voice groups (group1 ~ 8)
- SBT for sequential playblack the rest of voice groups & for CPU mode trigger
- S1 to S5 in CPU trigger mode to trigger all 30 voice groups
- Holdable, Unholdable, Edge, Level triggering option
- Debounce time : 22ms for both Key and CPU mode @ 6K sampling rate
- IRP interrupt pin for master reset
- 3 programmable Outputs for STP stop pulse, BUSY and LEDs
- Built-in oscillator with a single external resistor to determine the sampling rate
- Built-in D/A converter, EPROM
- ADPCM data compression provides high sound quality
- Optional POP noise elimination function
- C_{OUT} pin drives speaker with a transistor
- V_{OUT1} and V_{OUT2} drives buzzer or speaker directly
- Auto-power down
- 2.7V – 3.8V single power supply operation
- Low standby current (<5uA at 3V)
- Development Tools Support

General Description

***a*P8842** is a high quality voice synthesizer capable of varying playback duration. A proprietary ADPCM algorithm is used. The audio message is stored in a 1M bits on-chip EPROM which can store up to 42 seconds of voice data at 6 KHz sample rate.

The ***a*P8842** eliminates the need of complicated circuitry in voice playback but still achieves high voice quality for different kind of sounds. Combinations in sections achieve longer playback duration.

A pair of PWM output pins, V_{OUT1} and V_{OUT2} provides direct drive to buzzer or speaker.

A current output pin, C_{OUT}, enables the device to drive a speaker through a low cost NPN transistor. No complex filtering or amplifier circuit is needed. An automatic ramp-down function eliminates undesired noise at the end of playback.

Group of sections

The voice memory of the **aP8842** is subdivided into 254 memory blocks. Any combination of playback of these memory blocks will form an individual voice group. A maximum of 30 groups are available with triggering S1 to S5 pins together with the SBT pin in CPU trigger mode. In Key trigger mode, S1 to S8 pins are used to trigger the beginning 8 voice groups. The rest of the voice groups can be triggered one by one sequentially with the SBT pin.

Group Configuration

Data within each group are combinations of different fixed memory blocks of up to 254 blocks. They are the fundamental building blocks for arranging playback without limiting sequencing. This provides flexibility and allows data to be re-used, beneficial for applications with many repeated sounds or words.

An example of group configuration is illustrated below:

Group no.	Section entry
Group 1	Block 1 + Block 2 + Block 3 ……. + Block 109
Group 2	Block 3 + Block 2
Group 3	Block 10 + Block 11 + Block 12
Group 4	Block 10 + Block 10 + Block 5

The entries of blocks for each group is truly random and without limitation. However, there is a limit in the total number of entries for 30 voice groups, which is 896 entries in **aP8842**. It is acceptable to allocate all entries into only one group or distribute out to other groups. It depends on how many groups of messages are required.

Programmable Options

Each groups in **aP8842** can have independent options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable
- Outputs are programmable to LED1, LED2, BUSY and STOP pulse

Options that affect all voice groups are called whole chip options. They are:

- Key trigger mode or CPU trigger mode
- Ramp enable (for Cout drive) or Ramp disable (for Vout drive)

Output Selections

There are three independent output pins OUT1, OUT2 and OUT3, available for four combinations of LED1, LED2, STOP and BUSY signals for each voice group.

Options	OUT1	OUT2	OUT3
1.	LED2	LED1	BUSY
2.	STOP	LED1	LED2
3.	LED1	BUSY	STOP
4.	LED1	BUSY	/BUSY

LED1 and LED2 are complemented outputs flashing at a fix interval. STOP pulse gives a long enough positive pulse at the end of the playback for each group with option to enable or disable it.

BUSY is active high during voice playback.

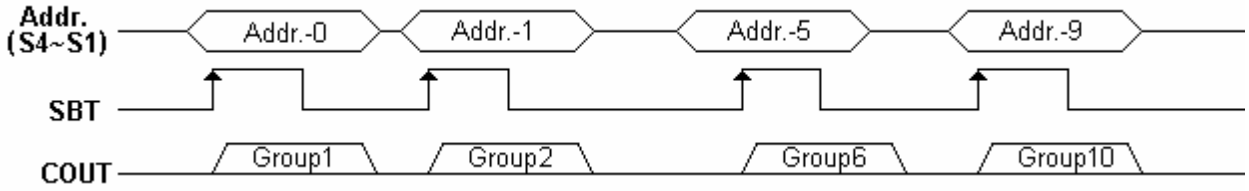
Software Support

All those Options and Output selections can be set with a dedicated OTP compiler and programmer software supplied by APLUS.

Key trigger mode and CPU trigger mode

In Key trigger mode, S1 to S8 will trigger eight voice groups. The rest of the voice groups can only be triggered by SBT sequential trigger pin.

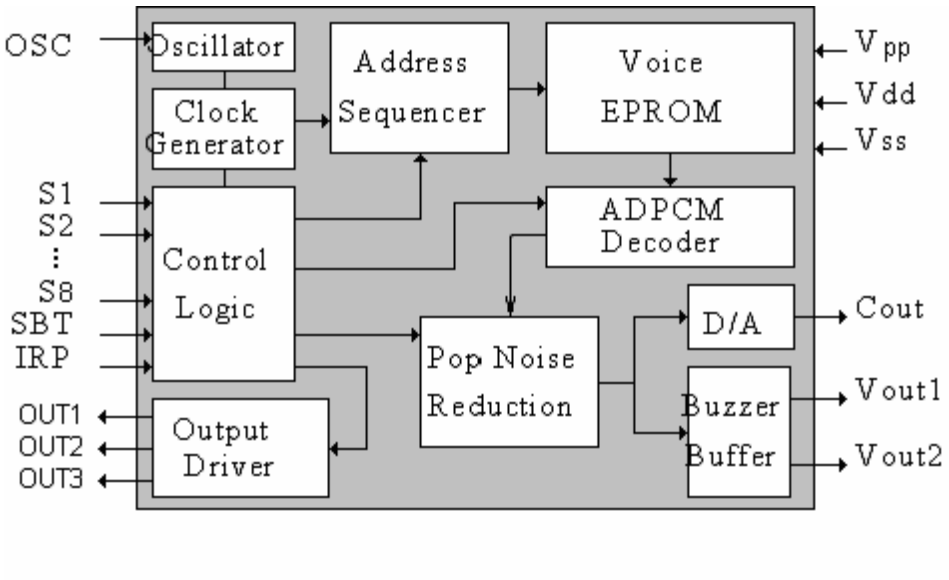
In CPU trigger mode, binary data is input through S5 to S1. A high pulse is input to SBT pin with pulse width equal to or longer than the debounce time to strobe the data to initial the playblack. Data patterns “11110” and “11111” are reserved and not allowed.



Group-n	S5	S4	S3	S2	S1	Group-n	S5	S4	S3	S2	S1
Group1	0	0	0	0	0	Group9	0	1	0	0	0
Group2	0	0	0	0	1	Group10	0	1	0	0	1
Group3	0	0	0	1	0	Group11	0	1	0	1	0
Group4	0	0	0	1	1	Group12	0	1	0	1	1
Group5	0	0	1	0	0	Group13	0	1	1	0	0
Group6	0	0	1	0	1	Group14	0	1	1	0	1
Group7	0	0	1	1	0	Group15	0	1	1	1	0
Group8	0	0	1	1	1	Group16	0	1	1	1	1

Group-n	S5	S4	S3	S2	S1	Group-n	S5	S4	S3	S2	S1
Group17	1	0	0	0	0	Group25	1	1	0	0	0
Group18	1	0	0	0	1	Group26	1	1	0	0	1
Group19	1	0	0	1	0	Group27	1	1	0	1	0
Group20	1	0	0	1	1	Group28	1	1	0	1	1
Group21	1	0	1	0	0	Group29	1	1	1	0	0
Group22	1	0	1	0	1	Group30	1	1	1	0	1
Group23	1	0	1	1	0	Reserve	1	1	1	1	0
Group24	1	0	1	1	1	Reserve	1	1	1	1	1

■ Block Diagram



■ Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +4.5	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating)	-10 ~ +60	℃
T (Storage)	-55 ~ +125	℃

■ Pin Description

Pin No.	Name	I/O/P	Function
1	S8	I	Trigger switch 8, internal pull low, active high
2	OUT1	O	Programmable output 1
3	V_{OUT1}	O	PWM audio signal output 1 for buzzer & speaker
4	V_{OUT2}	O	PWM audio signal output 2 for buzzer & speaker
5	V_{SS}	P	Power ground
6	OUT2	O	Programmable output 2
7	OUT3	O	Programmable output 3
8	C_{OUT}	O	Current output from internal DAC for speaker playback
9	OSC	I	Oscillator resistor pin to control sampling frequency
10	S5	I	Trigger switch 5 / CPU Addr.5 (MSB), internal pull low, active high
11	S6	I	Trigger switch 6, internal pull low, active high
12	VPP	P	Program power, must connect to VDD when playback
13	S1	I	Trigger switch 1 / CPU Addr.1 (LSB), internal pull low, active high
14	S2	I	Trigger switch 2 / CPU Addr.2, internal pull low, active high
15	V_{DD}	P	Positive power supply
16	S3	I	Trigger switch 3 / CPU Addr.3, internal pull low, active high
17	S4	I	Trigger switch 4 / CPU Addr.4, internal pull low, active high
18	SBT	I	Key Sequential/CPU trigger, internal pull low, active high
19	IRP	I	Interrupt to stop playback, internal pull low, active high
20	S7	I	Trigger switch 7, internal pull low, active high

Note1: The following pins are used to program data into the memory: 5 – 7 and 9 - 20.
Note2: Vpp and Vcc MUST be connected to positive power supply during normal playback. However, they MUST be separated during data programming.

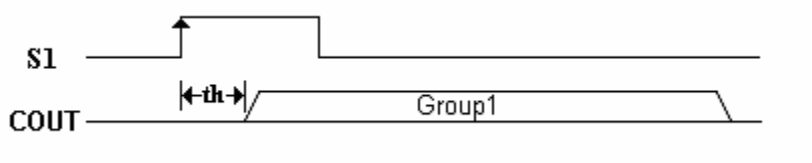
■ DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.7	3.0	3.8	V	
I_{SB}	Standby current	—	1	5	μA	V_{DD}=3.0V, I/O open
I_{OP}	Operating current	—	—	15	mA	V_{DD}=3.0V, I/O open
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	V_{DD}=3.0V
I_{OL}	V_{OUT} low O/P Current	—	120	—	mA	V_{DD}=3.0V, Vout=0.3V
I_{OH}	V_{OUT} high O/P Current	—	-65	—	mA	V_{DD}=3.0V, Vout=2.5V
I_{CO}	C_{OUT} O/P Current	—	-3	—	mA	V_{DD}=3.0V,V_{COUT}=1.0V
I_{OH}	O/P high Current	—	-8	—	mA	V_{DD}=3.0V, V_{OH}=2.5V
I_{OL}	O/P low Current	—	8	—	mA	V_{DD}=3.0V, V_{OL}=0.3V
ΔF/F	Frequency Stability	-5	—	+5	%	$\frac{Fosc(2.7V) - Fosc(3.4V)}{Fosc(3V)}$

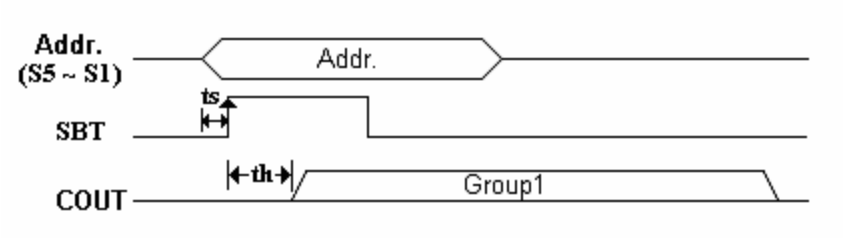
■ AC Characteristics

1. INPUT SETUP AND HOLD TIME :

◆ KEY Trigger Mode : **S1** to **S8** hold time, **th** (min.) = 22ms @ 6K Hz sampling



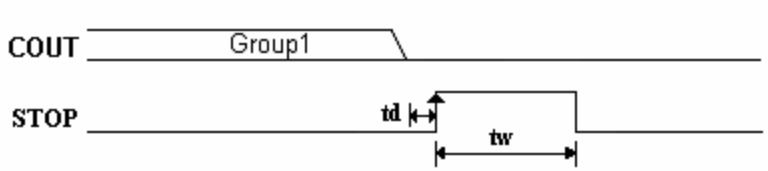
◆ CPU Trigger Mode : **SBT** setup time **ts** (min.) = 1us, and
S1 to **S5** hold time **th** (min.) = 22ms @ 6K Hz sampling



Note: Input hold time **th** is inverse proportional to the sampling frequency.

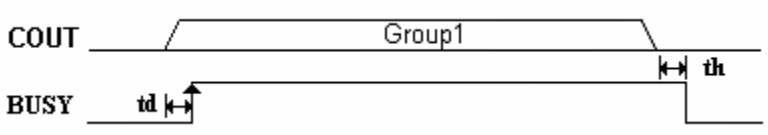
2. OUTPUTS DELAY TIME :

◆ STOP : Delay time **td** (max.) = 1us, plus width **tw** (min.) = 64ms @ 6K Hz sampling



Note: The pulse width **tw** is inverse proportional to the sampling frequency.

◆ BUSY : Delay time **td** (max.) = 1us, hold time **th** (max.) = 1us @ 6K Hz sampling



Note: The BUSY delay time **td** and hold time **th** is fixed and
independent of sampling frequency.

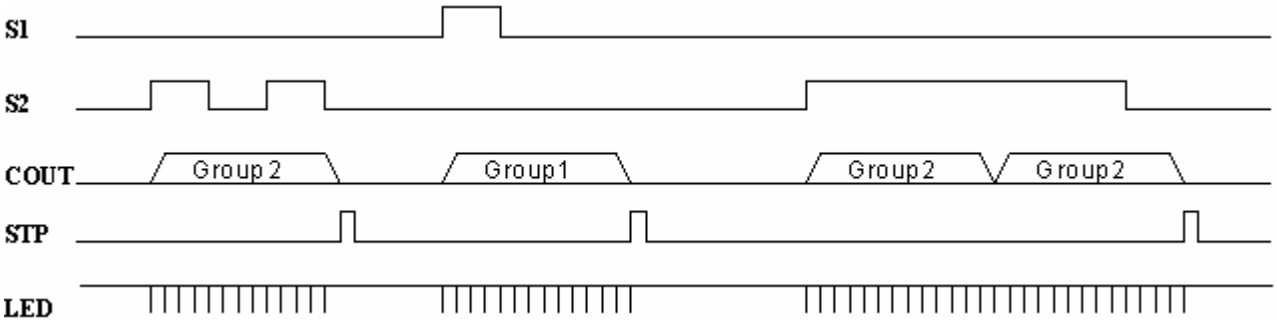
◆ LED flash at fixed 2Hz @ 6K Hz sampling

Timing Diagrams

1. Level, Unholdable, Non-retriggerable

a. Trigger is shorter than a Group output

b. Trigger is longer than a Group output



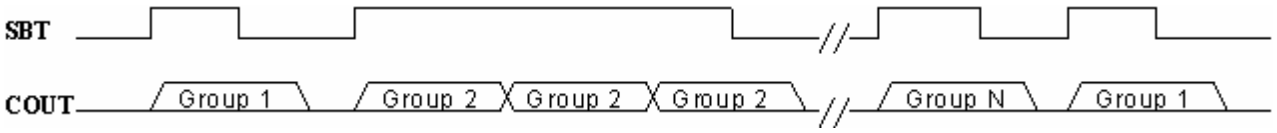
2. Level Holdable

a. Trigger is shorter than a Group output

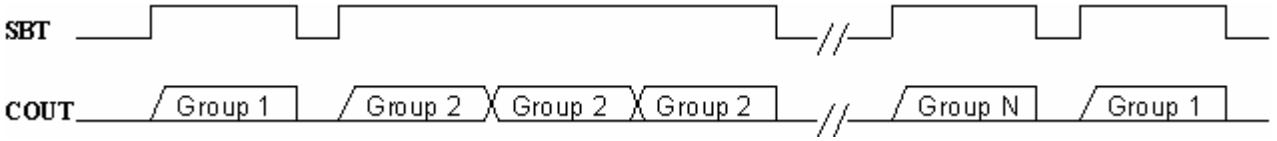
b. Trigger is longer than a Group output

3. Single Button Trigger(SBT), Sequential

a. Level Unholdable



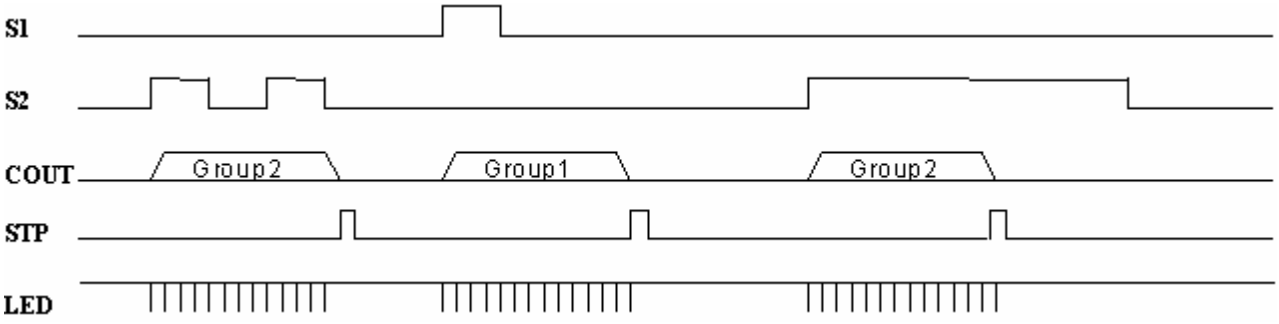
b. Level Holdable



where N is up to 30.

4. Edge, Unholdable, Non-retriggerable

a. Trigger is shorter than a Group output b. Trigger is longer than a Group output



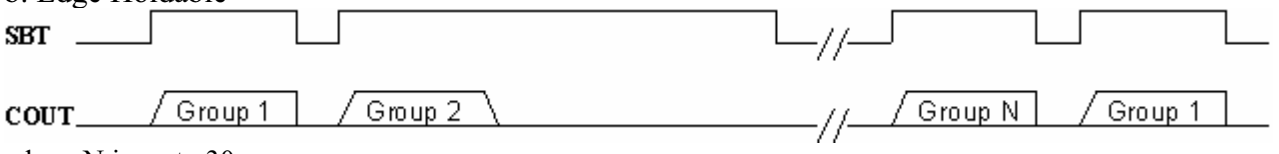
5. Edge Holdable

a. Trigger is shorter than a Group output b. Trigger is longer than a Group output

6. Single Button Trigger(SBT), Sequential

a. Edge Unholdable

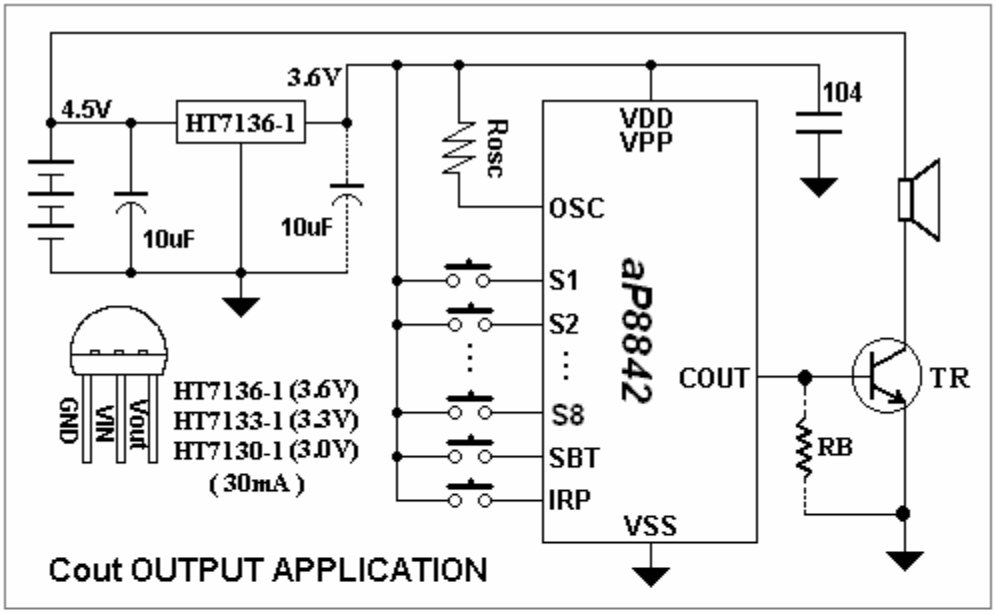
b. Edge Holdable



where N is up to 30.

■ Application Circuits

1. Typical Application



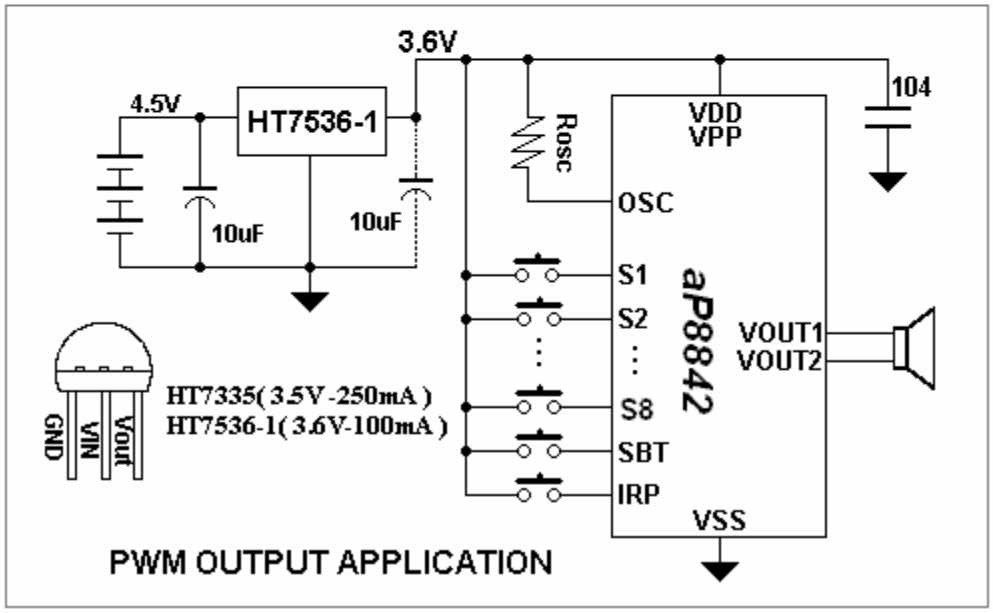


Fig. 1a COUT with transistor

Fig. 1b VOUT direct drive

2. CPU Mode control

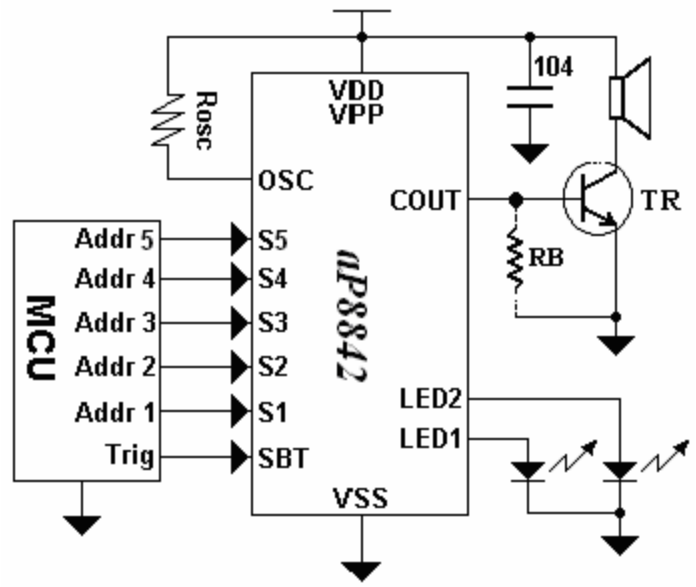
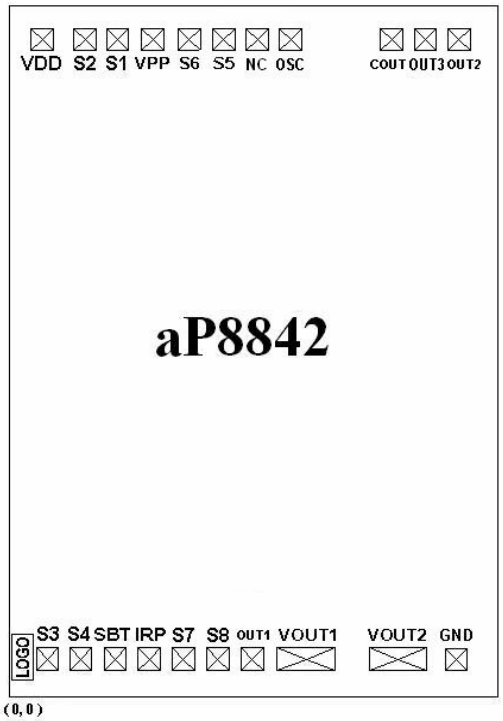


Fig. 2

■ Bonding Pad Locations

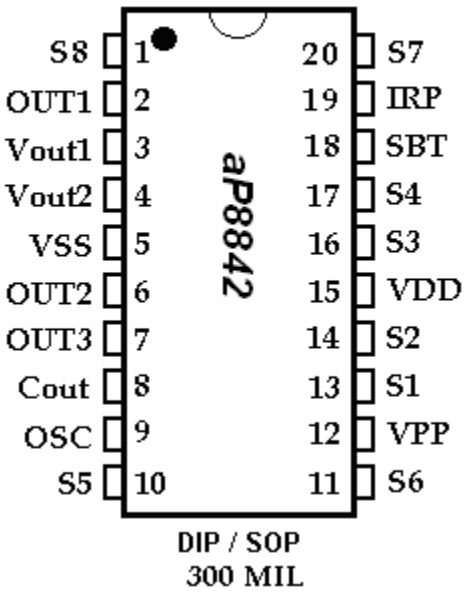


Pin	Name	X	Y
1	S8	883	180
2	OUT1	1024	180
3	VOUT1	1247	180
4	VOUT2	1625	180
5	VSS	1864	180
6	OUT2	1876	2697
7	OUT3	1736	2697
8	COUT	1598	2697
9	OSC	1182	2697
10	S5	907	2697
11	S6	766	2697
12	VPP	614	2697
13	S1	471	2697
14	S2	336	2697
15	VDD	159	2697
16	S3	180	180
17	S4	319	180
18	SBT	459	180
19	IRP	600	180
20	S7	740	180

Note:Substrate must be connected to V_{SS}

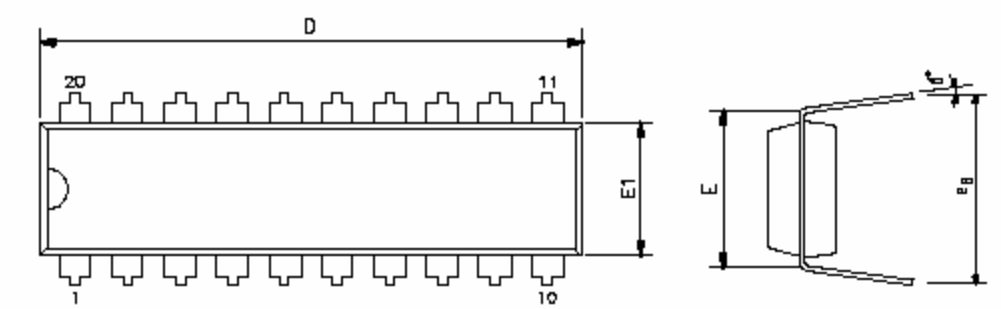
Pad size = 90um x 90um

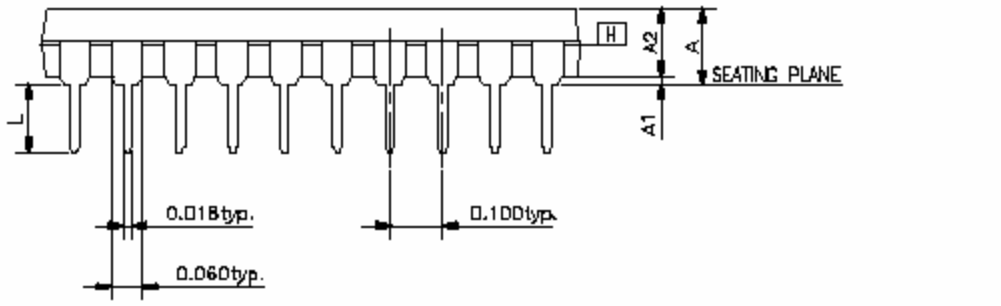
PIN CONFIGURATIONS



DIP / SOP
300 MIL

- Package : DIP - 20 pin - 300 mil





SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.98	1.030	1.060
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 AD
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.