NIPPON PRECISION CIRCUITS INC.

SM8211M

POCSAG Decoder For Pagers

OVERVIEW

The SM8211M is a POCSAG-standard (Post Office Code Standardization Advisory Group) signal processor LSI, which conforms to CCIR recommendation 584 concerning standard international wireless calling codes.

The SM8211M supports call messages in either tone, numerical or character outputs at signal speeds of 512 bps or 1200 bps using a 76.8 kHz system clock, or 2400 bps using a double-speed 153.6 kHz system clock. Note that output timing values for 2400 bps mode operation are not shown in this datasheet, but can be obtained by halving the values for 1200 bps mode operation.

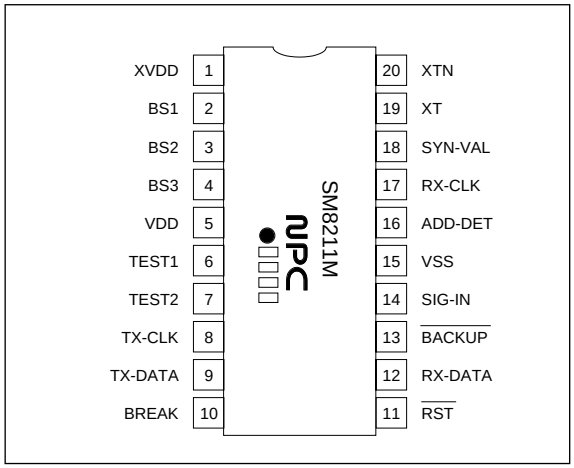
CMOS structure and low-voltage operation realize low power dissipation, plus an intermittent-duty receive method (battery-saving function) reduces battery consumption.

The SM8211M is available in 20-pin SSOPs.

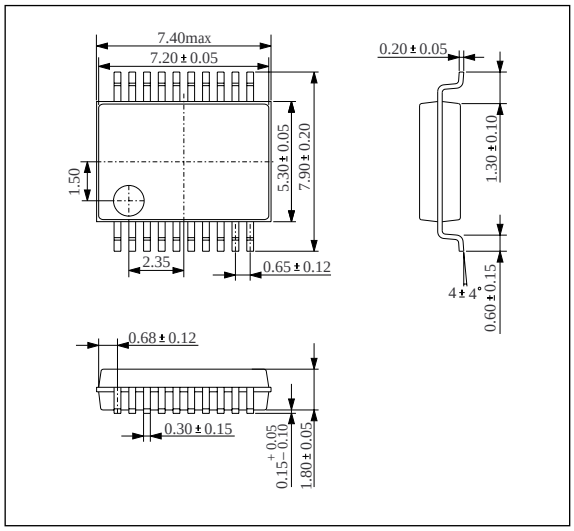
FEATURES

- Conforms to POCSAG standard for pagers
- 512 or 1200 bps signal speed
- Supports tone, numeric or character call messages
- Battery-saving function for low battery consumption
- BS1 (RF control main output signal) and BS3 (PLL setup signal) 60-step setup time setting—for BS3, 50.8 ms (max) at 1200 bps and 119.1 ms (max) at 512 bps
  Note that (BS3 setup time) − (BS1 setup time) should be set to ≥ 2.
- BS2 (RF DC-level adjustment signal) before/during reception selectable adjustment timing
- 6 addresses × 4 sub-addresses (total of 24 addresses)
- 1-bit and 2-bit burst error auto-correction function (messages only)
- 25 to 75% duty factor signal coverage (during preamble detection)
- 8 rate error detection condition settings
- 8 receive mode settings
- 76.8 or 153.6 kHz system clock (crystal oscillator or external clock input)
- Built-in oscillator capacitor
- Built-in input signal filter, with filter ON/OFF and 4 selectable filter characteristics
- 1.2 to 3.5 V (76.8 kHz system clock) or 2.0 to 3.5 V (153.6 kHz system clock) operating supply voltage
- Molybdenum-gate CMOS process realizes low power dissipation
- 20-pin SSOP

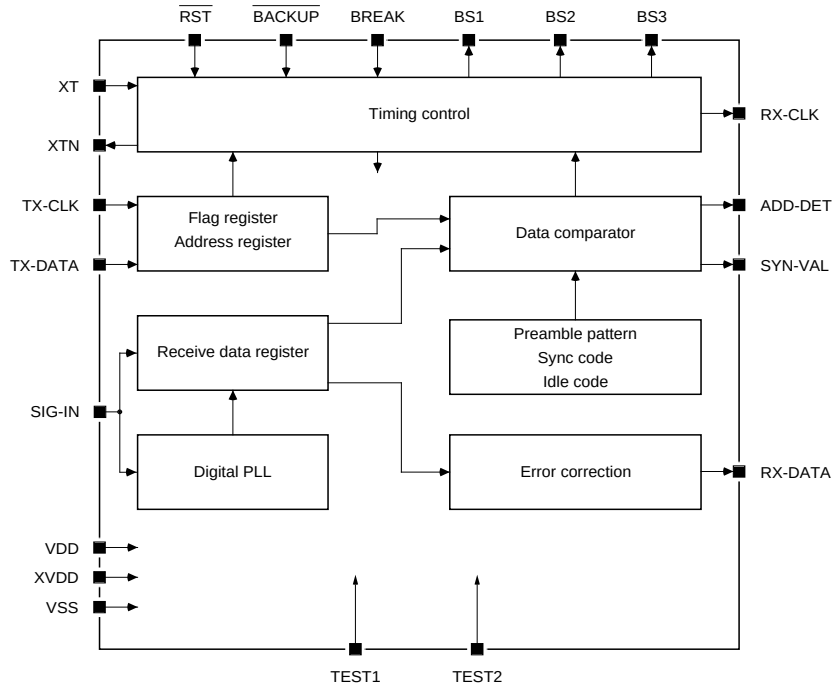
PINOUT



PACKAGE DIMENSIONS



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	XVDD	–	Oscillator circuit supply pin. Capacitor connected between XVDD and VSS.
2	BS1	O	RF control main output signal
3	BS2	O	RF DC-level adustment signal
4	BS3	O	PLL setup signal
5	VDD	–	Supply voltage
6	TEST1	I	Test pin. Leave open for normal operation.
7	TEST2	I	Test pin. Leave open for normal operation.
8	TX-CLK	I	ID data read sync clock
9	TX-DATA	I	ID data input
10	BREAK	I	Message transmission interrupt
11	$\overline{\text{RST}}$	I	Hardware reset input
12	RX-DATA	O	Received data output (to CPU)
13	$\overline{\text{BACKUP}}$	I	Power save
14	SIG-IN	I	NRZ signal input pin
15	VSS	–	Ground
16	ADD-DET	O	Address detection output. HIGH on detection
17	RX-CLK	O	Received data output sync clock
18	SYN-VAL	O	Sync code detection output. HIGH on detection
19	XT	I	76.8 or 153.6 kHz oscillator or external clock input pin
20	XTN	O	Oscillator output pin

I:Input O:Output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	°C
Soldering temperature	T_{sld}	260	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}	76.8 kHz system clock	1.2 to 3.5	V
		153.6 kHz system clock	2.0 to 3.5	
Operating temperature range	T_{opr}		–20 to 70	°C

DC Characteristics

V_{DD} = 1.2 to 3.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Consumption current[1]	I_{DD}	XT = 76.8 kHz, V_{DD} = 3.5 V	–	20.0	30.0	µA
		XT = 153.6 kHz, V_{DD} = 3.5 V	–	25.0	35.0	
HIGH-level input voltage (all inputs)	V_{IH}		0.8V_{DD}	–	–	V
LOW-level input voltage (all inputs)	V_{IL}		–	–	0.2V_{DD}	V
HIGH-level output voltage (all outputs except XTN)	V_{OH}	I_{OH} = –20 µA, V_{DD} = 2.0 V	V_{DD} – 0.1	–	–	V
LOW-level output voltage (all outputs except XTN)	V_{OL}	I_{OH} = 20 µA, V_{DD} = 2.0 V	–	–	0.1	V
Input leakage current (all inputs except XT)	I_{IL}	V_{IN} = V_{DD} or V_{SS}	–	–	±1.0	µA
Standby supply current	I_{DDS}	T_a = 25 °C	–	–	1.0	µA

1. The consumption current is slightly higher when $\overline{RST}$ is going LOW.

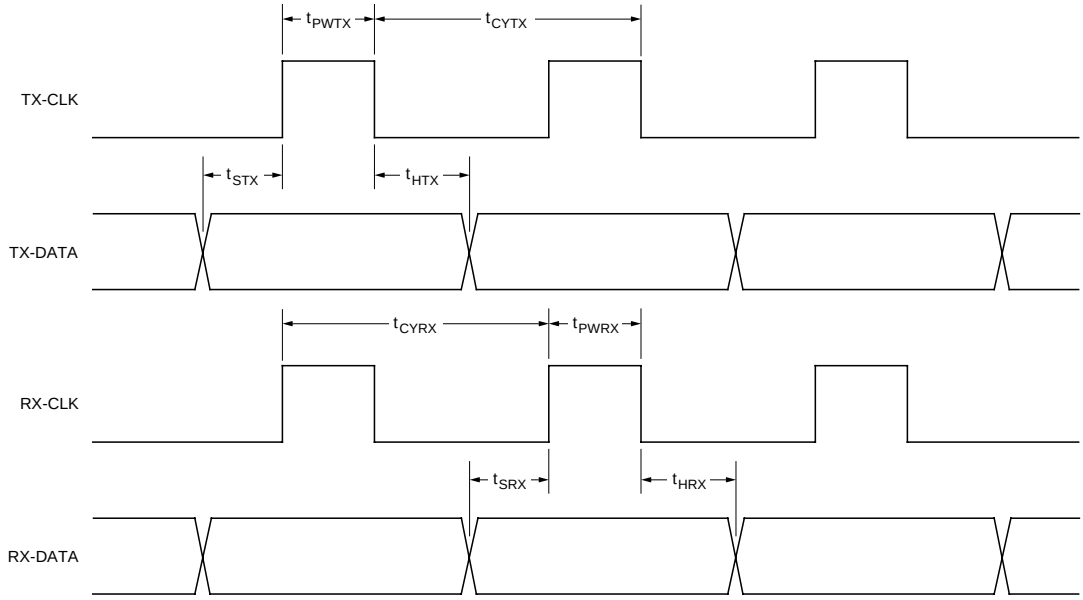
AC Characteristics

V_{DD} = 1.2 to 3.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
TX-CLK pulsewidth	t_{PWTX}		13	–	100	µs
TX-CLK pulse cycle	t_{CYTX}		450	–	–	µs
TX-DATA setup time	t_{STX}		1.0	–	–	µs
TX-DATA hold time	t_{HTX}		1.0	–	–	µs
XT pulse frequency	t_{CYXT}		–250 ppm	76.8 or 153.6	+250 ppm	kHz
XT pulse duty cycle	D_{XT}		25	–	75	%
BREAK pulsewidth	t_{PWBR}		13	–	–	µs
RX-CLK pulse cycle[1]	t_{CYRX}	512 bps	–	1953	–	µs
		1200 bps	–	833	–	
RX-CLK pulsewidth[1]	t_{PWRX}	512 bps	–	124	–	µs
		1200 bps	–	52	–	
RX-DATA lead time[1]	t_{SRX}	512 bps	–	1341	–	µs
		1200 bps	–	573	–	
RX-DATA hold time[1]	t_{HRX}	512 bps	–	488	–	µs
		1200 bps	–	208	–	

1. Internal digital PLL operation is subject to some change.

AC timing



FUNCTIONAL DESCRIPTION

Receive Format

The receive format conforms to CCIR RPC No. 1 (POCSAG).

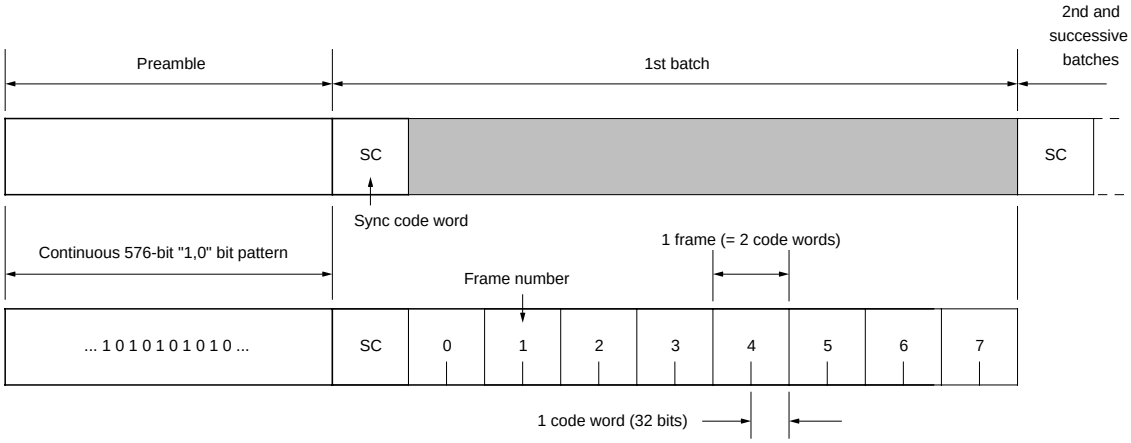


Figure 1. Receive signal format

Sync signal (SC)

The sync signal is a continuous code word in the received signal, used for word synchronization. It comprises 31 bits in an M-series bit pattern plus one even-parity bit, making a 32-bit signal. The sync code word pattern is shown in table 1.

Table 1. Sync code word

Bit number	Bit value	Bit number	Bit value	Bit number	Bit value	Bit number	Bit value
1	0	9	1	17	0	25	1
2	1	10	1	18	0	26	1
3	1	11	0	19	0	27	0
4	1	12	1	20	1	28	1
5	1	13	0	21	0	29	1
6	1	14	0	22	1	30	0
7	0	15	1	23	0	31	0
8	0	16	0	24	1	32	0

Code words (address and message signals)

Each code word comprises 32 bits as shown in table 2.

Table 2. Code word format

<table>
<tr><th rowspan="2">Code word</th><th colspan="5">Bit number</th></tr>
<tr><th>1 (MSB)[1]</th><th>2 to 19[2]</th><th>20, 21[2]</th><th>22 to 31[3]</th><th>32 (LSB)[4]</th></tr>
<tr><td>Address signal</td><td>0</td><td>Address bits</td><td>Function bits
<table><tr><th>20</th><th>21</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>A call</td></tr><tr><td>0</td><td>1</td><td>B call</td></tr><tr><td>1</td><td>0</td><td>C call</td></tr><tr><td>1</td><td>1</td><td>D call</td></tr></table></td><td>Check bits</td><td>Even-parity bit</td></tr>
<tr><td>Message signal</td><td>1</td><td colspan="2">Message bits</td><td>Check bits</td><td>Even-parity bit</td></tr>
</table>

1. The MSB is the address/message code word control bit. It is 0 for an address signal, and 1 for a message signal.
2. Bits 2 to 21 contain the address or message information.
3. Bits 22 to 31 are BCH(31,21) format generated check bits, where BCH(n,k) = BCH(word length, number of information bits).
4. The LSB is an even-parity bit for bits 1 to 31.

Call number to call sign conversion

This conversion expands a 7-digit decimal call number into a 21-bit binary call sign, as shown in figure 2.

After expansion, the high-order 18 bits are assigned to bits 2 to 19 (address signal), and the low-order 3 bits are the user-defined frame identification pattern, which is stored in ID-ROM. The two function bits define which of four call functions is active.

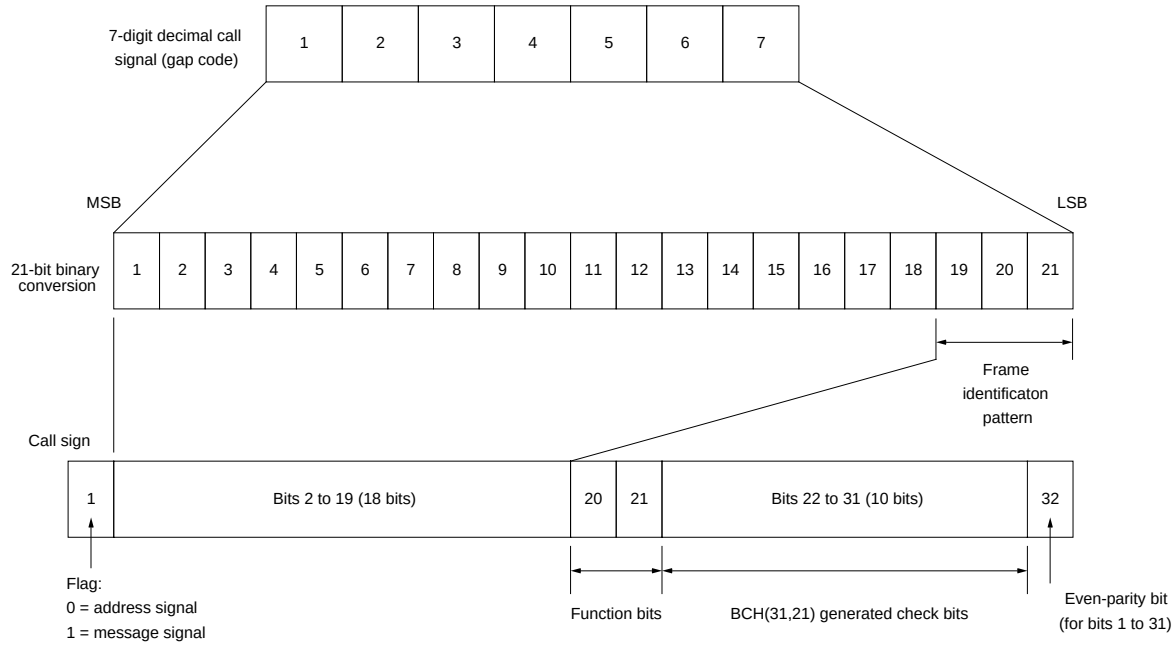


Figure 2. Call number to call sign conversion

Idle signal (dummy signal)

An idle word can be inserted into either the address or message signal to indicate that the word contains no information. The idle word bit pattern is shown in table 3. Message reception is halted when the receiver detects an idle word.

In pager systems that send numeric data, the number of frames varies with the type of message being sent. In this case, an idle signal is transmitted to indicate completion of the message.

Table 3. Idle code word

Bit number	Bit value	Bit number	Bit value
1	0	17	1
2	1	18	1
3	1	19	0
4	1	20	0
5	1	21	0
6	0	22	0
7	1	23	0
8	0	24	1
9	1	25	1
10	0	26	0
11	0	27	0
12	0	28	1
13	1	29	0
14	0	30	1
15	0	31	1
16	1	32	1

Receive signal duty factor

During preamble detection, the preamble pattern (1,0) is recognized at duty factors from 25% (min) to 75% (max) of the (1,0) preamble cycle.

Battery Saving (BS1, BS2, BS3)

The SM8211M controls the intermittent-duty operation of the RF stage, which reduces battery consumption, and outputs three control signals (BS1, BS2, BS3). The function each signal controls in each mode is described below.

- BS1 (RF-control main output signal)—The RF stage is active when BS1 is HIGH. The rising-edge setup time for receive timing is set by flags RF0 to RF5 (60 steps). The maximum setup time is 49.167 ms at 1200 bps, and 115.234 ms at 512 bps.
  Note that 3C, 3D, 3E and 3F are invalid settings for BS1.
- BS2 (RF-control output signal)—BS2 is used to control the discharge of the receive signal DC-cut capacitor. The function of BS2 is determined by flag BS2, as described below.
  - When flag BS2 is 0, pin BS2 goes HIGH together with BS1 and then goes LOW again after the BS1 setup time. However, in lock mode (during address/message reception), it stays LOW.
  - When flag BS2 is 1, pin BS2 goes HIGH during lock mode sync code receive timing, and preamble mode and idle mode signal receive timing.
- BS3 (RF-control output signal)—BS3 is used to control PLL operation when the PLL is used. The rising-edge setup time for receive timing is set by flags PL0 to PL5 (60 steps). The maximum setup time is 50.833 ms at 1200 bps, and 119.141 ms at 512 bps.
  Note that 3E and 3F are invalid settings for BS3.

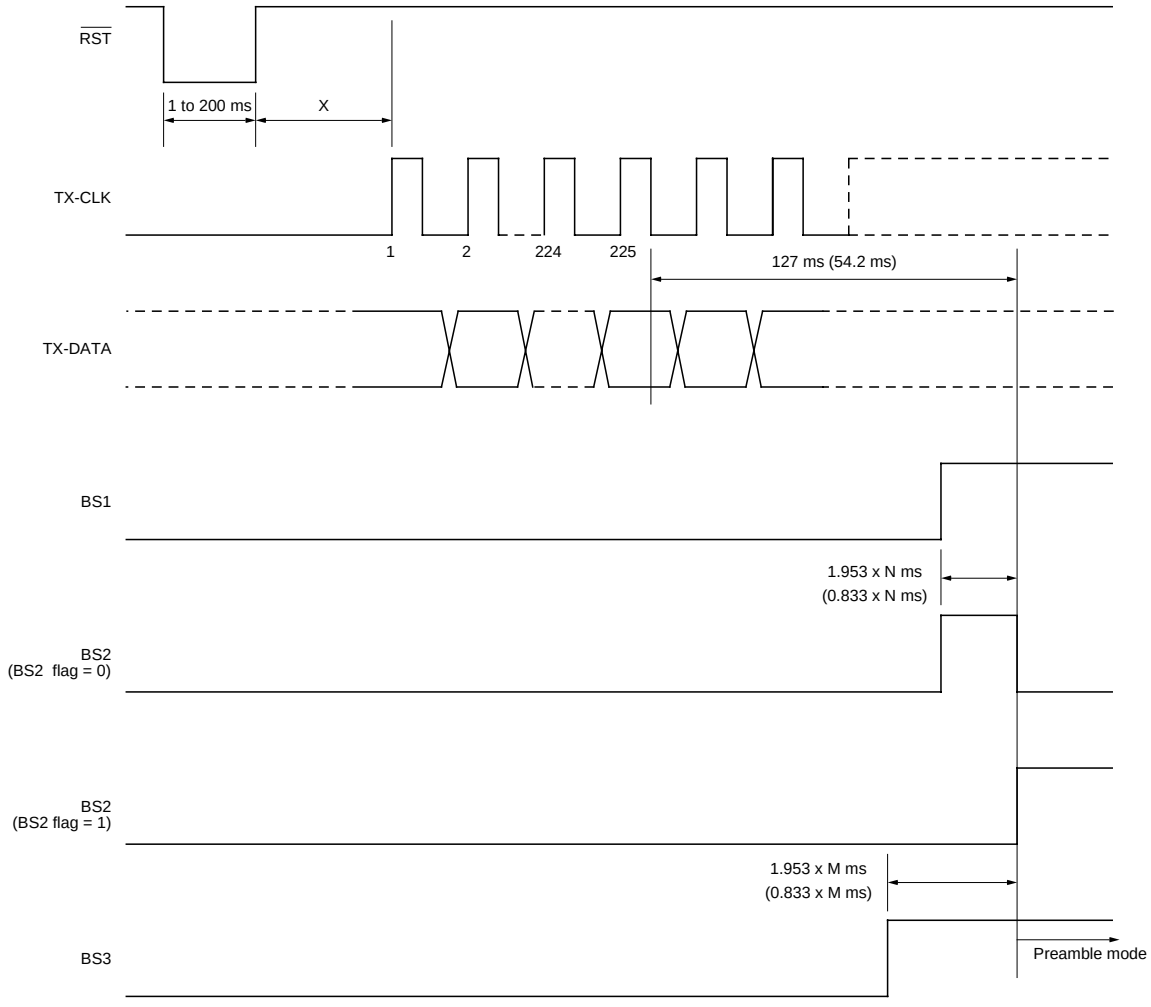
Note also that (BS3 rising-edge setup time) − (BS1 rising-edge setup time) should be ≥ 2.

Operating Modes

The SM8211M has four operating modes—Switch-ON, Preamble, Idle and Lock modes. Note that all values in parentheses in the following figures are for the case when the speed is 1200 bps.

Switch-ON mode

After power is applied and after $\overline{RST}$ has gone LOW to reset all internal circuits, code words for the 27-bit flag data and the six 18-bit addresses are received from the CPU on TX-DATA and are stored. As each code word comprises 32 bits, this process takes (32 × 7) + 1 TX-CLK cycles to complete. When the 225 TX-CLK cycles have been received, BS1, BS2 and BS3 are set and device operation transfers to preamble mode.



X > 2 ms for external system clock operation or during continuous oscillations
X > 900 ms for internal oscillator operation immediately after power is applied or $\overline{BACKUP}$ is released (V_{DD} = 1.5 to 3.5 V)
X > 1.5 s for internal oscillator operation immediately after power is applied or $\overline{BACKUP}$ is released (V_{DD} < 1.5 V)

Figure 3. Switch-ON mode timing

Preamble mode

Preamble mode is a continuous 544-bit long period. If neither a preamble pattern, rate error nor sync code is detected during this period, operation transfers to idle mode.

If a preamble pattern is detected, the preamble mode 544-bit long period is recommenced.

If a rate error is detected, device operation transfers to idle mode. (A single error occurs when two active edges occur in the received signal on SIG-IN within 1-bit unit time. A rate error occurs when the number of errors in the error counter equals the error threshold set by flags ER0 to ER2. The error counter is reset when a preamble pattern is detected.)

If the sync code is detected, SYN-VAL goes HIGH and operation transfers to lock mode. (If an error of 2 bits or less occurs, the detected word is recognized as the sync code.)

Idle mode

In idle mode, a check is made for the presence of a preamble signal when the RF intermittent-duty control signals (BS1, BS2, BS3) for battery saving are active. If a preamble pattern is detected, operation immediately transfers to preamble mode. If a preamble pattern is not detected, intermittent-duty operation continues.

A preamble pattern is detected when either a 101010 or 010101 6-bit pattern is detected. Since there is a reasonable probability that this simple pattern can occur during a valid communicated signal (data, not preamble), this 6-bit pattern makes returning to preamble mode easier. This is useful for cases where weak electric fields, noise or other temporary interference cause device operation to transfer to idle mode. Further, if a sync code is detected within one cycle after device operation has transferred from lock mode, device operation returns to lock mode. (If flag BS2 is 0, pin BS2 does not go HIGH during the cycle after device operation has transferred from lock mode.)

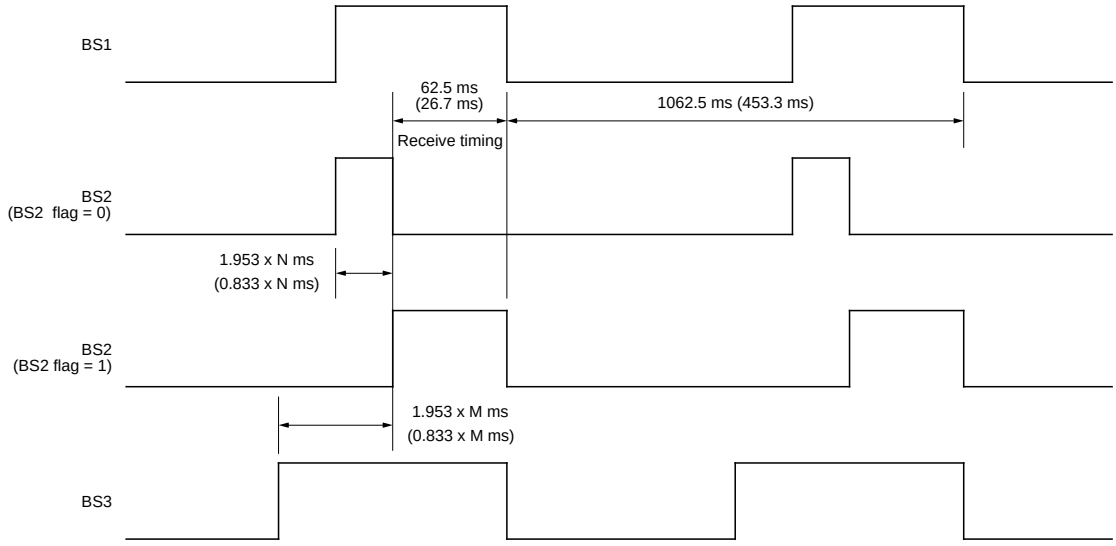


Figure 4. Idle mode timing

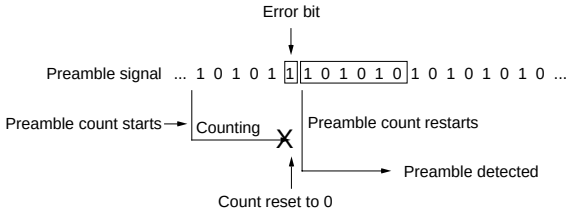


Figure 5. Preamble pattern sequence

Lock mode

If the sync code is detected during the preamble period, device operation transfers to lock mode and BS1 goes LOW. BS1 then goes HIGH again under frame timing, where the frame number is set by flags FF0 to FF2, and the 24 addresses are compared with ID-ROM (If the frame number is 0, BS1 stays HIGH). If errors of 2 bits or less occur, the address is still recognized. Since there are two code words per frame, this check is done twice.

When one of the 24 addresses does not match, BS1 goes LOW and the device waits for the next sync code receive timing. If the sync code is still not detected after two consecutive attempts, device operation transfers to idle mode, except during message reception where operation stays in lock mode. If the sync code is not detected on the second attempt, but instead a pattern forming a preamble is detected, device operation transfers to preamble mode and not idle mode (preamble mode is more advantageous for sync code detection).

When one of the 24 addresses does match, ADDDET goes HIGH for the duration of the next code word period and the corresponding 5-bit address information is transmitted to the CPU on RX-DATA in sync with RX-CLK. When the address information is confirmed, BS1 is held HIGH and the message is received. The 20-bit error-corrected message data, a 2-bit error correction result code and an even-parity bit form a 23-bit word that is sent to the CPU on RX-DATA in sync with RX-CLK. When an incoming message spans two or more batches, additional sync code detection occurs during sync code receive timing.

Message reception ends when an address code or idle code is detected, or when interrupted using the BREAK input. When message reception ends, BS1 goes LOW and the device waits for either the address detect timing of the next frame or the sync code receive timing.

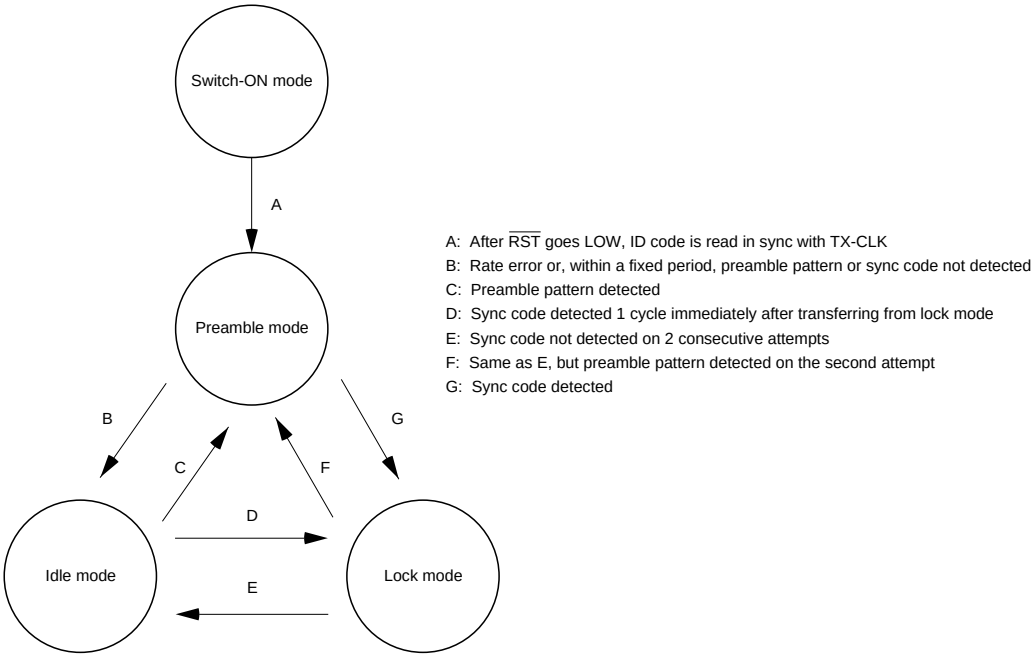


Figure 6. Operating mode transition diagram

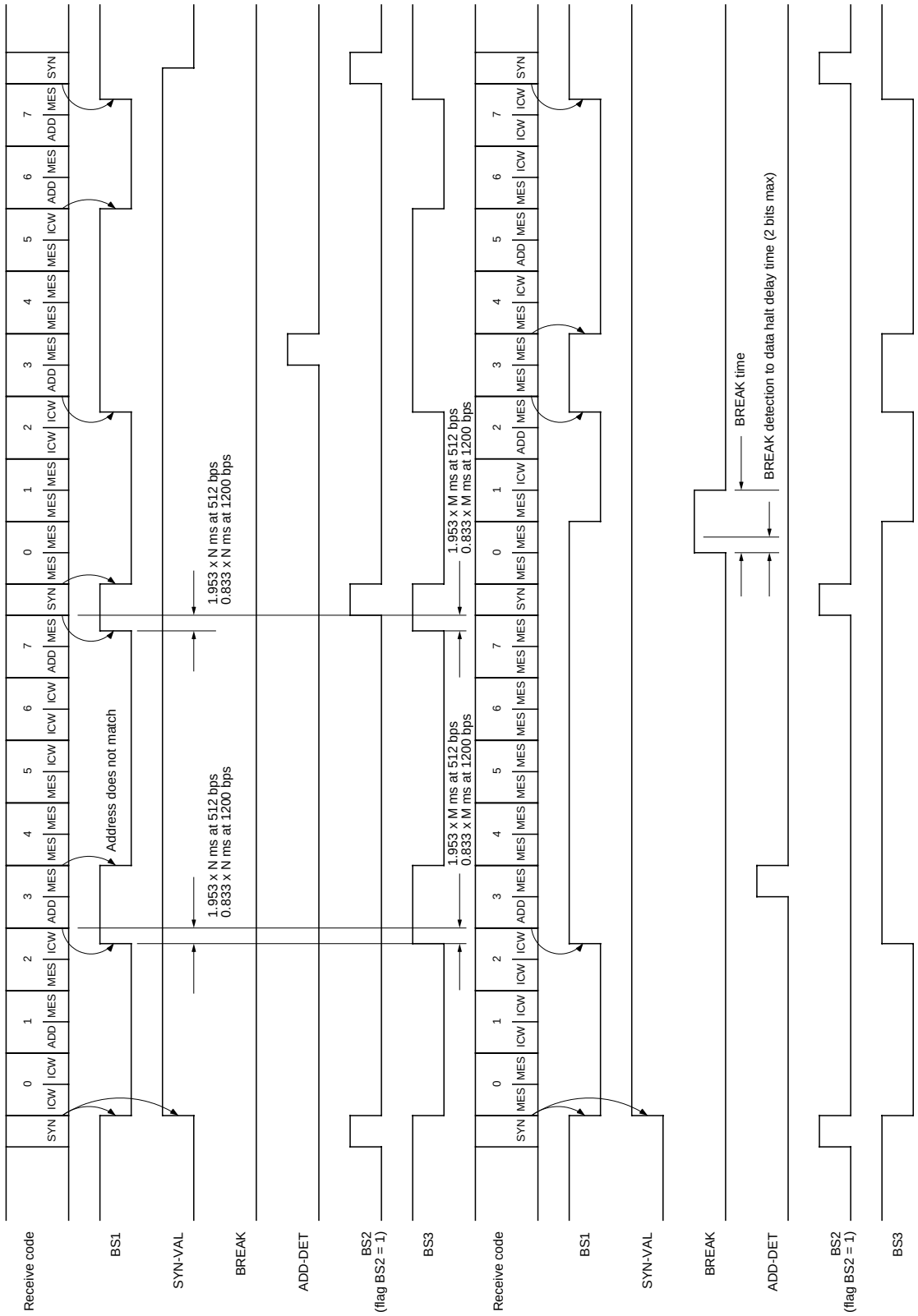


Figure 7. Lock mode timing (frame ID number 3)

Address/Flag Data Transmission (CPU to SM8211M)

After device reset initialization, the address and flag data is transmitted from the CPU on TX-DATA in 225 cycles in sync with the falling edge of TX-CLK. (See the description in “Switch-ON mode”).

The SM8211M supports six independent addresses (identified as A, B, C, D, E and F). Using these, it is possible to cover all kinds of group calls.

The address data for each of the six addresses comprises an 18-bit address plus two function bits used to select one of four sub-addresses. Then, one MSB bit (0 for address signals), ten BCH(31,21) format generated check bits and an even-parity bit are added to form 32-bit code words representing the address information which is then stored in RAM. This address information is then compared with the received data to determine correct addressing.

If the number of addresses used is less than six, the same address should be repeated as many times as necessary to cancel the remaining addresses. Also, each 18-bit address should be input MSB first.

The TX-CLK cycle and corresponding address data bits are shown in table 4, and the function of each flag is shown in tables 5 to 13.

Table 4. Address/flag transmit format

TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit	TX clock	Data bit
1	0	27	FL1	53	0	79	AB3	105	AC9	131	AD15	157	0	183	0	209	AF1
2	SS	28	FL0	54	0	80	AB2	106	AC8	132	AD14	158	0	184	0	210	AF0
3	S1	29	ER2	55	0	81	AB1	107	AC7	133	AD13	159	0	185	0	211	0
4	S0	30	ER1	56	0	82	AB0	108	AC6	134	AD12	160	0	186	0	212	0
5	LBO	31	ER0	57	0	83	0	109	AC5	135	AD11	161	AE17	187	0	213	0
6	FF2	32	0	58	0	84	0	110	AC4	136	AD10	162	AE16	188	0	214	0
7	FF1	33	AA17	59	0	85	0	111	AC3	137	AD9	163	AE15	189	0	215	0
8	FF0	34	AA16	60	0	86	0	112	AC2	138	AD8	164	AE14	190	0	216	0
9	INV	35	AA15	61	0	87	0	113	AC1	139	AD7	165	AE13	191	0	217	0
10	BS2	36	AA14	62	0	88	0	114	AC0	140	AD6	166	AE12	192	0	218	0
11	0	37	AA13	63	0	89	0	115	0	141	AD5	167	AE11	193	AF17	219	0
12	0	38	AA12	64	0	90	0	116	0	142	AD4	168	AE10	194	AF16	220	0
13	0	39	AA11	65	AB17	91	0	117	0	143	AD3	169	AE9	195	AF15	221	0
14	PL5	40	AA10	66	AB16	92	0	118	0	144	AD2	170	AE8	196	AF14	222	0
15	PL4	41	AA9	67	AB15	93	0	119	0	145	AD1	171	AE7	197	AF13	223	0
16	PL3	42	AA8	68	AB14	94	0	120	0	146	AD0	172	AE6	198	AF12	224	0
17	PL2	43	AA7	69	AB13	95	0	121	0	147	0	173	AE5	199	AF11	225	0
18	PL1	44	AA6	70	AB12	96	0	122	0	148	0	174	AE4	200	AF10		
19	PL0	45	AA5	71	AB11	97	AC17	123	0	149	0	175	AE3	201	AF9		
20	RF5	46	AA4	72	AB10	98	AC16	124	0	150	0	176	AE2	202	AF8		
21	RF4	47	AA3	73	AB9	99	AC15	125	0	151	0	177	AE1	203	AF7		
22	RF3	48	AA2	74	AB8	100	AC14	126	0	152	0	178	AE0	204	AF6		
23	RF2	49	AA1	75	AB7	101	AC13	127	0	153	0	179	0	205	AF5		
24	RF1	50	AA0	76	AB6	102	AC12	128	0	154	0	180	0	206	AF4		
25	RF0	51	0	77	AB5	103	AC11	129	AD17	155	0	181	0	207	AF3		
26	FL2	52	0	78	AB4	104	AC10	130	AD16	156	0	182	0	208	AF2		

Table 5. Flag functions

Flag	Function
SS	Receive mode set ON/OFF. ON when 1.
S0, S1	One of eight operating conditions select (with LBO when SS is 1)
LBO	512/1200 bps speed select. 512 bps when 1.
FF0 to FF2	Frame number select
INV	Signal input (SIG-IN) normal/inverse select. Normal when 0.
BS2	BS2 output signal mode select
PL0 to PL5	BS3 output signal rising-edge setup time for receive timing
RF0 to RF5	BS1 output signal rising-edge setup time for receive timing
FL2	Internal digital filter ON/OFF. ON when 1.
FL0, FL1	Digital filter parameter select (when FL2 is 1)
ER0 to ER2	Rate error detection threshold select

Table 6. Receive mode set flags[1]

SS	S1	S0	LBO	Set flags																
				PL5	PL4	PL3	PL2	PL1	PL0	RF5	RF4	RF3	RF2	RF1	RF0	FL2	FL1	FL0	ER2	ER1	ER0
1	0	0	0	1	1	1	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1
1	0	1	0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	1	0	0	1
1	1	0	0	1	1	1	1	0	1	0	0	1	1	1	0	1	0	1	0	0	1
1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	0	0	1	0	0	1	0	1	0	0	1
1	0	1	1	0	1	1	0	1	1	0	0	0	1	0	1	1	0	1	0	0	1
1	1	0	1	0	1	1	0	1	1	0	0	0	1	1	0	1	0	1	0	0	1
1	1	1	1	0	1	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1
0	×	×	0	All other combinations not set automatically																	
0	×	×	1																		

1. × = don't care

Table 7. Baud rate flag

LBO	Baud rate
0	1200 bps
1	512 bps

Table 8. Input polarity flag

INV	Polarity
0	Normal
1	Inverse

Table 9. BS2 flag

BS2	BS2 operating mode
0	See the description in section "Battery Saving (BS1, BS2, BS3)"
1	

Table 10. Frame number flags

FF2	FF1	FF0	Frame number
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 11. PLL setup time flags/BS1 rising-edge setup time flags[1]

PL5 (RF5)	PL4 (RF4)	PL3 (RF3)	PL2 (RF2)	PL1 (RF1)	PL0 (RF0)	PLL setup time (BS1 rising-edge setup time)	
						LBO = 0	LBO = 1
0	0	0	0	0	0	0.000 ms	0.000 ms
0	0	0	0	0	1	0.833 ms	1.953 ms
0	0	0	0	1	0	1.667 ms	3.906 ms
↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	1	1	25.833 ms	60.547 ms
1	0	0	0	0	0	26.667 ms	62.500 ms
1	0	0	0	0	1	27.500 ms	64.453 ms
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	0	1	50.833 ms	119.141 ms

1. Note that (BS3 rising-edge setup time) – (BS1 rising-edge setup time) should be ≥ 2.

Table 12. Digital filter constant set flags[1]

FL2	FL1	FL0	Filter constant
0	×	×	Digital filter not used
1	0	0	Filter constant 1
1	0	1	Filter constant 2
1	1	0	Filter constant 3
1	1	1	Filter constant 4

1. × = don't care

Table 13. Rate error detection set flags

ER2	ER1	ER0	Rate error threshold
0	0	0	Count = 1
0	0	1	Count = 2
0	1	0	Count = 3
0	1	1	Count = 4
1	0	0	Count = 5
1	0	1	Count = 6
1	1	0	Count = 7
1	1	1	Count = 8

Received Data Transmission (SM8211M to CPU)

In lock mode, if the receive data for the frame is recognized as one of the 24 addresses with 2 bit errors or less, then ADD-DET goes HIGH for the duration of the next code word period and the corresponding 5-bit address information is transmitted to the CPU on RX-DATA in sync with RX-CLK.

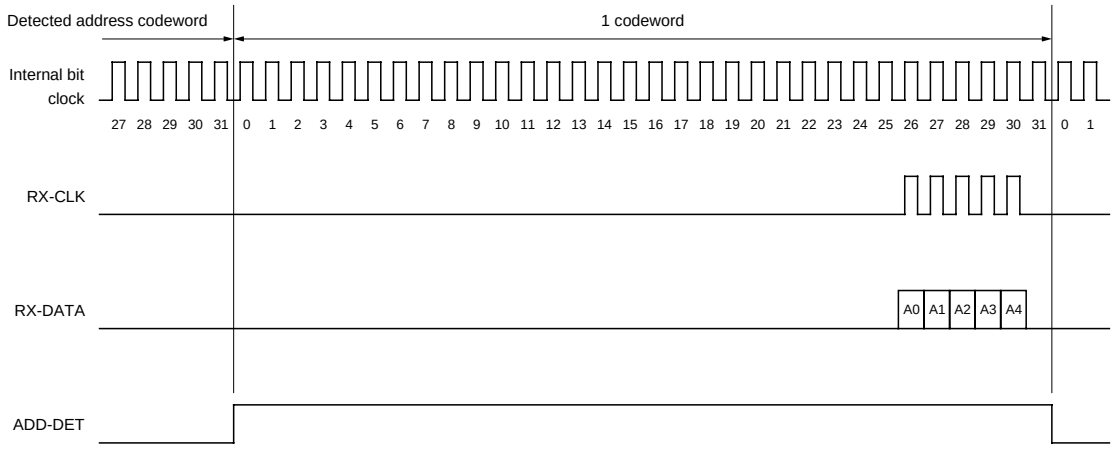


Figure 8. Received address transmit timing

Table 14. Address set flags

A0	A1	A2	A3	A4	Address	Function	A0	A1	A2	A3	A4	Address	Function
0	0	1	0	0	A	A call	0	0	0	0	1	D	A call
1	0	1	0	0		B call	1	0	0	0	1		B call
0	1	1	0	0		C call	0	1	0	0	1		C call
1	1	1	0	0		D call	1	1	0	0	1		D call
0	0	0	1	0	B	A call	0	0	1	0	1	E	A call
1	0	0	1	0		B call	1	0	1	0	1		B call
0	1	0	1	0		C call	0	1	1	0	1		C call
1	1	0	1	0		D call	1	1	1	0	1		D call
0	0	1	1	0	C	A call	0	0	0	1	1	F	A call
1	0	1	1	0		B call	1	0	0	1	1		B call
0	1	1	1	0		C call	0	1	0	1	1		C call
1	1	1	1	0		D call	1	1	0	1	1		D call

When an address is detected, the next 32-bit data code word is received. The BCH(31,21) format error check bits are checked and if a 1-bit or two consecutive bit errors occur, they are corrected. Two random bit errors, or three or more bit errors are not corrected. If the corrected data MSB is 1, the data is recognized as a message, data reception continues and the corrected message data and error check flags are sent to the CPU. If the MSB is 0, the data is recognized as an address signal or idle code and data reception or data transmission to the CPU is halted.

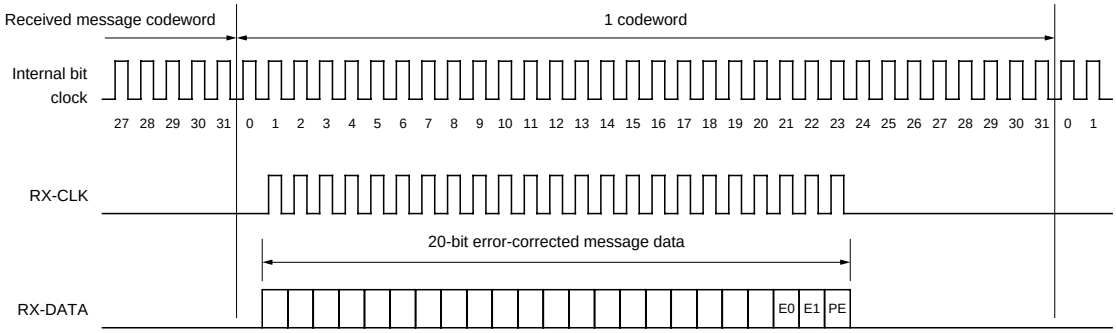


Figure 9. Received message transmit timing

Table 15. Error count flags

E0	E1	Error count
0	0	No errors
1	0	1-bit error
0	1	Two consecutive bit errors
1	1	Two random, or three or more bit errors

Table 16. Parity check flag

PE	Even-parity check result[1]
0	No errors
1	An error occurred

1. The even-parity check is performed on the data before error correction.

CPU Interface

SYN-VAL

If a sync code is detected with two bit errors or less during sync code detection timing while in preamble, lock or idle mode, SYN-VAL goes HIGH for the duration of the next batch (544 bits long).

ADD-DET

If frame data is received and recognized with two bit errors or less while in lock mode, ADD-DET goes HIGH for the duration of the next code word period. If an address is detected in the second code word in the frame, ADD-DET stays HIGH for the duration of two code word periods.

BREAK

On a rising edge of BREAK, message reception and received message transmission are halted. After a BREAK interrupt, the device waits for frame address detection or sync code detection timing. This function is useful in cases of continuing message reception, because without sync code or other detection taking place the received data would be deemed to have many errors.

Extended Reset

When $\overline{RST}$ goes LOW for 1 to 2 ms or longer, BS1 and BS3 together go HIGH. Approximately 1 to 2 ms after $\overline{RST}$ goes HIGH, device operation continues. This function is useful for checking the RF stage circuits. After $\overline{RST}$ goes HIGH, the device waits for the ID code input.

When $\overline{RST}$ is LOW for less than 200 ms

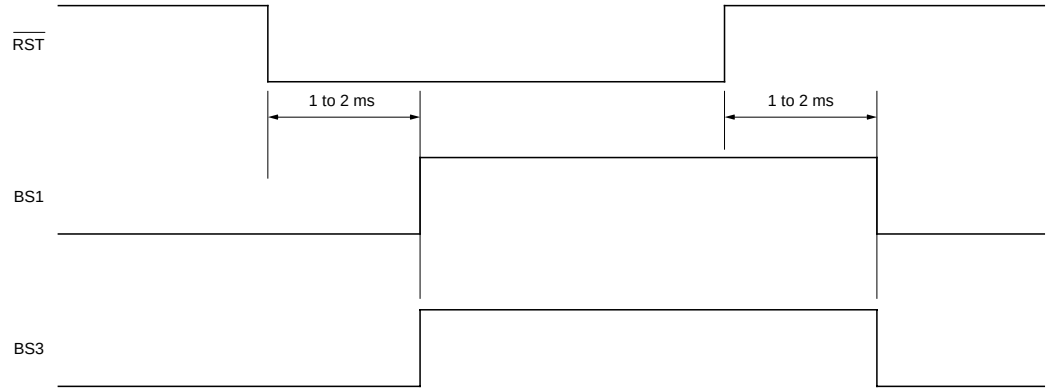


Figure 10. Extended reset timing

When $\overline{RST}$ is LOW for more than 200 ms

If the $\overline{RST}$ LOW-level pulsewidth exceeds 200 ms, the parameters for switch-ON mode should be quickly set over again as soon as $\overline{RST}$ returns HIGH.

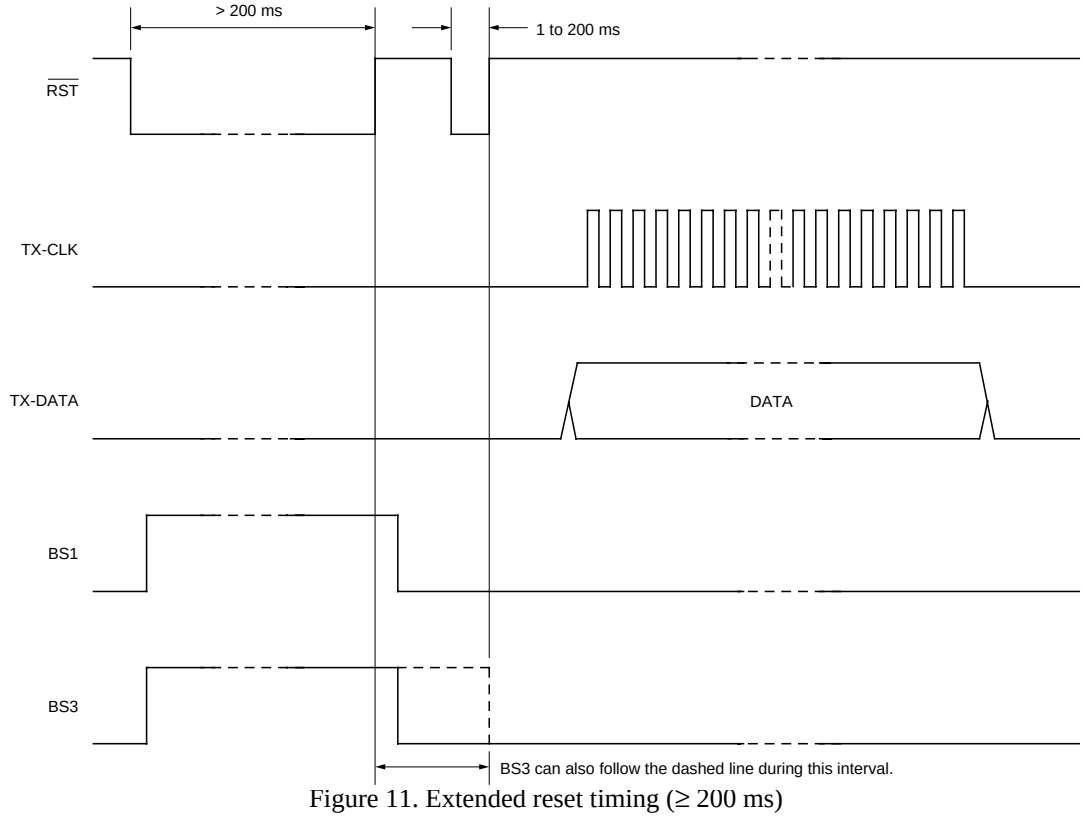


Figure 11. Extended reset timing (≥ 200 ms)

For internal oscillator operation, $\overline{RST}$ goes LOW for 1 ms or longer immediately after power is applied or just after a $\overline{BACKUP}$ release. After $\overline{RST}$ returns HIGH, a wait time of approximately 900 ms (V_{DD} = 1.5 to 3.5 V) or 1.5 s (V_{DD} < 1.5 V) should be observed before operation starts.

Power Save Control

When $\overline{\text{BACKUP}}$ goes LOW, the internal operation stops and all outputs go high impedance. When power save mode is released for normal operation, switch-ON mode internal initialization and ID code re-setting is required. The XT clock and TX-CLK timing when $\overline{\text{BACKUP}}$ goes LOW is described below.

TX-DATA loading

During TX-DATA loading, TX-CLK should be maintained and not stopped until the ID code is read in.

Also, the XT clock should be maintained until after the equivalent time of 1 bit after the ID code is read in (150 cycles at 512 bps and 64 cycles at 1200 bps).

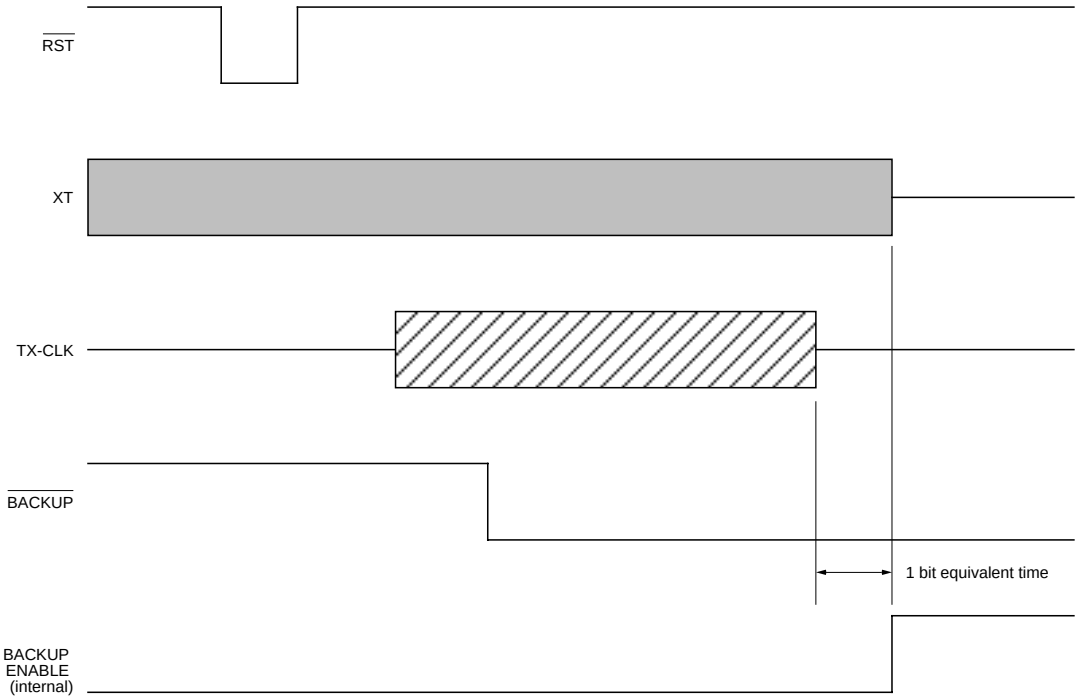


Figure 12. TX-DATA load timing

TX-DATA when not loading

After $\overline{\text{BACKUP}}$ has gone LOW, the XT clock should be maintained for the equivalent time of 65 bits or longer.

Input Signal Digital Processing (Digital Filter)

In pagers, two baud rates, 512 and 1200 bps, are in use. The current method of ensuring the most suitable reception conditions is to substitute RF-stage LPF constants that are proportional to the baud rate.

In the SM8211M, digital processing of the signal input deals with both baud rates without substituting RF-stage LPF constants. With this digital processing, a particularly small rise in the rate error probability can be expected.

The digital processing can be set ON or OFF using flag FL2, and when ON, there are four filter constant settings that can be set using flags FL0 and FL1 to obtain the most suitable reception conditions in a flexible manner. (See table 12.)

System Clock

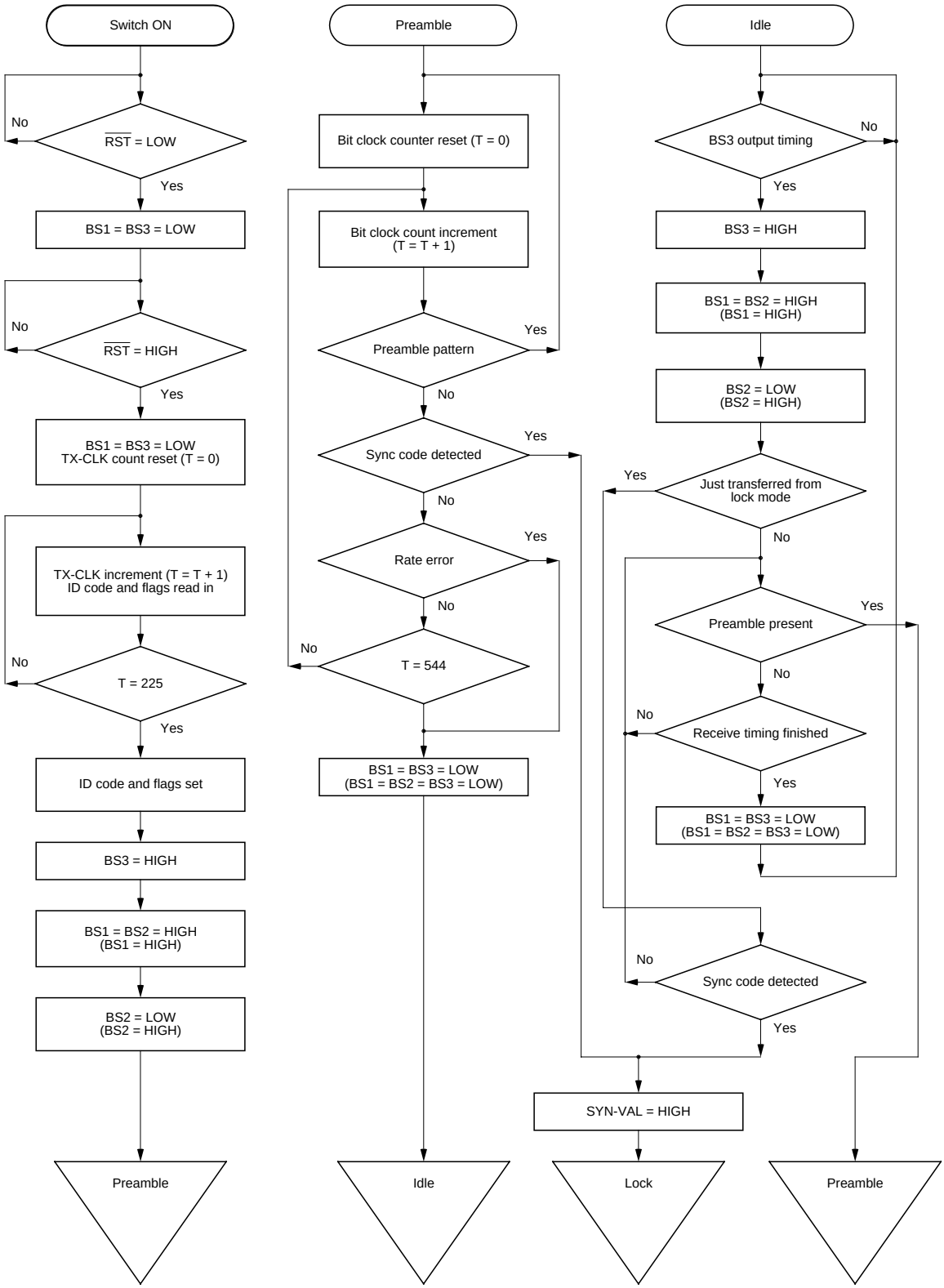
The SM8211M operates using a 76.8 or 153.6 kHz system clock. The clock can be set up using a crystal oscillator or an externally input clock.

For crystal oscillator clocks, only a crystal needs to be connected between XT and XTN. The oscillator amplifier, feedback resistor and oscillator capacitor are all built-in.

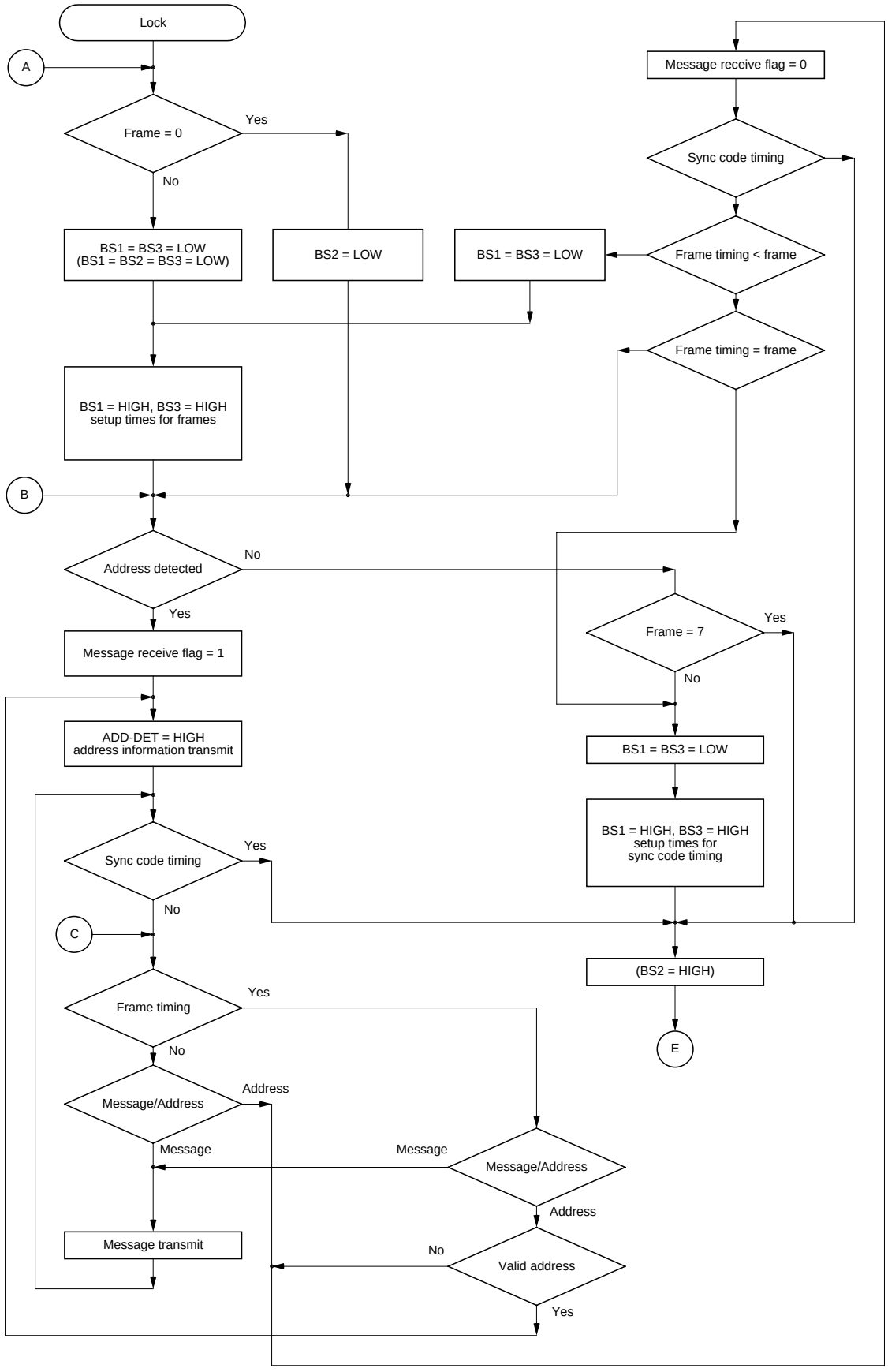
For externally input clocks, the clock is connected to XT through a 100 pF to 0.1 μF coupling capacitor.

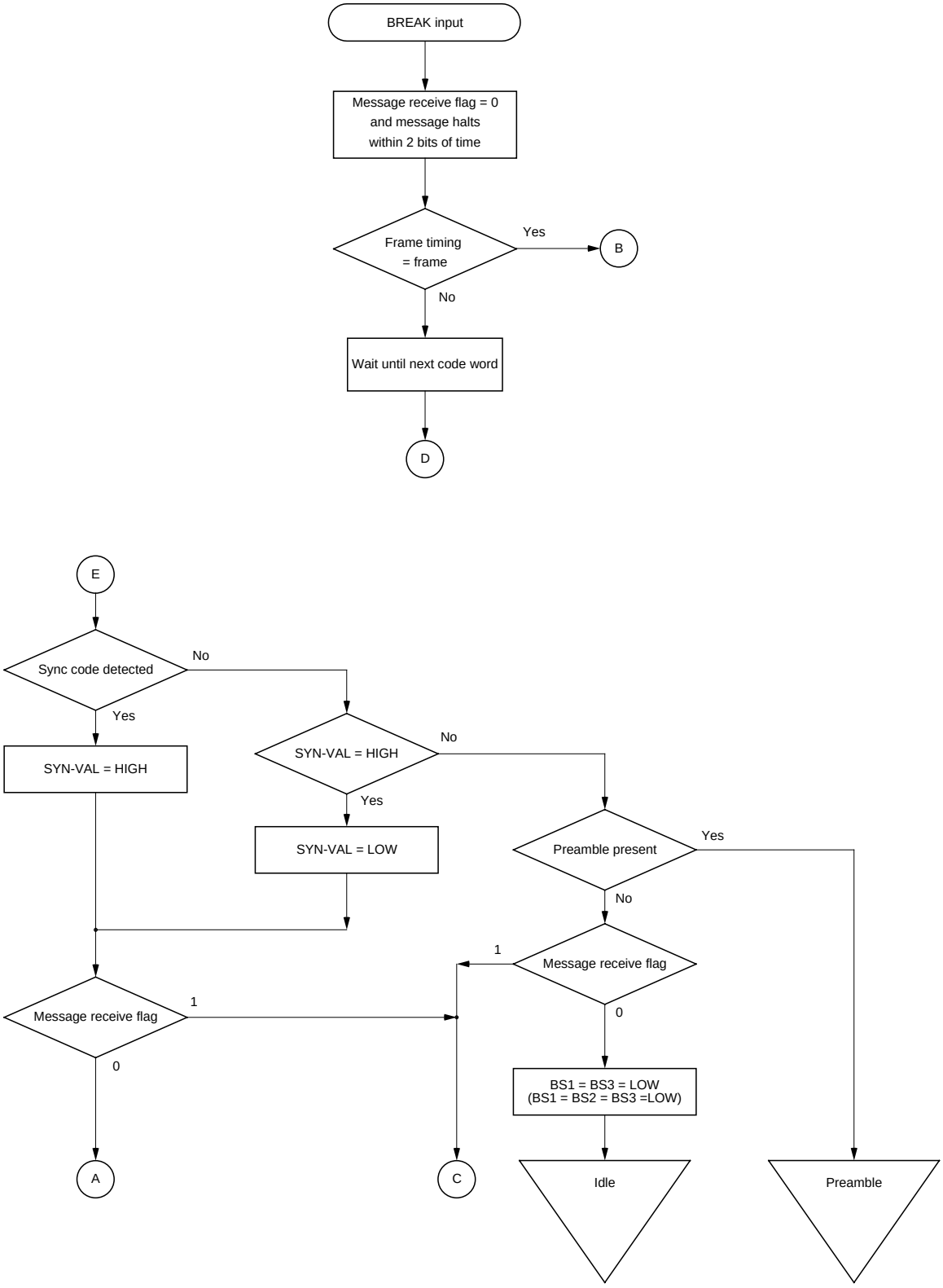
In both cases, crystal oscillator and external clock, a supply decoupling capacitor of 1000 pF to 0.1 μF should be connected between XVDD and VSS. Also, the output on XTN should not be used as a clock to drive an external device.

FLOWCHARTS



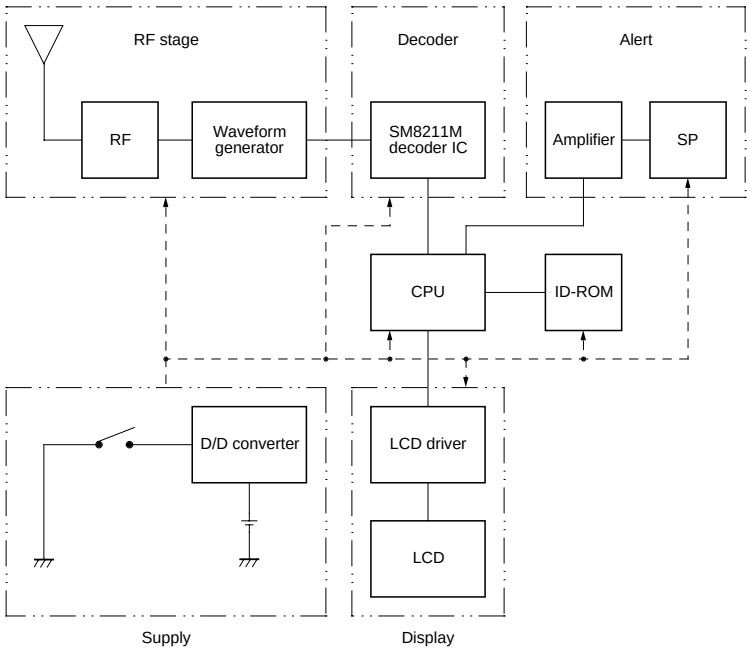
Parentheses indicate operation with flag BS2 = 1.


Lock
A
Frame = 0
Yes
No
BS1 = BS3 = LOW
(BS1 = BS2 = BS3 = LOW)
BS2 = LOW
BS1 = BS3 = LOW
BS1 = HIGH, BS3 = HIGH
setup times for frames
B
Address detected
No
Yes
Message receive flag = 1
ADD-DET = HIGH
address information transmit
Sync code timing
Yes
No
C
Frame timing
Yes
No
Message/Address
Address
Message
Message transmit
Message receive flag = 0
Sync code timing
Frame timing < frame
Frame timing = frame
Frame = 7
Yes
No
BS1 = BS3 = LOW
BS1 = HIGH, BS3 = HIGH
setup times for
sync code timing
(BS2 = HIGH)
E
Message
Message/Address
Address
No
Valid address
Yes


BREAK input
Message receive flag = 0
and message halts
within 2 bits of time
Frame timing
= frame
Yes
B
No
Wait until next code word
D
E
Sync code detected
No
Yes
SYN-VAL = HIGH
SYN-VAL = HIGH
No
Yes
SYN-VAL = LOW
Preamble present
Yes
No
Message receive flag
1
0
Message receive flag
1
0
BS1 = BS3 = LOW
(BS1 = BS2 = BS3 =LOW)
A
C
Idle
Preamble

TYPICAL APPLICATIONS

Paging Receiver System



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