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NTE2117
Integrated Circuit
16K Dynamic Random Access Memory (RAM)

Description:

The NTE2117 is a new generation MOS dynamic random access memory circuit in a 16–Lead DIP type package organized as 16,384 x 1–bit and incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving higher performance levels in both speed and power.

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize “false triggering” of the inputs (a common cause of soft errors), on–chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of the memory system. The NTE2117 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read–modify–write cycles, this device is capable of delayed write cycles, page–mode operation, and $\overline{\text{RAS}}$–Only refresh. Proper control of the clock inputs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WRITE}}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

Features:

- Fast Access Time: 200ns, 375ns cycle
- ±10% Tolerance on All Power Supplies (+12V, ±5V)
- Low Power: 462mW Active, 20W Standby (Max)
- Output Data Controlled bt $\overline{\text{CAS}}$ and Unlatched at End of Cycle to Allow Two Dimensional Chip Selection and Extended Page Boundary.
- Common I/O Capability using “Early Write” Operation
- Read–Modify–Write, $\overline{\text{RAS}}$–Only Refresh, and Page–Mode Capability
- All Inputs TTL Compatible, Low Capacitance, and Protected Against Static Charge
- 128 Refresh Cycles
- ECL Compatible on V_{BB} Power Supply (–5.7V)

Absolute Maximum Ratings: (Note 1)

Voltage on Any Pin Relative to V_{BB} . . . . . –0.5V to +20V
Voltage on V_{DD}, V_{CC} Supplies Relative to V_{SS} . . . . . –1V to +15V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SWS} > 0V$) 0V
Ambient Operating Temperature, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C
Short–Circuit Output Current 50mA
Power Dissipation, P_D 1W

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation Conditions: ($0° \le T_A \le +70°C$, Note 2, Note 3 unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	10.8	12.0	13.2	V
	V_{CC} (Note 4)	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
	V_{BB}	–4.5	–5.0	–5.7	V
Input High (Logic “1”) Voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	V_{IHC}	2.4	–	7.0	V
Input High (Logic “1”) Voltage (All Other Inputs)	V_{IH}	2.2	–	7.0	V
Input Low (Logic “0”) Voltage (All Inputs)	V_{IL}	–1.0	–	0.8	V

Note 2. Several cycles are required after power–up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Note 3. All voltages referenced to V_{SS}.

Note 4. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

DC Electrical Characteristics: ($0° \le T_A \le +70°C$, V_{DD} = 12V ±10%, V_{CC} = 5V Δ10%, V_{SS} = 0, $-5.7V \le V_{BB} \le -4.5V$ unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Average Power Supply Operating Current	I_{DD1}	$\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ Min	Note 5	–	–	35	mA
	I_{CC1}		Note 6				
	I_{BB1}			–	–	200	μA
Power Supply Standby Current	I_{DD2}	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance		–	–	1.5	mA
	I_{CC2}			–10	–	+10	μA
	I_{BB2}			–	–	100	μA
Average Power Supply Current, Refresh Mode	I_{DD3}	$\overline{RAS}$ Cycling, $\overline{RAS} = V_{IHC}$, $t_{RC} = t_{RC}$ Min	Note 5	–	–	25	mA
	I_{CC3}			–10	–	+10	μA
	I_{BB3}			–	–	200	μA
Average Power Supply Current, Page–Mode	I_{DD4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling, $t_{PC} = t_{PC}$ Min	Note 5	–	–	27	mA
	I_{CC4}		Note 6				
	I_{BB4}			–	–	200	μA
Input Leakage Current (Any Input)	$I_{I(L)}$	$V_{BB} = -5V$, $0V \le V_{IN} \le +7V$, all other pins not under test = 0V		–10	–	+10	μA
Output Leakage Current	$I_{O(L)}$	D_{OUT} is disabled, $0V \le V_{OUT} \le +5.5V$		–10	–	+10	μA
Output High (Logic “1”) Voltage	V_{OH}	$I_{OUT} = -5mA$		2.4	–	–	V
Output Low (Logic “0”) Voltage	V_{OL}	$I_{OUT} = 4.2mA$		–	–	0.4	V

Note 5. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 6. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω Typ) to data out. At all other times I_{CC} consists of leakage currents only.

Electrical Characteristics and Recommended AC Operating Conditions: ($0°C \le T_A \le +70°C$, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{SS} = 0V, $-5.7V \le V_{BB} \le -4.5V$, Note 2, Note 7, Note 8, Note 9 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Random Read or Write Cycle Time	t_{RC}	Note 10	375	–	–	ns
Read–Write Cycle Time	t_{RWC}	Note 10	375	–	–	ns
Read–Modify–Write Cycle Time	t_{RMW}	Note 10	405	–	–	ns
Page Mode Cycle Time	t_{PC}	Note 10	225	–	–	ns
Access Time from $\overline{RAS}$	t_{RAC}	Note 11, Note 13	–	–	200	ns
Access Time from $\overline{CAS}$	t_{CAC}	Note 12, Note 13	–	–	135	ns
Output Buffer Turn–Off Delay	t_{OFF}	Note 14	0	–	50	ns
Transition Time (Rise and Fall)	t_T	Note 9	3	–	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}		120	–	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}		200	–	10,000	ns
$\overline{RAS}$ Hold Time	t_{RSH}		135	–	–	ns
$\overline{CAS}$ Hold Time	t_{CSH}		200	–	–	ns
$\overline{CAS}$ Pulse Width	t_{CAS}		135	–	10,000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	Note 15	25	–	65	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}		–20	–	–	ns
Row Address Set–Up Time	t_{ASR}		0	–	–	ns
Row Address Hold Time	t_{RAH}		25	–	–	ns
Column Address Set–Up Time	t_{ASC}		–10	–	–	ns
Column Address Hold Time	t_{CAH}		55	–	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}		120	–	–	ns
Read Command Set–Up Time	t_{RCS}		0	–	–	ns
Read Command Hold Time	t_{RCH}		0	–	–	ns
Write Command Hold Time	t_{WCH}		55	–	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}		120	–	–	ns
Write Command Pulse Width	t_{WP}		55	–	–	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}		70	–	–	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}		70	–	–	ns
Data–In Set–Up Time	t_{DS}	Note 16	0	–	–	ns
Data–In Hold Time	t_{DH}	Note 16	55	–	–	ns
Data–In Hold Time Referenced to $\overline{RAS}$	t_{DHR}		120	–	–	ns
$\overline{CAS}$ Precharge Time (for Page–Mode Cycle Only)	t_{CP}		80	–	–	ns
Refresh Period	t_{REF}		–	–	2	ms
$\overline{WRITE}$ Command Set–Up Time	t_{WCS}	Note 17	–20	–	–	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	Note 17	80	–	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	Note 17	145	–	–	ns

Note 7. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

Note 8. AC measurements assume t_T = 5ns.

Note 9. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

Note 10. The specifications for t_{RC}(min), t_{RMW}(min), and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq +70°C$) is assured.

Note 11. Assumes that $t_{RCD} \leq t_{RCD}$(Max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

Note 12. Assumes that t_{RCD}(max).

Note 13. Measured with a load equivalent to 2 TTL loads and 100pF.

Note 14. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Note 15. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

Note 16. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read–modify–write cycles.

Note 17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read–write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

AC Electrical Characteristics: ($0°C \leq T_A \leq +70°C$, V_{DD} = 12V ±10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance ($A_0 - A_6$), D_{IN}	C_{I1}	Note 18	$C = \frac{\Delta t}{\Delta V}$	4	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	Note 18		8	10	pF
Output Capacitance (D_{OUT})	C_O	Note 18, Note 19	–	5	7	pF

Note 18. Effective capacitance calculated from the equation:

ΔV with Δ = 3V and
power supplies at nominal levels.

Note 19. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

Pin Connection Diagram