ASX340AT

VGA, 1/4" SOC with 5.6µm Pixel
Aptina DR-PIX™ technology
Dynamic Overlays
iBGA 7.5x7.5mm Package

High Performance Automotive System-On-Chip (SOC) Imager

Excellent Low-Light Performance
Enhanced pixel performance offers the driver greater visibility and awareness under minimal light conditions

DR-PIX™ Technology
Aptina's dynamic response pixel technology for increased sensitivity and low noise

On-Chip Image Flow Processor
Includes color correction, defect correction, auto white balancing, sharpening and auto exposure functions

Dynamic Overlays
Up to 4 overlays to provide colored graphics in the display to visually aid the driver when backing into a parking space

Digital Zoom and Pan
Allows customization of the image to suit a wide range of vehicle body designs

Additional Optical Alignment Pixels
Offers customers ease of lens alignment to sensor during camera assembly leading to cost savings

Applications

Automotive Viewing Applications:
- Rear View
- Surround View
- Blind Spot Detection

How to Buy

Production and sample quantities of Aptina products may be ordered through qualified distributors. See our Web site for details. You may also request access to NDA data sheets and other technical documentation by visiting our Web site.

Aptina™ IMAGING

ASX340AT

Features

- System-On-Chip (SOC) provides integrated camera system
- Dynamic Response Pixel Technology DR-PiX™ for increased sensitivity and low read noise allows increased flexibility for imaging of challenging scenes.
- 2x upscaling zoom and pan control
- ±40 additional columns and ±36 additional rows to compensate for lens alignment tolerances
- Overlay generator for dynamic bitmap overlay
- Integrated video encoder for NTSC/PAL with overlay capability and 10-bit I-DAC
- On-chip image flow processor performs sophisticated processing, such as color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, auto white balancing, and auto exposure
- 10-bit, on-chip analog-to-digital converter (ADC)
- Internal master clock generated by on-chip phase-locked loop (PLL)
- Two-wire serial programming interface
- Interface to low-cost EEPROM and Flash through SPI bus for settings and overlay storage
- Comprehensive tool support for overlay generation and lens correction setup
- Temperature Sensor allows for control and protection of the camera system in excessive temperature conditions
- AEC-Q100 Qualified with operating temperature -40°C to +105°C

Specifications

Imaging Array
- Optical Format: 1/4-inch
- Active Array: 640 (H) x 480 (V)

Speed/Output
- Frame Rate: Up to 60 fps
- Data Rate: 27 MB/s
- Digital Data Formats: Raw Bayer 8-bit, 10-bit, CCIR656, 565RGB, 555RGB, 444RGB

Pixel
- Pixel Size: 5.6µm x 5.6µm
- Dynamic Range: 74.8dB
- Responsivity: 16.5V/lux-s at 550nm

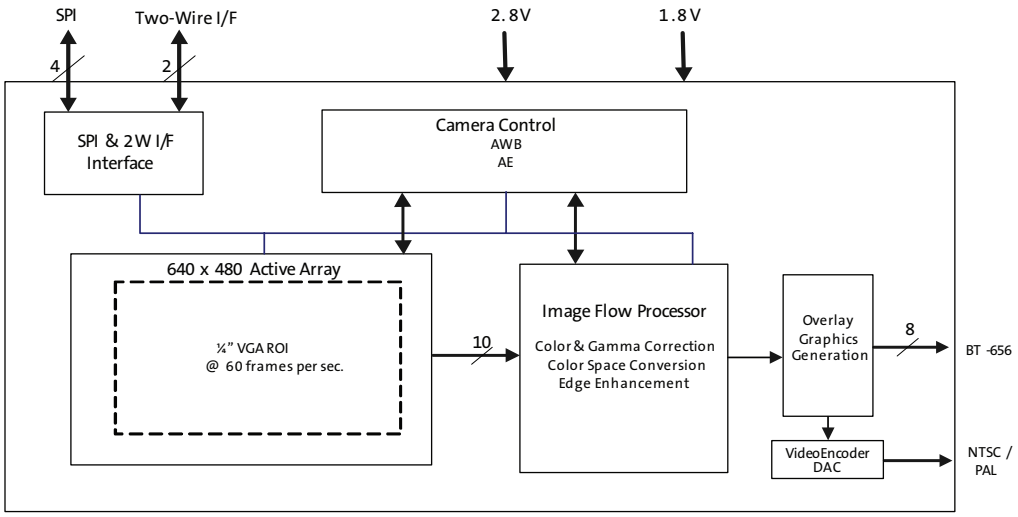
Gain
- Analog: 0.5–8x

Supply Voltage
- Analog: 2.8V +-5%
- Core: 1.8V +-5%
- I/O: 2.8V +-5%

Temperature Range
- Operating: -40°C to +105°C
- Functional: -40°C to +85°C
- Storage: -50°C to +150°C

Package
- 63-BGA, 7.5 mm x 7.5 mm, 0.65mm ball pitch

Block Diagram



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