HT1647A

64×16 LCD Controller for I/O MCU

PATENTED

PAT No. : 099352

Technical Document

- Application Note

Features

- Operating voltage: 2.7V~5.2V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal oscillator or 32kHz frequency source input
- Standby current: <1μA at 3V, <2μA at 5V
- Internal resistor type: 1/5 bias or 1/4 bias, 1/16 duty
- Two selectable LCD frame frequencies: 89Hz or 170Hz
- Max. 64×16 patterns, 64 segments and 16 commons
- Built-in bit-map display RAM: 1024 bits (=64×16 bits)
- Built-in internal resistor type bias generator
- Six-wire interface (four data wires)
- Eight kinds of time base/WDT selection
- Time base or WDT overflow output
- R/W address auto increment
- Built-in buzzer driver (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provides VLCD pin to adjust LCD operating voltage
- Provides three kinds of bias current programming
- Control of TN-type, STN-type LCDs and ECB-type LCDs
- 100-pin QFP package and in chip form

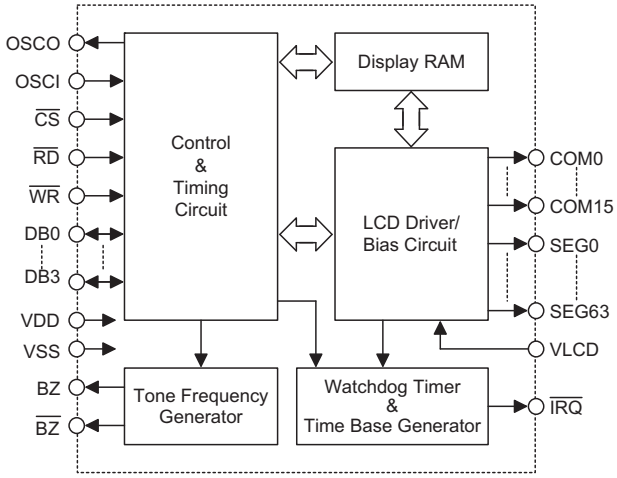
Applications

- Leisure products
- Games
- Personal digital assistant
- Cellular phone
- Global positioning system
- Consumer electronics

General Description

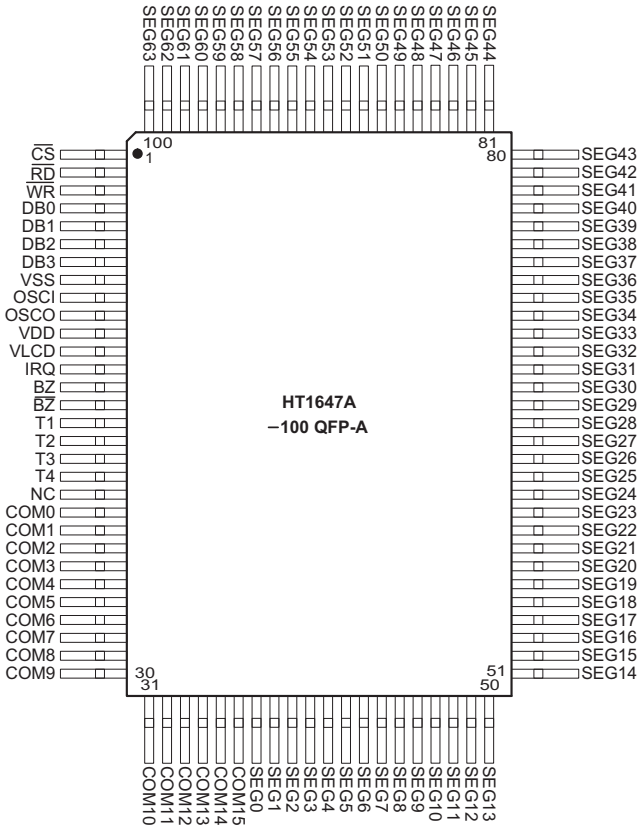
HT1647A is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 1024 patterns (64 segments and 16 commons). It also supports four data bits interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1647A is a memory mapping and multi-function LCD controller. Since the HT1647A can control ECB-type (Electrically Controlled Birefringence) LCDs in addition to current TN-type (Twisted Nematic) or STN-type (Super Twisted Nematic) LCDs. The software configuration feature of the HT1647A make it suitable for multiple LCD applications including LCD modules and display subsystems. Only six lines ($\overline{CS}$, $\overline{WR}$, DB0~DB3) are required for the interface between the host controller and the HT1647A.

Block Diagram

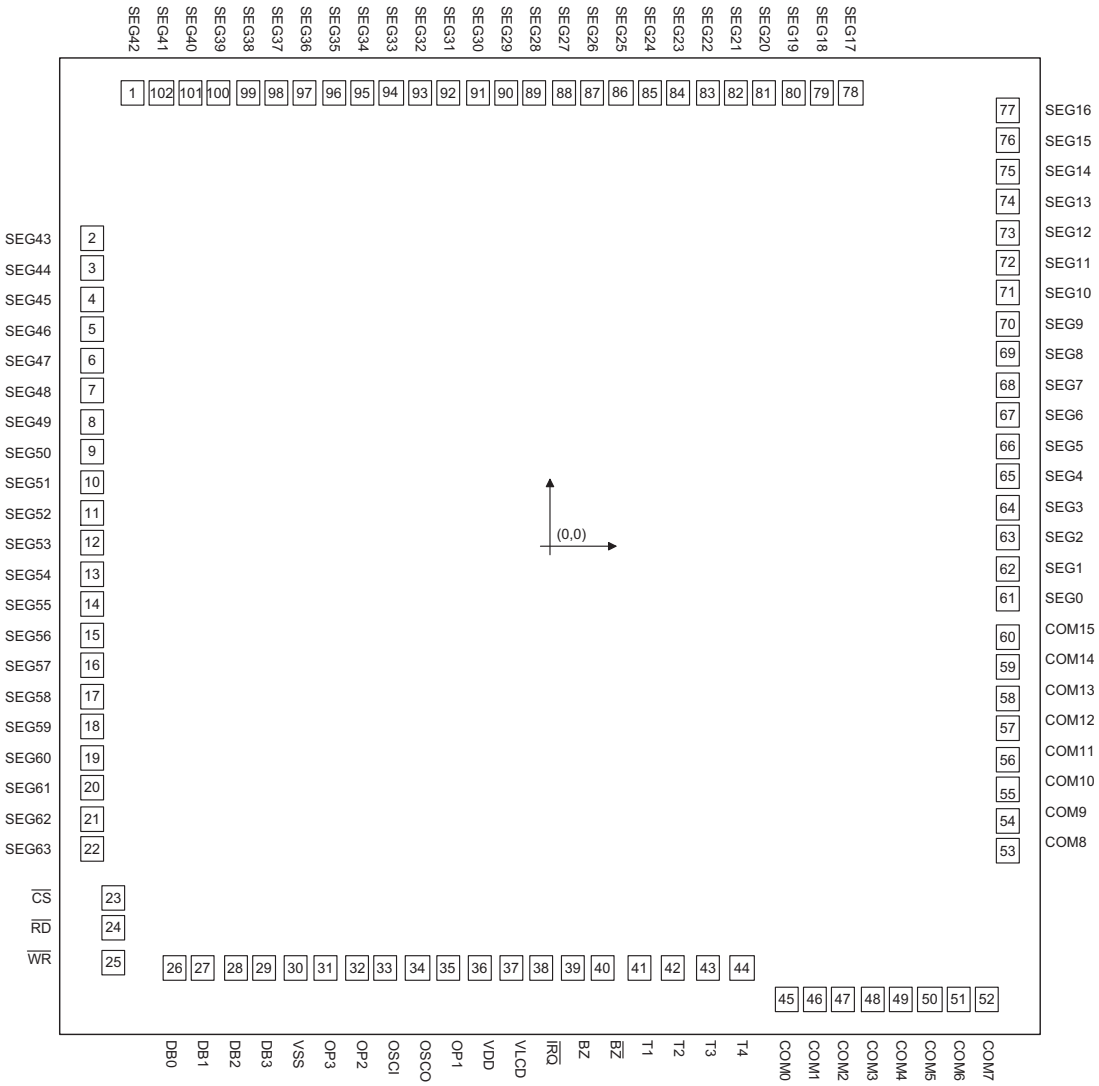


Note: CS: Chip selection
BZ, BZ: Tone outputs
WR, RD: WRITE clock, READ clock
DB0~DB3: Data bus
COM0~COM15, SEG0~SEG63: LCD outputs
IRQ: Time base or WDT overflow output

Pin Assignment



Pad Assignment



Chip size: 3255 × 3050 (μm)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	−1379.40	1407.45	35	−336.80	−1310.40	69	1512.50	593.85
2	−1512.50	956.25	36	−233.40	−1310.40	70	1512.50	688.85
3	−1512.50	861.25	37	−125.00	−1310.40	71	1512.50	783.85
4	−1512.50	766.25	38	−28.00	−1310.40	72	1512.50	878.85
5	−1512.50	671.25	39	77.60	−1310.40	73	1512.50	973.85
6	−1512.50	576.25	40	172.60	−1310.40	74	1512.50	1068.85
7	−1512.50	481.25	41	295.20	−1310.40	75	1512.50	1163.85
8	−1512.50	386.25	42	408.80	−1310.40	76	1512.50	1258.85
9	−1512.50	291.25	43	522.40	−1310.40	77	1512.50	1353.85
10	−1512.50	196.25	44	636.00	−1310.40	78	995.60	1407.45

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
11	–1512.50	101.25	45	781.30	–1410.00	79	900.60	1407.45
12	–1512.50	6.25	46	876.30	–1410.00	80	805.60	1407.45
13	–1512.50	–88.75	47	971.30	–1410.00	81	710.60	1407.45
14	–1512.50	–183.75	48	1066.30	–1410.00	82	615.60	1407.45
15	–1512.50	–278.75	49	1161.30	–1410.00	83	520.60	1407.45
16	–1512.50	–373.75	50	1256.30	–1410.00	84	425.60	1407.45
17	–1512.50	–468.75	51	1351.30	–1410.00	85	330.60	1407.45
18	–1512.50	–563.75	52	1446.30	–1410.00	86	235.60	1407.45
19	–1512.50	–658.75	53	1512.50	–949.55	87	140.60	1407.45
20	–1512.50	–753.75	54	1512.50	–845.55	88	45.60	1407.45
21	–1512.50	–848.75	55	1512.50	–759.55	89	–49.40	1407.45
22	–1512.50	–943.75	56	1512.50	–664.55	90	–144.40	1407.45
23	–1441.90	–1095.00	57	1512.50	–569.55	91	–239.40	1407.45
24	–1441.90	–1190.00	58	1512.50	–474.55	92	–334.40	1407.45
25	–1441.90	–1295.60	59	1512.50	–379.55	93	–429.40	1407.45
26	–1240.80	–1310.40	60	1512.50	–284.55	94	–524.40	1407.45
27	–1145.80	–1310.40	61	1512.50	–166.15	95	–619.40	1407.45
28	–1040.20	–1310.40	62	1512.50	–71.15	96	–714.40	1407.45
29	–945.20	–1310.40	63	1512.50	23.85	97	–809.40	1407.45
30	–842.00	–1310.40	64	1512.50	118.85	98	–904.40	1407.45
31	–743.30	–1310.40	65	1512.50	213.85	99	–999.40	1407.45
32	–637.70	–1310.40	66	1512.50	308.85	100	–1094.40	1407.45
33	–542.70	–1310.40	67	1512.50	403.85	101	–1189.40	1407.45
34	–437.10	–1310.40	68	1512.50	498.85	102	–1284.40	1407.45

Pad Description

Pad No.	Pad Name	I/O	Description
23	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1647A are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1647A are all enabled.
24	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1647A are clocked out on the rising edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
25	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1647A on the rising edge of the $\overline{WR}$ signal.
26~29	DB0~DB3	I/O	Parallel data input/output with a pull-high resistor
30	VSS	—	Negative power supply for logic circuit, ground
31	OP1	I	Used to select D3, D1 or D2, D0; OP1 input with pull-low resistor.
32	OP2	I	OP2 and OP3 are used to select two of four level gray scale; OP2 input with pull-high resistor.
33	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected, the OSCI and OSCO pads can be left open.
34	OSCO	O	
35	OP3	I	OP2 and OP3 are used to select two of four level gray scale ; OP3 input with pull-high resistor.

Pad No.	Pad Name	I/O	Description
36	VDD	—	Positive power supply for logic circuit
37	VLCD	I	Power supply for LCD driver circuit
38	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
39, 40	BZ, $\overline{BZ}$	O	2kHz or 4kHz frequency output pair (tristate output buffer)
41~44	T1~T4	I	Not connected
45~60	COM0~COM15	O	LCD common outputs
61~102, 1~22	SEG0~SEG63	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+5.5V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	250	μA
		5V		—	250	370	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	135	200	μA
		5V		—	200	300	μA
I_{DD11}	Operating Current	3V	No load/LCD OFF On-chip RC oscillator	—	15	30	μA
		5V		—	50	70	μA
I_{DD22}	Operating Current	3V	No load/LCD OFF Crystal oscillator	—	2	10	μA
		5V		—	3	10	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	—	1	μA
		5V		—	—	2	μA
V_{IL}	Input Low Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$ Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH1}	BZ, $\overline{BZ}$ Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OL2}	DB0~DB3 Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH2}	DB0~DB3 Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA
I_{OL3}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL4}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH4}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH1}	Pull-high Resistor	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	150	250	410	kΩ
		5V		60	125	210	kΩ
R_{PH2}	Pull-high Resistor	3V	OP2, OP3	150	250	410	kΩ
		5V		60	125	210	kΩ
R_{PL}	Pull-low Resistor	3V	OP1	150	250	410	kΩ
		5V		60	125	210	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	22	32	40	kHz
		5V		24	32	40	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	32	—	kHz
		5V		—	32	—	kHz
f_{LCD1}	LCD Frame Frequency	3V	On-chip RC oscillator	61/117	89/170	111/213	Hz
		5V		61/117	89/170	111/213	Hz
f_{LCD2}	LCD Frame Frequency	3V	Crystal oscillator	—	64	—	Hz
		5V		—	64	—	Hz
f_{LCD3}	LCD Frame Frequency	3V	External clock source	—	64	—	Hz
		5V		—	64	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	4-Bit Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{CLK2}	4-Bit Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	4-Bit Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34			
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{OFF}	V_{DD} OFF Times (Figure 4)	—	VDD drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 4)	—	—	0.05	—	—	V/ms

Note: 1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.
2. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

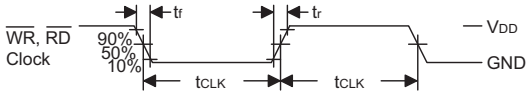


Figure 1

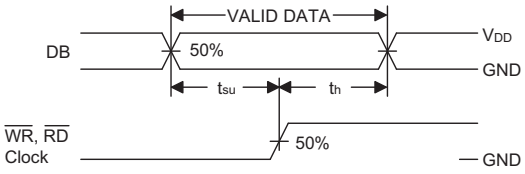


Figure 2

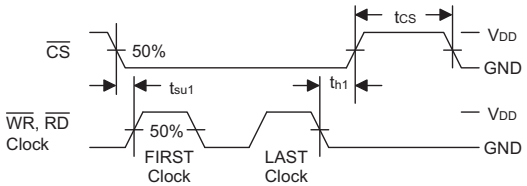


Figure 3

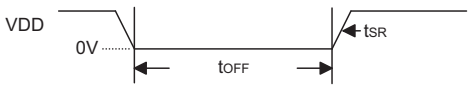


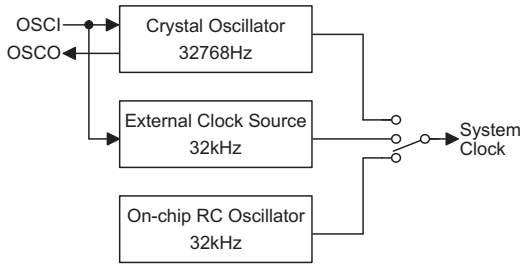
Figure 4. Power-on Reset Timing

Functional Description

System Oscillator

The HT1647A system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The clock source may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 32kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT loses its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, thus serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 32kHz clock source operation. At the initial system power on, the HT1647A is at the SYS DIS state.



System Oscillator Configuration

Display Memory – RAM Structure

The static display RAM is organized into 512×2 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	000H	**008H**	**010H ----------1E8H**	**1F0H**	**1F8H**
COM0	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM1	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	001H	**009H**	**011H ----------1E9H**	**1F1H**	**1F9H**
COM2	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM3	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	002H	**00AH**	**012H ----------1EAH**	**1F2H**	**1FAH**
COM4	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM5	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	003H	**00BH**	**013H ----------1EBH**	**1F3H**	**1FBH**
COM6	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM7	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	004H	**00CH**	**014H ----------1ECH**	**1F4H**	**1FCH**
COM8	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM9	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	005H	**00DH**	**015H ----------1EDH**	**1F5H**	**1FDH**
COM10	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM11	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	006H	**00EH**	**016H ----------1EEH**	**1F6H**	**1FEH**
COM12	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM13	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	007H	**00FH**	**017H ----------1EFH**	**1F7H**	**1FFH**
COM14	D0 or D1	D0 or D1		D0 or D1	D0 or D1
COM15	D2 or D3	D2 or D3		D2 or D3	D2 or D3
	SEG0	**SEG1**	**SEG2 ---------- SEG61**	**SEG62**	**SEG63**

Note: One bit of RAM maps to LCD's one pixel and decide 2-level gray scale.
RAM structure depends on OP1, OP2 and OP3 option.

Write Data Mapping to RAM for Pad Option

Pad Option			Level Selected	RAM Data	Note
OP1	OP2	OP3			
0 (Select D2 and D0)	0	0	Level2 (1,0)	0	Level1 and Level4 are not used
			Level3 (0,1)	1	
	0	1	Level4 (0,0)	0	Level1 and Level2 are not used
			Level3 (0,1)	1	
	1	0	Level2 (1,0)	0	Level3 and Level4 are not used
			Level1 (1,1)	1	
	1	1	Level4 (0,0)	0	Level2 and Level3 are not used
			Level1 (1,1)	1	
1 (Select D3 and D1)	0	0	Level3 (0,1)	0	Level1 and Level4 are not used
			Level2 (1,0)	1	
	0	1	Level4 (0,0)	0	Level1 and Level3 are not used
			Level2 (1,0)	1	
	1	0	Level3 (0,1)	0	Level2 and Level4 are not used
			Level1 (1,1)	1	
	1	1	Level4 (0,0)	0	Level2 and Level3 are not used
			Level1 (1,1)	1	

Note: OP1 is used to select D3, D1 or D2, D0.
OP2 and OP3 are used to select two of four level gray scale.
The default value of OP1, OP2 and OP3 are (0,1,1).

Gray Scale Level Decision

HT1647A uses PWM technique to provide gray scale display and only two of four level gray scale can be displayed simultaneously by setting OP1~OP3 pads. OP1 is used to select D3, D1 or D2, D0 and OP2 and OP3 are used to select two of four level gray scale. The four level gray scale are defined below table ″RAM Data Defined Gray Scale Level″. MCU write two bits data and only one bit data is written to internal display RAM. The OP1~OP3 pads setting is shown as following table ″Write Data Mapping to RAM for Pad Option″.

RAM Data Code (D3, D2) or (D1, D0)	Choice Gray Scale Level
(1, 1)	Level 1
(1, 0)	Level 2
(0, 1)	Level 3
(0, 0)	Level 4

RAM Data Defined Gray Scale Level

Frame Frequency

HT1647A provides two kinds of frame frequency option by command code; 89Hz and 170Hz respectively. FRAME 89Hz provides 89Hz frame frequency and active segment signal width can be divided into 24 sections concurrently. FRAME 170Hz provides 170Hz frame frequency and active segment signal width can be divided into 13 sections concurrently. The 24 sections display a particularly gray scale more than the 13 sections by PWM data. The default is FRAME 89Hz.

Gray Scale Display

If the user choose 89Hz frame frequency, a max. of 24 sections can be programmed to suit a satisfactory gray scale in every level. Similarly, if the user choose 170Hz frame frequency, a max. of 13 sections can be programmed to suit a satisfactory gray scale in every level. HT1647A provides 5-bit PWM data to control the length of the section. In other words, a max. Of 24 gray scales are generated by 5-bit binary PWM data. At FRAME 89Hz mode, the HT1647A only provides a max. of 24 adjustable gray scales although 32 is the expressed max. value by 5 bits binary code. When 5 bits binary code value is more than 23, the PWM control circuit uniformly regards 23. To increase PWM data indicates to increase the length of the active segment signal. The varied length of the active segment signal displays varied gray scale in TN-type, STN-type LCDs (refer to table 1). Similarly, it displays varied color in ECB-type LCDs. The color display is derived from ECB-type LCD specification. At FRAME 170Hz mode, the HT1647A only provides a max. of 13 adjustable gray scales although 32 is the expressed max. value by 5 bits binary code. When the 5 bits binary code value is more than 12, the PWM control circuit uniformly regards 12. The user must appoint four kinds of PWM data to four kinds of different gray scale level by commanding PWM data (refer to table 2).

Name	Command Code	Function
FRAME 170Hz	X**100**-0001-1000-XXXX	Select 170Hz frame frequency and active segment signal width can be divided into 13 sections
FRAME 89Hz	X**100**-0001-1101-XXXX	Select 89Hz frame frequency and active segment signal width can be divided into 24 sections

Frame Frequency Selection Command Code

Relationship Table between PWM Data and Gray Scale

Value	5 bits PWM data					PWM (ON width)	Gray Scale
	B4	B3	B2	B1	B0		
0	0	0	0	0	0	0 (0/23)	
1	0	0	0	0	1	1/23	
2	0	0	0	1	0	2/23	
3	0	0	0	1	1	3/23	
4	0	0	1	0	0	4/23	
5	0	0	1	0	1	5/23	
6	0	0	1	1	0	6/23	
7	0	0	1	1	1	7/23	
8	0	1	0	0	0	8/23	
9	0	1	0	0	1	9/23	
10	0	1	0	1	0	10/23	
11	0	1	0	1	1	11/23	
12	0	1	1	0	0	12/23	
13	0	1	1	0	1	13/23	
14	0	1	1	1	0	14/23	
15	0	1	1	1	1	15/23	
16	1	0	0	0	0	16/23	
17	1	0	0	0	1	17/23	
18	1	0	0	1	0	18/23	
19	1	0	0	1	1	19/23	
20	1	0	1	0	0	20/23	
21	1	0	1	0	1	21/23	
22	1	0	1	1	0	22/23	
23	1	0	1	1	1	1 (23/23)	
24	1	1	0	0	0	1 (24/23)	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
31	1	1	1	1	1	1 (31/23)	

Table 1: FRAME 89Hz Mode

Value	5 bits PWM data					PWM (ON width)	Gray Scale
	B4	B3	B2	B1	B0		
0	0	0	0	0	0	0 (0/12)	
1	0	0	0	0	1	1/12	
2	0	0	0	1	0	2/12	
3	0	0	0	1	1	3/12	
4	0	0	1	0	0	4/12	
5	0	0	1	0	1	5/12	
6	0	0	1	1	0	6/12	
7	0	0	1	1	1	7/12	
8	0	1	0	0	0	8/12	
9	0	1	0	0	1	9/12	
10	0	1	0	1	0	10/12	
11	0	1	0	1	1	11/12	
12	0	1	1	0	0	1 (12/12)	
13	0	1	1	0	1	1 (13/12)	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
31	1	1	1	1	1	1 (31/12)	

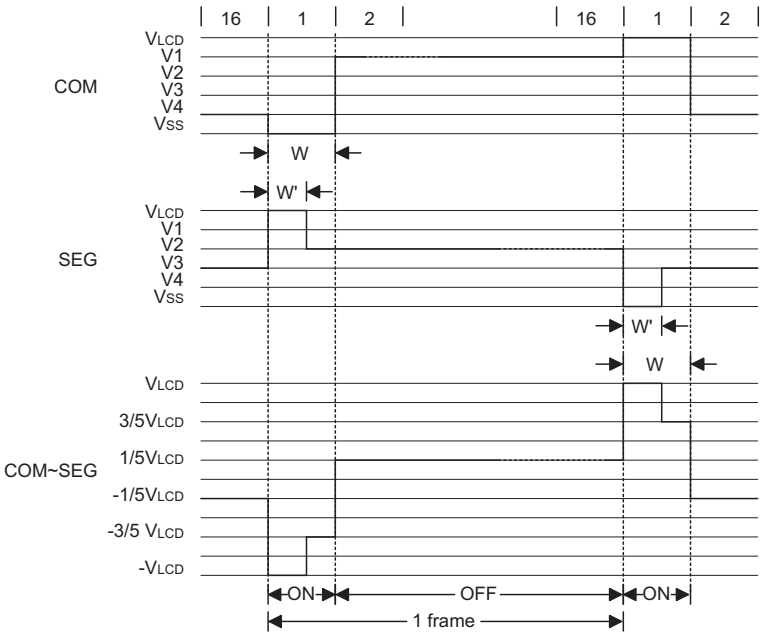
Table 2: FRAME 170Hz Mode

Note: The varied PWM data displays various gray scale in TN-type, STN-type LCDs.

The color display derives from ECB-type LCD's specification.

Name	Command Code	Function
GRS LEVEL 1	X**100**-001 B4-B3 B2 B1 B0-XXXX	Set PWM data in gray scale level 1
GRS LEVEL 2	X**100**-010 B4-B3 B2 B1 B0-XXXX	Set PWM data in gray scale level 2
GRS LEVEL 3	X**100**-011 B4-B3 B2 B1 B0-XXXX	Set PWM data in gray scale level 3
GRS LEVEL 4	X**100**-100 B4-B3 B2 B1 B0-XXXX	Set PWM data in gray scale level 4

Four Kinds of Gray Scale Level Command Code



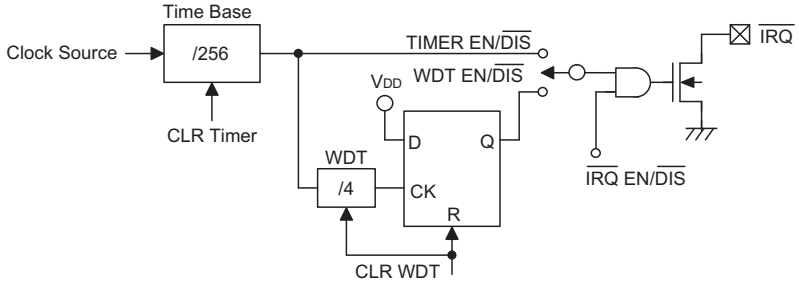
Note: "W"' Real active segment signal width (adjustable width by PWM data)
"W" Max. active segment signal width
PWM (ON width): W'/W, 0≤W'/W≤1 (refer to table 1 & tabel 2)

Example of Waveform (B Type) in 1/5 Bias, 1/16 Duty Cycle Drive

Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same counter which is divided by 256. The $\overline{IRQ}$ clock can be programmed as 1Hz, 2Hz, ..., 128Hz output. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

If an external clock is selected as the system frequency source, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.



Time Base and WDT Configurations

Buzzer Tone Output

A simple tone generator is implemented in the HT1647A. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

By executing the TONE 4K and TONE 2K commands there are two tone frequency outputs selectable that can turn on the tone output. The TONE 4K and TONE 2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned off by invoking the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

Name	Command Code	Function
TONE OFF	**X100**-0000-1000-XXXX	Turn-off tone output
TONE 4K	**X100**-0001-0000-XXXX	Turn-on tone output, tone frequency is 4kHz
TONE 2K	**X100**-0001-0001-XXXX	Turn-on tone output, tone frequency is 2kHz

Buzzer Tone Output Command Code

Command Format

The HT1647A can be configured by software setting. There are two mode commands to configure the HT1647A resource and to transfer the LCD display data.

The configuration mode of the HT1647A is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a bias current selection command, a gray scale level selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode ID and the command mode ID:

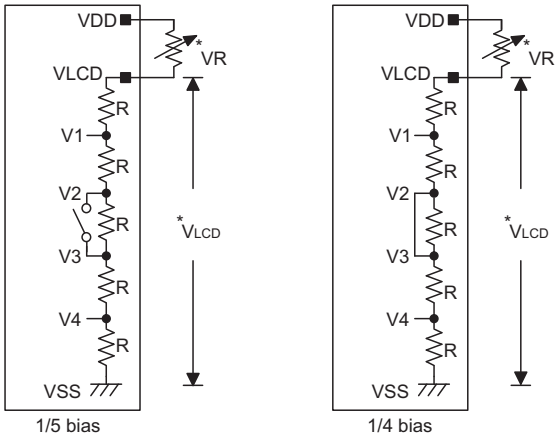
Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to ″1″ and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to ″0″, so a new operation mode ID should be issued first.

Bias Generator

The HT1647A bias voltage belongs to internal resistor type. It provides two kinds of bias option named 1/5 bias and 1/4 bias respectively. It is recommended to select 1/5 bias to fit TN-type, STN-type LCDs and select 1/4 bias to fit ECB-type LCDs. It also provides three kinds of bias current option by programming to suitably drive an LCD panel. The three kinds of bias current are large, middle, and small, respectively. Usually, large panel LCD can be excellently displayed by large bias current. Relatively, it consumes large current when LCD ON command is used. Small bias current provides low power consumption during On condition when the LCD is normally displayed. The following are the reference value table.

V_{LCD}	Bias	Large Bias Current	Middle Bias Current	Small Bias Current
4V	1/5	300μA	100μA	40μA
4V	1/4	375μA	125μA	50μA



* The voltage applied to VLCD pin must be lower than VDD
* Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ±20%

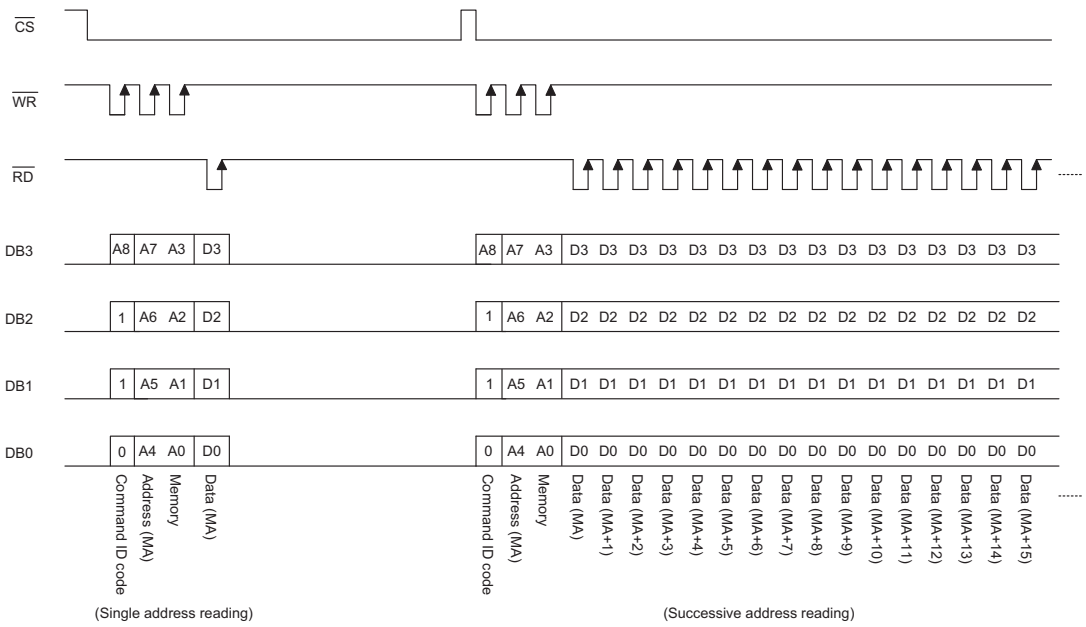
Internal Resistor Type Bias Generator Configurations

Interfacing

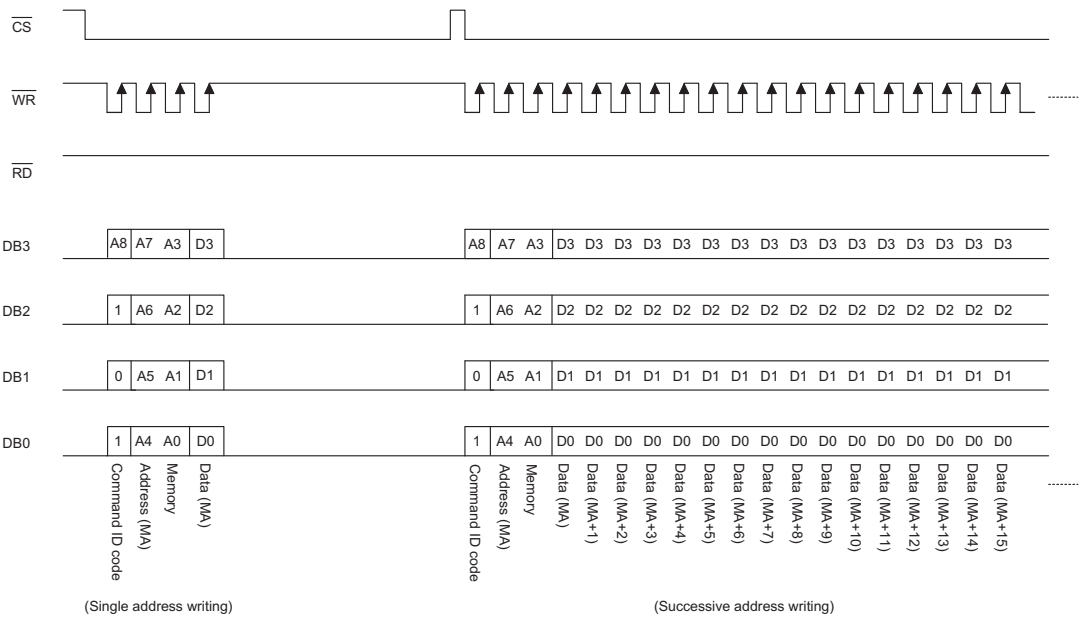
Only six lines are required to interface with the HT1647A. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1647A. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1647A are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1647A. The DB0~DB3 are the 4-bit parallel data input/output lines. Data to be read or written or commands to be written have to pass through the DB0~DB3 lines. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DB0~DB3 lines. It is recommended that the host controller read correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DB0~DB3 lines are all clocked into the HT1647A on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1647A. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the $\overline{IRQ}$ pin of the HT1647A.

Timing Diagrams

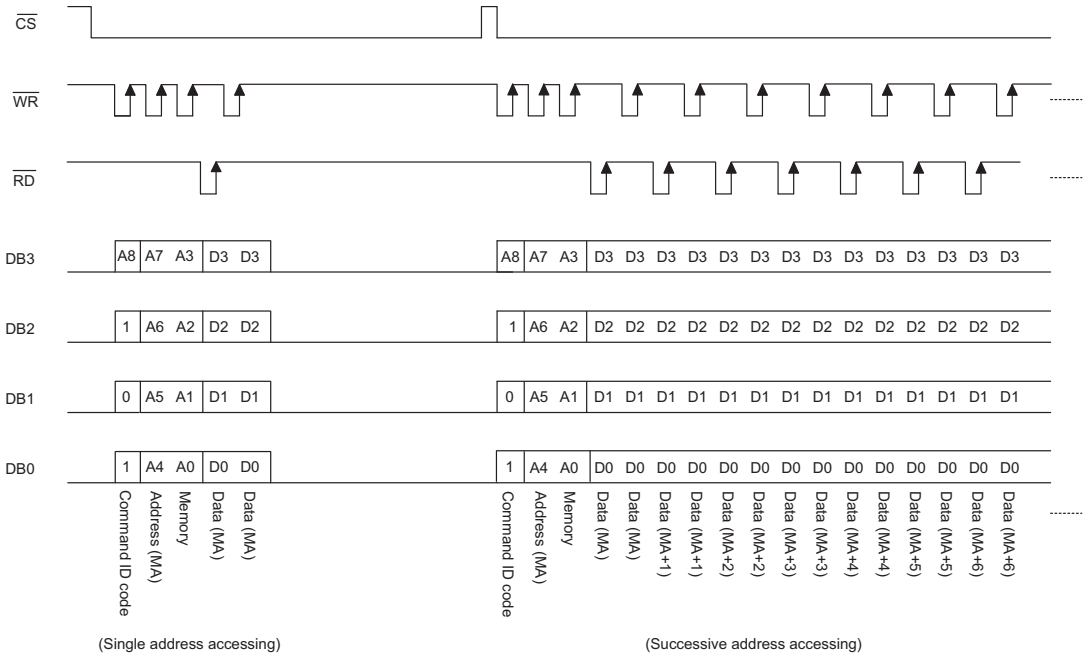
READ mode (command ID code : 1 1 0)



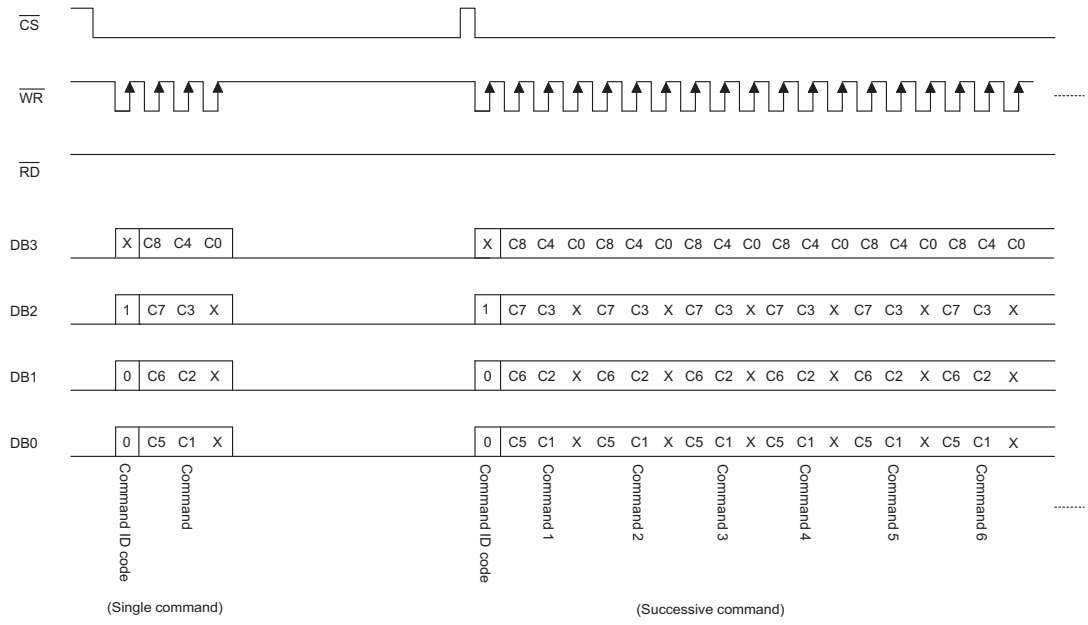
WRITE mode (command ID code : 1 0 1)



READ-MODIFY-WRITE mode (command ID code : 1 0 1)



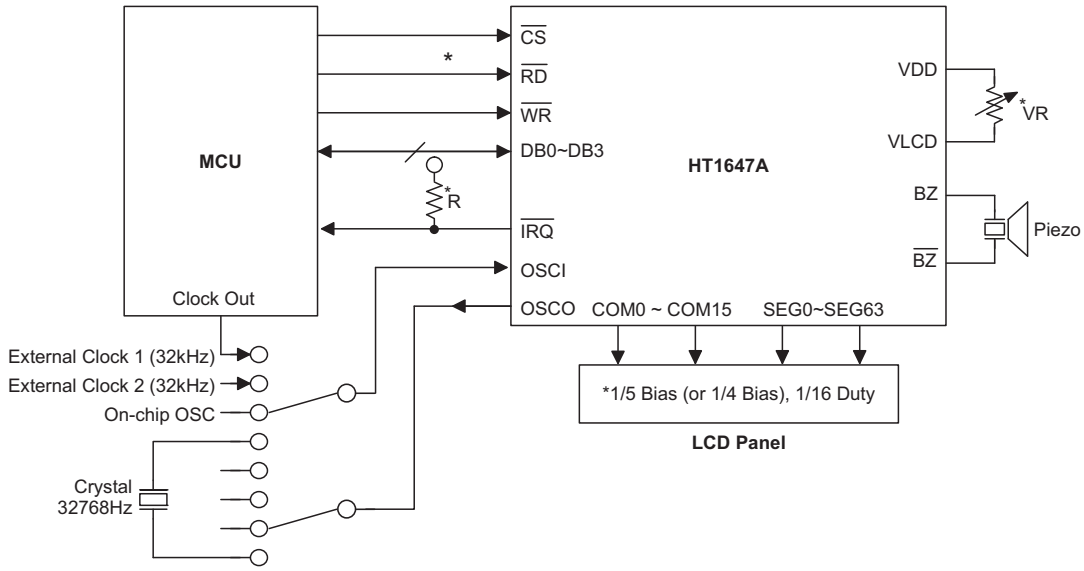
Command mode (command ID code : 1 0 0)



Note: "X" stands for don't care

Application Circuits

Host Controller with an HT1647A Display System



*Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the MCU.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ ± 20%.

It is recommended to select 1/5 bias to fit TN-type, STN-type LCDs and select 1/4 bias to fit ECB-type LCDs.

Adjust R (external pull high resistance) to fit user's time base clock.

Instruction Set Summary

Name	Command Code	D/C	Function	Def.
READ	A8**110**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Read data from the RAM	
WRITE	A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Write data to the RAM	
READ-MODIFY-WRITE	A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Read and Write data to the RAM	
SYS DIS	X**100**-0000-0000-XXXX	C	Turn Off both system oscillator and LCD bias generator	Yes
SYS EN	X**100**-0000-0001-XXXX	C	Turn On system oscillator	
LCD OFF	X**100**-0000-0010-XXXX	C	Turn Off LCD display	Yes
LCD ON	X**100**-0000-0011-XXXX	C	Turn On LCD display	
TIMER DIS	X**100**-0000-0100-XXXX	C	Disable time base output	Yes
WDT DIS	X**100**-0000-0101-XXXX	C	Disable WDT time-out flag output	Yes
TIMER EN	X**100**-0000-0110-XXXX	C	Enable time base output	
WDT EN	X**100**-0000-0111-XXXX	C	Enable WDT time-out flag output	
TONE OFF	X**100**-0000-1000-XXXX	C	Turn Off tone outputs	Yes
CLR TIMER	X**100**-0000-1101-XXXX	C	Clear the contents of the time base generator	
CLR WDT	X**100**-0000-1111-XXXX	C	Clear the contents of the WDT stage	
TONE 4K	X**100**-0001-0000-XXXX	C	Turn on tone output, tone frequency output: 4kHz	
TONE 2K	X**100**-0001-0001-XXXX	C	Turn on tone output, tone frequency output: 2kHz	

Name	Command Code	D/C	Function	Def.
IRQ DIS	X**100**-0001-0010-XXXX	C	Disable $\overline{IRQ}$ output	Yes
IRQ EN	X**100**-0001-0011-XXXX	C	Enable $\overline{IRQ}$ output	
RC 32K	X**100**-0001-0100-XXXX	C	System clock source, on-chip RC oscillator	Yes
EXT (XTAL)	X**100**-0001-0101-XXXX	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
LARGE BIAS	X**100**-0001-0110-XXXX	C	Large bias current option	Yes
MIDDLE BIAS	X**100**-0001-0111-XXXX	C	Middle bias current option	
SMALL BIAS	X**100**-0001-1000-XXXX	C	Small bias current option	
BIAS 1/5	X**100**-0001-1001-XXXX	C	LCD 1/5 bias option	Yes
BIAS 1/4	X**100**-0001-1010-XXXX	C	LCD 1/4 bias option	
FRAME 170Hz	X**100**-0001-1100-XXXX	C	Selects 170Hz frame frequency and active segment signal width can be divided into 13 sections	
FRAME 89Hz	X**100**-0001-1101-XXXX	C	Selects 89Hz frame frequency and active segment signal width can be divided into 24 sections	Yes
GRS LEVEL1	X**100**-001 B4-B3 B2 B1 B0-XXXX	C	Sets PWM data in gray scale level 1	
GRS LEVEL2	X**100**-010 B4-B3 B2 B1 B0-XXXX	C	Sets PWM data in gray scale level 2	
GRS LEVEL3	X**100**-011 B4-B3 B2 B1 B0-XXXX	C	Sets PWM data in gray scale level 3	
GRS LEVEL4	X**100**-100 B4-B3 B2 B1 B0-XXXX	C	Sets PWM data in gray scale level 4	
F1	X**100**-1010-0000-XXXX	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	X**100**-1010-0001-XXXX	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	X**100**-1010-0010-XXXX	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	X**100**-1010-0011-XXXX	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	X**100**-1010-0100-XXXX	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	X**100**-1010-0101-XXXX	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	X**100**-1010-0110-XXXX	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	X**100**-1010-0111-XXXX	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	X**100**-1111-1111-XXXX	C	Test mode, user don't use.	
NORMAL	X**100**-1111-1110-XXXX	C	Normal mode	Yes

Note: "X" stands for don't care

A8~A0: RAM address

D3~D0: RAM data

B4~B0: PWM data

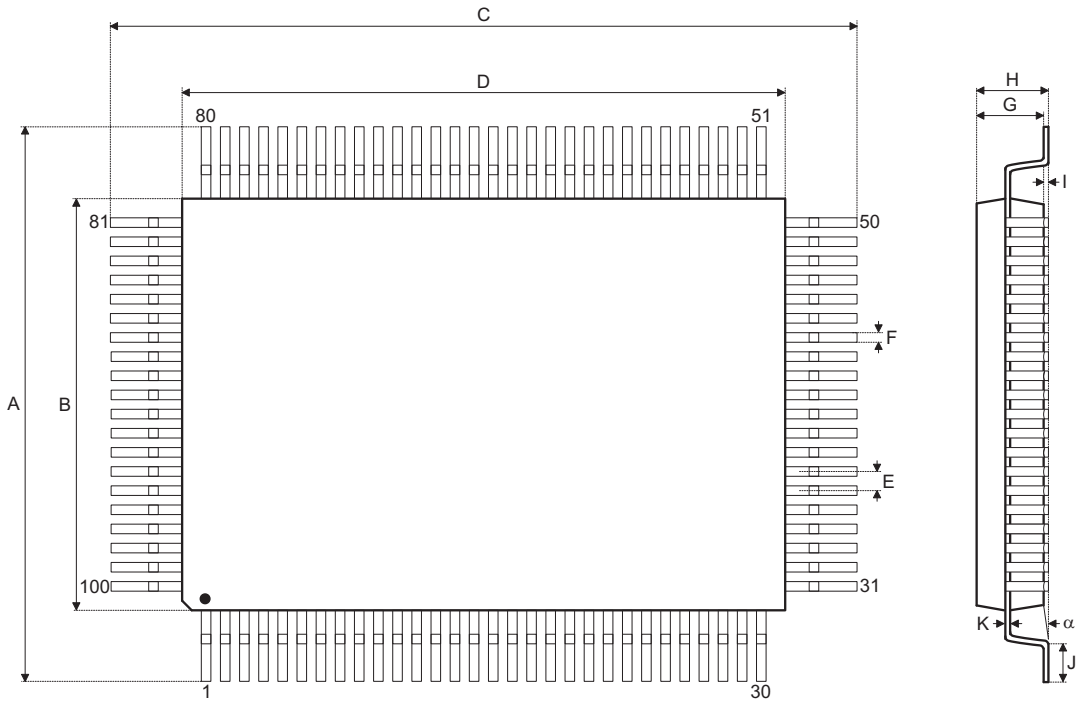
D/C: Data/Command mode

Def.: Power-on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The tone frequency source and the time base/WDT clock frequency source can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1647A after power-on reset, otherwise, power on reset may fail, which in turn leads to the malfunctioning of the HT1647A.

Package Information

100-pin QFP (14mm×20mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	18.80	—	19.20
B	13.90	—	14.10
C	24.80	—	25.20
D	19.90	—	20.10
E	—	0.65	—
F	—	0.30	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	1	—	1.40
K	0.10	—	0.20
α	0°	—	7°

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shanghai Sales Office)
G Room, 3 Floor, No.1 Building, No.2016 Yi-Shan Road, Minhang District, Shanghai, China 201103
Tel: 86-21-5422-4590
Fax: 86-21-5422-4705
http://www.holtek.com.cn

Holtek Semiconductor Inc. (Shenzhen Sales Office)
5F, Unit A, Productivity Building, No.5 Gaoxin M 2nd Road, Nanshan District, Shenzhen, China 518057
Tel: 86-755-8616-9908, 86-755-8616-9308
Fax: 86-755-8616-9722

Holtek Semiconductor Inc. (Beijing Sales Office)
Suite 1721, Jinyu Tower, A129 West Xuan Wu Men Street, Xicheng District, Beijing, China 100031
Tel: 86-10-6641-0030, 86-10-6641-7751, 86-10-6641-7752
Fax: 86-10-6641-0125

Holtek Semiconductor (USA), Inc. (North America Sales Office)
46729 Fremont Blvd., Fremont, CA 94538
Tel: 1-510-252-9880
Fax: 1-510-252-9885
http://www.holtek.com