REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45									
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

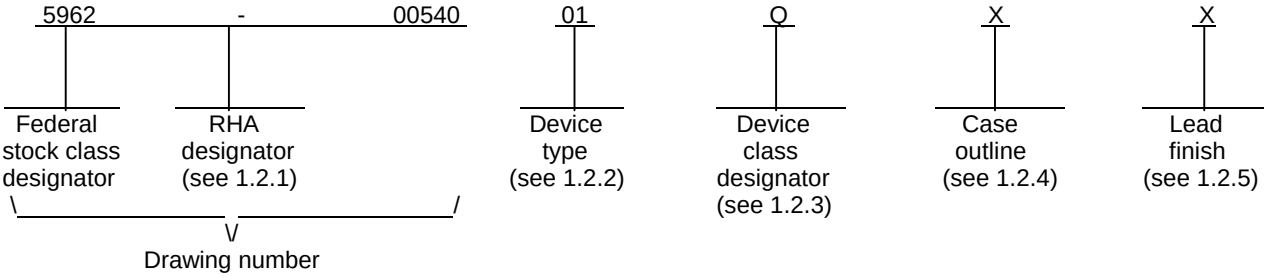
REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thanh V. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thanh V. Nguyen	
	APPROVED BY Charles Saffle	MICROCIRCUIT, DIGITAL, 32-BIT SPARC PROCESSOR, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 01-08-02	
	REVISION LEVEL	SIZE **A** / CAGE CODE **67268** / **5962-00540**
		SHEET 1 OF 45

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	695F	32-bit SPARC processor	25 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	256	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) ..... -0.5 V dc to +7.0 V dc 2/
Input voltage range (V_{IN}) ..... -0.5 V dc to V_{DD} +0.5 V dc 3/
Output current (I_{OUT})..... 50 mA 4/
Maximum power dissipation (continuous) (P_D)..... 1.5 W
Storage temperature range (T_{STG})..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +265°C 5/
Thermal resistance, junction-to-case (Θ_{JC}) ..... 3°C/W
Junction temperature (T_J)..... +165°C

1.4 Recommended operating conditions.

Operating supply voltage range (V_{DD}) ..... +4.5 V dc to +5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Device is functional from +4.5 V to +5.5 V with reference to ground.
3/ (V_{DD} + 0.5 V) should not exceed +7.0 V.
4/ This is the maximum current of any single output.
5/ Duration 10 seconds maximum at a distance not less than 1.5 mm from the device body, and the same lead shall not be resoldered until 3 minutes have elapsed.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maitained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activities upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 132 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. These devices shall be compliant to IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}	V_{DD} = 5.5 V 1/ 2/	1, 2, 3	All	2.2		V
	V_{IHCR}	V_{DD} = 5.5 V 1/ 3/	1, 2, 3	All	3.0		
Low level input voltage	V_{IL}	V_{DD} = 5.5 V 1/ 2/ 3/	1, 2, 3	All		0.8	V
High level output voltage	V_{OH}	V_{DD} =4.5 V, I_{OH} = -6.0 mA 4/ Minimum and maximum values recorded	1, 2, 3	All	2.4		V
	V_{OHB}	V_{DD} =4.5 V, I_{OH} = -16.0 mA 5/ Minimum and maximum values recorded	1, 2, 3	All	2.4		
Low level output voltage	V_{OL}	V_{DD} =4.5 V, I_{OL} = 4.0 mA 4/ Minimum and maximum values recorded	1, 2, 3	All		0.4	V
	V_{OLB}	V_{DD} =4.5 V, I_{OL} = 12.0 mA 5/ Minimum and maximum values recorded	1, 2, 3	All		0.4	
High level input current	I_{IH}	V_{DD} = 5.5 V, V_{IN} = V_{DD} 6/	1, 2, 3	All		10	µA
Low level input current	I_{IL}	V_{DD} = 5.5 V, V_{IN} = 0.0 V 7/	1, 2, 3	All		10	µA
	I_{ILT}	V_{DD} = 5.5 V, V_{IN} = 0.0 V 8/	1, 2, 3	All		350	
Three-state leakage current	I_{OZH}	V_{DD} = 5.5 V, V_{IN} = V_{DD} 9/	1, 2, 3	All		10	µA
Three-state leakage current	I_{OZL}	V_{DD} = 5.5 V, V_{IN} = 0.0 V 9/	1, 2, 3	All		10	µA
Supply current (idle) IV_{DD} pins	I_{DDIDLE}	V_{DD} = 5.5 V, f = 25 MHz	1, 2, 3	All		41	mA
Supply current (internal) IV_{DD} pins	I_{DDIN}	V_{DD} = 5.5 V, f = 25 MHz	1, 2, 3	All		230	mA
Input capacitance	C_{IN}	V_{IN} = 2.5 V T_C = 25°C f_{IN} = 1.0 MHz See 4.4.1c	4	All		10	pF
Functional test		V_{IL} = 0.0 V, V_{IH} = 3.0 V V_{OL} = 1.45 V, V_{OH} = 1.55 V V_{DD} = 4.5 V, 5.0 V, and 5.5 V f = 25 MHz See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK2 period 10/	t_1	V_{DD} = 4.5 V SYSCLK frequency = 25 MHz See figure 5	9, 10, 11	All	20		ns
SYSCLK period 10/	t_2		9, 10, 11	All	40		ns
CLK2 high and how pulse width 10/	t_3		9, 10, 11	All	9.75		ns
RA[31:0], RAPAR, RSIZE, RLDSTO, and LOCK output delay 11/	t_4		9, 10, 11	All		6.5	ns
$\overline{\text{MEMCS}}[9:0]$, $\overline{\text{ROMCS}}$, $\overline{\text{EXMCS}}$ output delay 10/ 11/	t_5		9, 10, 11	All		12.5	ns
DDIR, $\overline{\text{DDIR}}$ output delay 10/ 11/	t_6		9, 10, 11	All		15	ns
$\overline{\text{MEMWR}}$ and $\overline{\text{IOMWR}}$ output delay 11/ 12/	t_7		9, 10, 11	All		23.5	ns
$\overline{\text{OE}}$ (HL) output delay 11/	t_8		9, 10, 11	All		20.5	ns
Data setup time during load 11/	t_9		9, 10, 11	All	11.5		ns
Data hold time during load 10/ 11/	t_{10}		9, 10, 11	All	5		ns
Data output delay 12/	t_{11}		9, 10, 11	All		28	ns
Data output valid 10/ 11/	t_{12}		9, 10, 11	All	8		ns
CB output delay 10/ 11/	t_{13}		9, 10, 11	All		19	ns
$\overline{\text{ALE}}$ output delay 10/ 12/	t_{14}		9, 10, 11	All		13	ns
$\overline{\text{BUFFEN}}$ (HL) output delay 10/ 11/	t_{15}		9, 10, 11	All		21	ns
$\overline{\text{MHOLD}}$ output delay 10/ 11/	t_{16}		9, 10, 11	All		12	ns
$\overline{\text{MDS}}$, $\overline{\text{DRDY}}$ output delay 10/ 11/	t_{17}		9, 10, 11	All		15	ns
$\overline{\text{MEXC}}$ output delay 10/ 12/	t_{20}		9, 10, 11	All		15	ns
RASI[3:0], RSIZE[1:0], RASPAR setup time 10/ 11/	t_{21}		9, 10, 11	All	10		ns
RASI[3:0], RSIZE[1:0], RASPAR hold time 10/ 11/	t_{22}		9, 10, 11	All	3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
BOOT PROM address output delay 10/ 11/	t_{23}	V_{DD} = 4.5 V SYSCLK frequency = 25 MHz See figure 5	9, 10, 11	All		13	ns
$\overline{\text{BUSRDY}}$ setup time 10/ 11/	t_{24}		9, 10, 11	All	12		ns
$\overline{\text{BUSRDY}}$ hold time 10/ 11/	t_{25}		9, 10, 11	All	0		ns
$\overline{\text{IOSEL}}$ output delay 10/ 11/	t_{27}		9, 10, 11	All		15	ns
DMAAS setup time 10/ 11/	t_{28}		9, 10, 11	All	12	20	ns
DMAAS hold time 10/ 12/	t_{29}		9, 10, 11	All	0	20	ns
$\overline{\text{DMAREQ}}$ setup time 10/ 11/	t_{30}		9, 10, 11	All	12		ns
$\overline{\text{DMAGNT}}$ output delay 10/ 11/	t_{31}		9, 10, 11	All		15	ns
RA[31:0], RAPAR, CPAR setup time 10/ 11/	t_{32}		9, 10, 11	All	10		ns
RA[31:0], RAPAR, CPAR hold time 10/ 11/	t_{33}		9, 10, 11	All	3		ns
TCK period 10/	t_{36}		9, 10, 11	All	100		ns
TMS setup time 10/ 13/	t_{37}		9, 10, 11	All	10		ns
TMS hold time 10/ 13/	t_{38}		9, 10, 11	All	4		ns
TDI setup time 10/ 13/	t_{39}		9, 10, 11	All	10		ns
TDI hold time 10/ 13/	t_{40}		9, 10, 11	All	10		ns
TDO output delay 10/ 14/	t_{41}		9, 10, 11	All		20	ns
INULL output delay 10/ 11/	t_{46}		9, 10, 11	All		22	ns
$\overline{\text{RESET}}$, $\overline{\text{CPUHALT}}$ output delay 10/ 11/	t_{48}		9, 10, 11	All		22	ns
$\overline{\text{SYSERR}}$, SYSAV output delay 10/ 11/	t_{49}		9, 10, 11	All		20	ns
$\overline{\text{IUERR}}$ output delay 10/ 11/	t_{50}		9, 10, 11	All		20	ns
EXTINT[4:0] setup time 10/ 12/	t_{52}		9, 10, 11	All	12		ns
EXTINT[4:0] hold time 10/ 11/	t_{53}		9, 10, 11	All	0		ns
EXTINTACK output delay 10/ 11/	t_{54}		9, 10, 11	All		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{OE}$ (LH) output delay (no DMA mode) 10/ 11/	t_{56}	V_{DD} = 4.5 V SYSCLK frequency = 25 MHz See figure 5	9, 10, 11	All		8.5	ns
$\overline{BUFFEN}$ (LH) output delay 10/ 11/	t_{57}		9, 10, 11	All		9	ns
INST output delay 10/ 11/	t_{60}		9, 10, 11	All		22	ns
Data output delay to low-Z 10/ 11/	t_{61}		9, 10, 11	All	20		ns

1/ Not recorded – Tested go/no-go during functional test.

2/ Applies to RA[31:0], RAPAR, RASI[3:0], RSIZE[1:0], RASPAR, CPAR, D[31:0], CB[6:0], DPAR, RLDSTO, DXFER, LOCK, RD, $\overline{WE}$, WRT, $\overline{PROM8}$, $\overline{ROMWRT}$, $\overline{BUSRDY}$, $\overline{BUSERR}$, $\overline{DMAREQ}$, DMAAS, $\overline{SYSHALT}$, $\overline{NOPAR}$, IWDE, WDCLK, CLK2, TMODE[1:0], DEBUG, TCK, $\overline{TRST}$, TMS, TDI.

3/ Applies to RxA, RxB, GPI[7:0], EXTINT[4:0], EWDINT, $\overline{SYSRESET}$.

4/ Applies to RAPAR, RASI[3:0], RSIZE[1:0], RASPAR, CPAR, D[31:0], CB[6:0], DPAR, RLDSTO, $\overline{ALE}$, DXFER, LOCK, RD, $\overline{WE}$, WRT, $\overline{MHOLD}$, $\overline{MDS}$, $\overline{MEXC}$, BA[1:0], $\overline{ROMCS}$, $\overline{MEMCS[9:0]}$, $\overline{BUFFEN}$, DDIR, $\overline{DDIR}$, $\overline{IOSEL[3:0]}$, $\overline{IOWR}$, $\overline{EXMCS}$, $\overline{DMAGNT}$, $\overline{DRDY}$, $\overline{IUERR}$, $\overline{CPUHALT}$, $\overline{SYSERR}$, SYSAV, INULL, INST, FLUSH, DIA, RTC, TxA, TxB, GPIINT, EXTINTACK, SYSCLK, $\overline{RESET}$, TDO.

5/ Applies to RA[31:0], $\overline{MEMWR}$, $\overline{OE}$.

6/ Applies to $\overline{PROM8}$, $\overline{ROMWRT}$, $\overline{BUSRDY}$, $\overline{BUSERR}$, $\overline{DMAREQ}$, DMAAS, $\overline{SYSHALT}$, $\overline{NOPAR}$, RxA, RxB, EXTINT[4:0], IWDE, EWDINT, WDCLK, CLK2, $\overline{SYSRESET}$, TMODE[1:0], DEBUG, TCK, $\overline{TRST}$, TMS, TDI.

7/ Applies to $\overline{PROM8}$, $\overline{ROMWRT}$, $\overline{BUSRDY}$, $\overline{BUSERR}$, $\overline{DMAREQ}$, DMAAS, $\overline{SYSHALT}$, $\overline{NOPAR}$, RxA, RxB, EXTINT[4:0], IWDE, EWDINT, WDCLK, CLK2, $\overline{SYSRESET}$, TMODE[1:0], DEBUG TCK, $\overline{TRST}$.

8/ Applies to TMS, TDI.

9/ Applies to RA[31:0], RAPAR, RASI[3:0], RSIZE[1:0], RASPAR, CPAR, D[31:0], CB[6:0], DPAR, RLDSTO, DXFER, LOCK, RD, $\overline{WE}$, WRT, GPI[7:0].

10/ Tested during AC tests but not recorded.

11/ With reference edge of SYSCLK+.

12/ With reference edge of SYSCLK-.

13/ With reference edge of TCK+.

14/ With reference edge of TCK-.

Case outline X

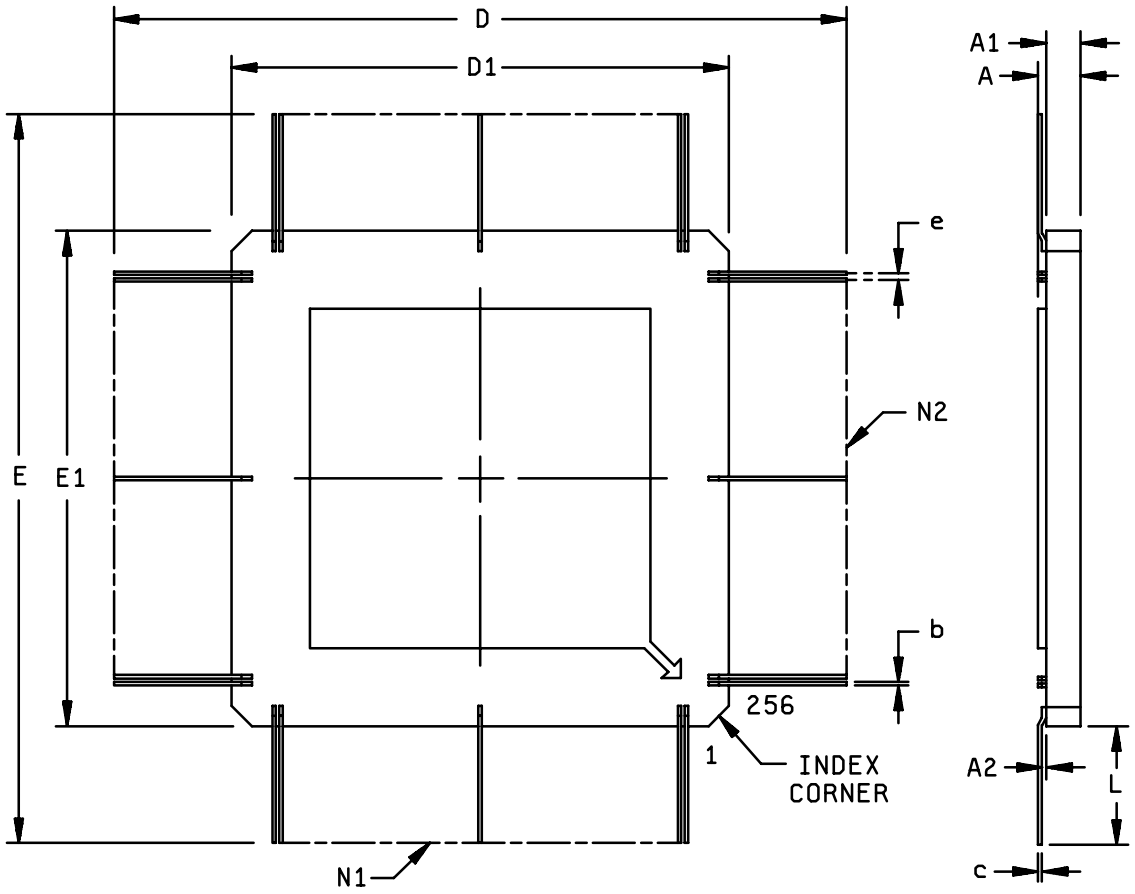


FIGURE 1. Case outline.

Case outline X - Continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
b	0.15	0.25	.006	.010
c	0.10	0.20	.004	.008
D/E	53.23	55.74	2.095	2.195
D1/E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
L	8.20	9.20	.323	.362
N1/N2	64		64	

FIGURE 1. Case outline – Continued.

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	GPIINT	33	D[20]	65	D[0]	97	RA[18]
2	GPI[7]	34	D[19]	66	RSIZE[1]	98	V_{CCO}
3	V_{CCO}	35	D[18]	67	RSIZE[0]	99	V_{SSO}
4	V_{SSO}	36	V_{CCO}	68	RASI[3]	100	RA[17]
5	GPI[6]	37	V_{SSO}	69	V_{CCO}	101	RA[16]
6	GPI[5]	38	D[17]	70	V_{SSO}	102	RA[15]
7	GPI[4]	39	D[16]	71	RASI[2]	103	V_{CCO}
8	GPI[3]	40	V_{CCI}	72	RASI[1]	104	V_{SSO}
9	V_{CCO}	41	V_{SSI}	73	RASI[0]	105	RA[14]
10	V_{SSO}	42	D[15]	74	RA[31]	106	V_{CCI}
11	GPI[2]	43	D[14]	75	RA[30]	107	V_{SSI}
12	GPI[1]	44	V_{CCO}	76	V_{CCO}	108	RA[13]
13	GPI[0]	45	V_{SSO}	77	V_{SSO}	109	RA[12]
14	D[31]	46	D[13]	78	RA[29]	110	V_{CCO}
15	D[30]	47	D[12]	79	RA[28]	111	V_{SSO}
16	V_{CCO}	48	D[11]	80	RA[27]	112	RA[11]
17	V_{SSO}	49	D[10]	81	V_{CCO}	113	RA[10]
18	D[29]	50	V_{CCO}	82	V_{SSO}	114	RA[9]
19	D[28]	51	V_{SSO}	83	RA[26]	115	V_{CCO}
20	V_{CCI}	52	D[9]	84	RA[25]	116	V_{SSO}
21	V_{SSI}	53	D[8]	85	RA[24]	117	RA[8]
22	D[27]	54	D[7]	86	V_{CCI}	118	RA[7]
23	D[26]	55	D[6]	87	V_{SSI}	119	RA[6]
24	V_{CCO}	56	V_{CCO}	88	V_{CCO}	120	V_{CCO}
25	V_{SSO}	57	V_{SSO}	89	V_{SSO}	121	V_{SSO}
26	D[25]	58	D[5]	90	RA[23]	122	RA[5]
27	D[24]	59	D[4]	91	RA[22]	123	RA[4]
28	D[23]	60	D[3]	92	RA[21]	124	RA[3]
29	D[22]	61	D[2]	93	V_{CCO}	125	V_{CCO}
30	V_{CCO}	62	V_{CCO}	94	V_{SSO}	126	V_{SSO}
31	V_{SSO}	63	V_{SSO}	95	RA[20]	127	RA[2]
32	D[21]	64	D[1]	96	RA[19]	128	RA[1]

FIGURE 2. Terminal connections.

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
129	RA[0]	161	$\overline{\text{SYSERR}}$	193	DXFER	225	$\overline{\text{MEMCS[3]}}$
130	V_{CCO}	162	SYSAV	194	$\overline{\text{MEXC}}$	226	V_{CCO}
131	V_{SSO}	163	EXTINT[4]	195	V_{CCO}	227	V_{SSO}
132	RAPAR	164	EXTINT[3]	196	V_{SSO}	228	$\overline{\text{MEMCS[2]}}$
133	RASPAR	165	EXTINT[2]	197	$\overline{\text{RESET}}$	229	$\overline{\text{MEMCS[1]}}$
134	DPAR	166	EXTINT[1]	198	$\overline{\text{SYSRESET}}$	230	$\overline{\text{MEMCS[0]}}$
135	V_{CCO}	167	EXTINT[0]	199	BA[1]	231	V_{CCI}
136	V_{SSO}	168	V_{CCI}	200	BA[0]	232	V_{SSI}
137	SYSCLK	169	V_{SSI}	201	CB[6]	233	$\overline{\text{OE}}$
138	TDO	170	EXTINTACK	202	CB[5]	234	V_{CCO}
139	$\overline{\text{TRST}}$	171	$\overline{\text{IUERR}}$	203	V_{CCO}	235	V_{SSO}
140	TMS	172	V_{CCO}	204	V_{SSO}	236	$\overline{\text{MEMWR}}$
141	TDI	173	V_{SSO}	205	CB[4]	237	$\overline{\text{BUFFEN}}$
142	TCK	174	CPAR	206	CB[3]	238	DDIR
143	CLK2	175	TXA	207	CB[2]	239	V_{CCO}
144	$\overline{\text{DRDY}}$	176	RXA	208	CB[1]	240	V_{SSO}
145	DMAAS	177	RXB	209	V_{CCO}	241	$\overline{\text{DDIR}}$
146	V_{CCO}	178	TXB	210	V_{SSO}	242	$\overline{\text{MHOLD}}$
147	V_{SSO}	179	$\overline{\text{IOWR}}$	211	CB[0]	243	$\overline{\text{MDS}}$
148	$\overline{\text{DMAGNT}}$	180	$\overline{\text{IOSEL[3]}}$	212	$\overline{\text{ALE}}$	244	WDCLK
149	$\overline{\text{EXMCS}}$	181	V_{CCO}	213	V_{CCI}	245	IWDE
150	V_{CCI}	182	V_{SSO}	214	V_{SSI}	246	EWDINT
151	V_{SSI}	183	$\overline{\text{IOSEL[2]}}$	215	$\overline{\text{PROM8}}$	247	TMODE[1]
152	$\overline{\text{DMAREQ}}$	184	$\overline{\text{IOSEL[1]}}$	216	$\overline{\text{ROMCS}}$	248	TMODE[0]
153	$\overline{\text{BUSERR}}$	185	$\overline{\text{IOSEL[0]}}$	217	$\overline{\text{MEMCS[9]}}$	249	DEBUG
154	$\overline{\text{BUSRDY}}$	186	WRT	218	V_{CCO}	250	INULL
155	$\overline{\text{ROMWRT}}$	187	$\overline{\text{WE}}$	219	V_{SSO}	251	DIA
156	$\overline{\text{NOPAR}}$	188	V_{CCO}	220	$\overline{\text{MEMCS[8]}}$	252	V_{CCO}
157	$\overline{\text{SYSHALT}}$	189	V_{SSO}	221	$\overline{\text{MEMCS[7]}}$	253	V_{SSO}
158	$\overline{\text{CPUHALT}}$	190	RD	222	$\overline{\text{MEMCS[6]}}$	254	FLUSH
159	V_{CCO}	191	RLDSTO	223	$\overline{\text{MEMCS[5]}}$	255	INST
160	V_{SSO}	192	LOCK	224	$\overline{\text{MEMCS[4]}}$	256	RTC

FIGURE 2. Terminal connections – Continued.

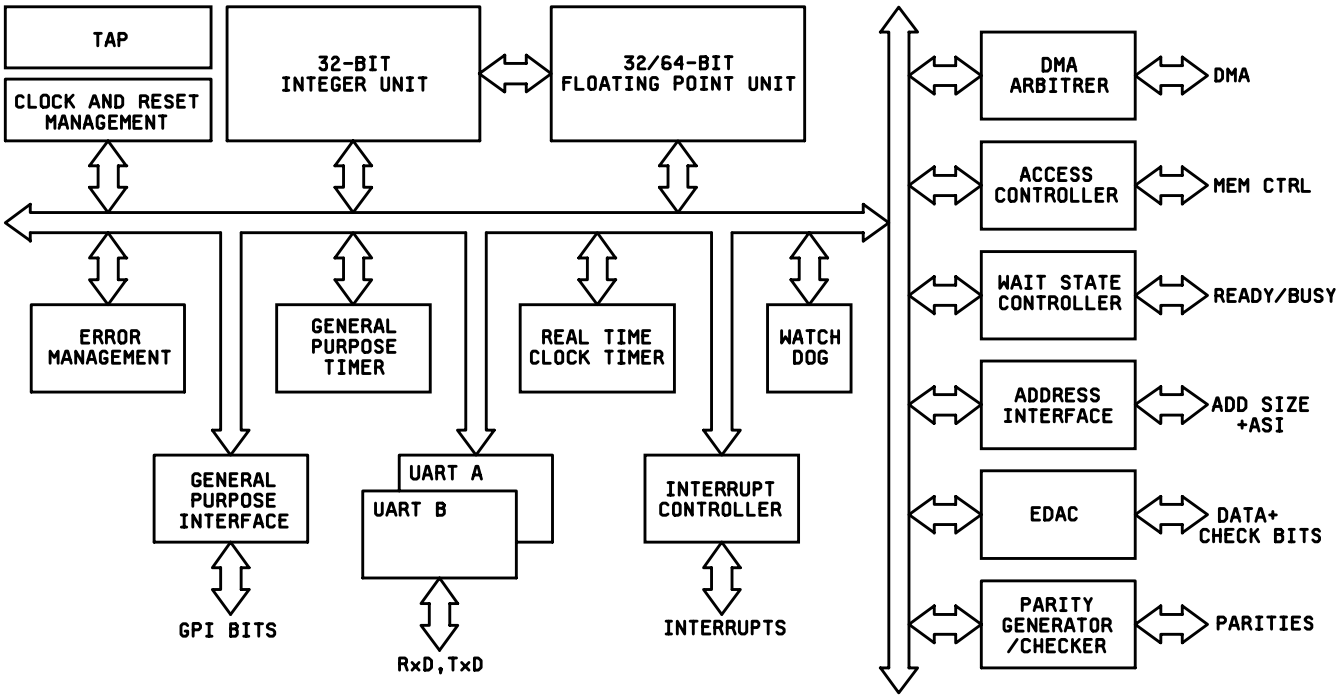
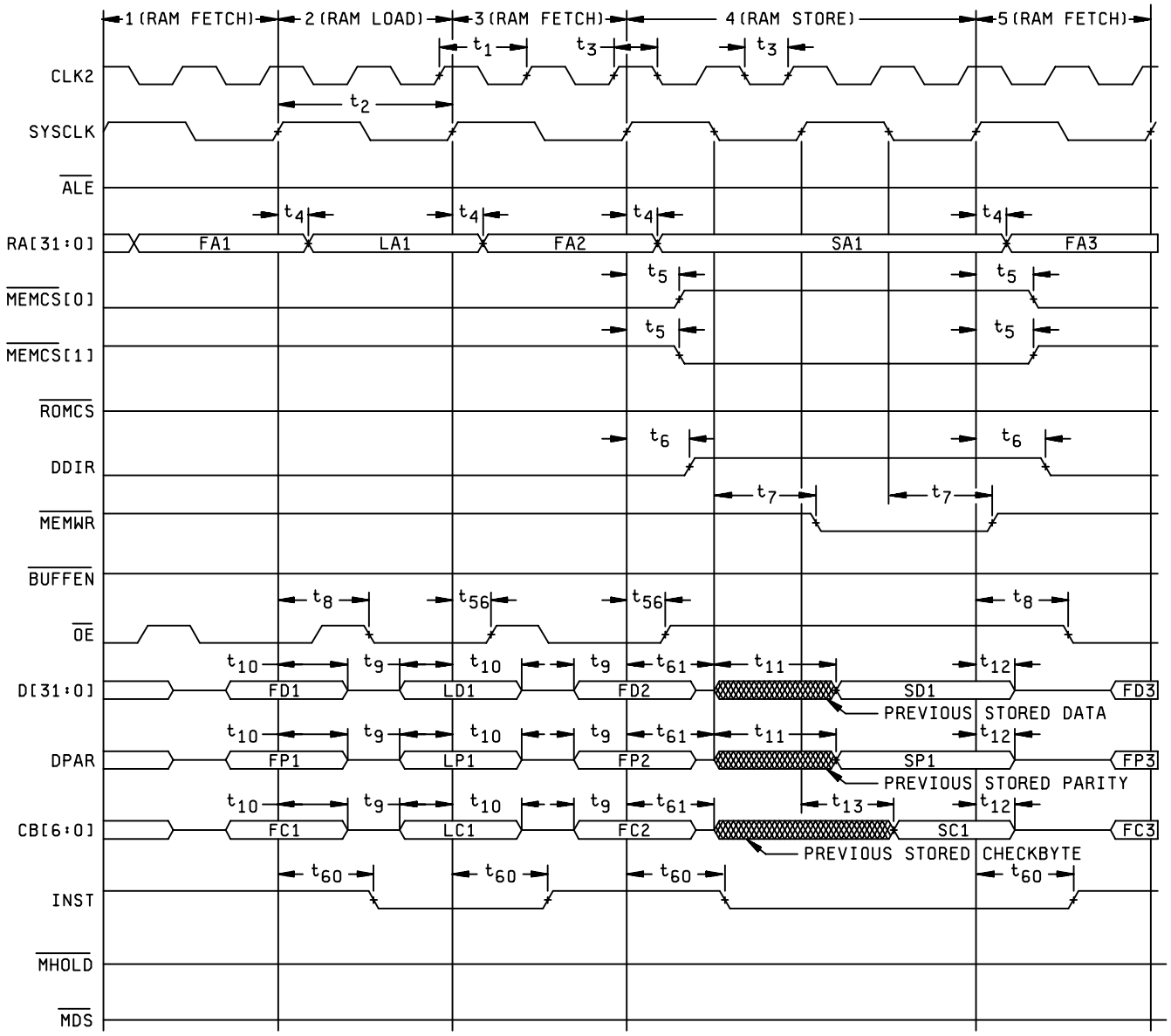


FIGURE 3. Block diagram.

Device type 01	
Instruction name	Instruction code
BYPASS	11.1111
EXTEST	00.0000
SAMPLE/PRELOAD	00.0001
INTEST	00.0011
ID code	10.0000
Reserved for emulation	01.1000
Reserved for emulation	01.1001
Reserved for emulation	01.1010
Reserved for emulation	01.1100
Reserved for emulation	01.1101
Reserved for emulation	01.1110

FIGURE 4. Boundary scan instruction codes.



RAM FETCH, RAM LOAD, RAM FETCH AND RAM STORE SEQUENCE -0 WAITSTATE

FIGURE 5. Timing waveforms.

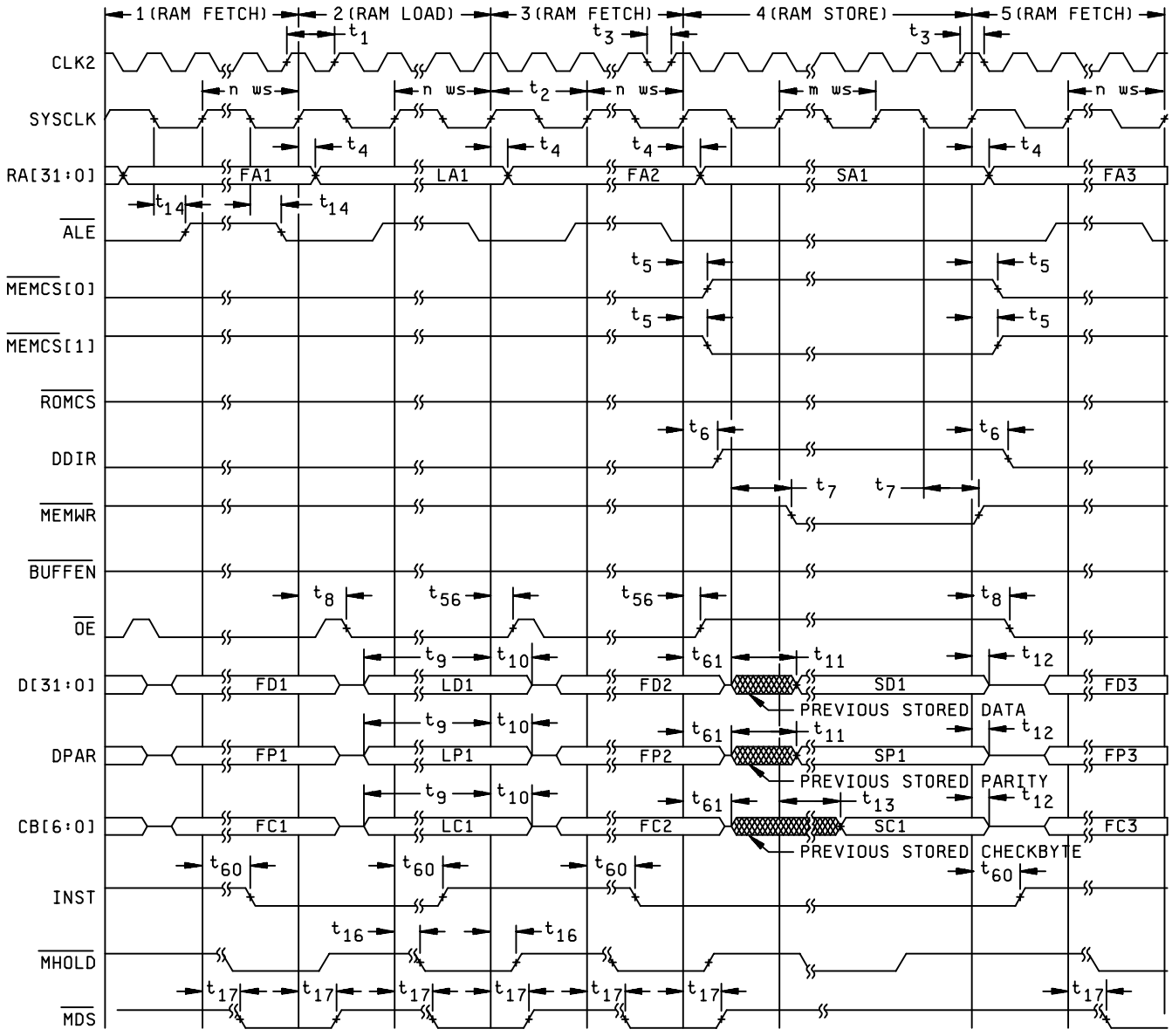


FIGURE 5. Timing waveforms - Continued.

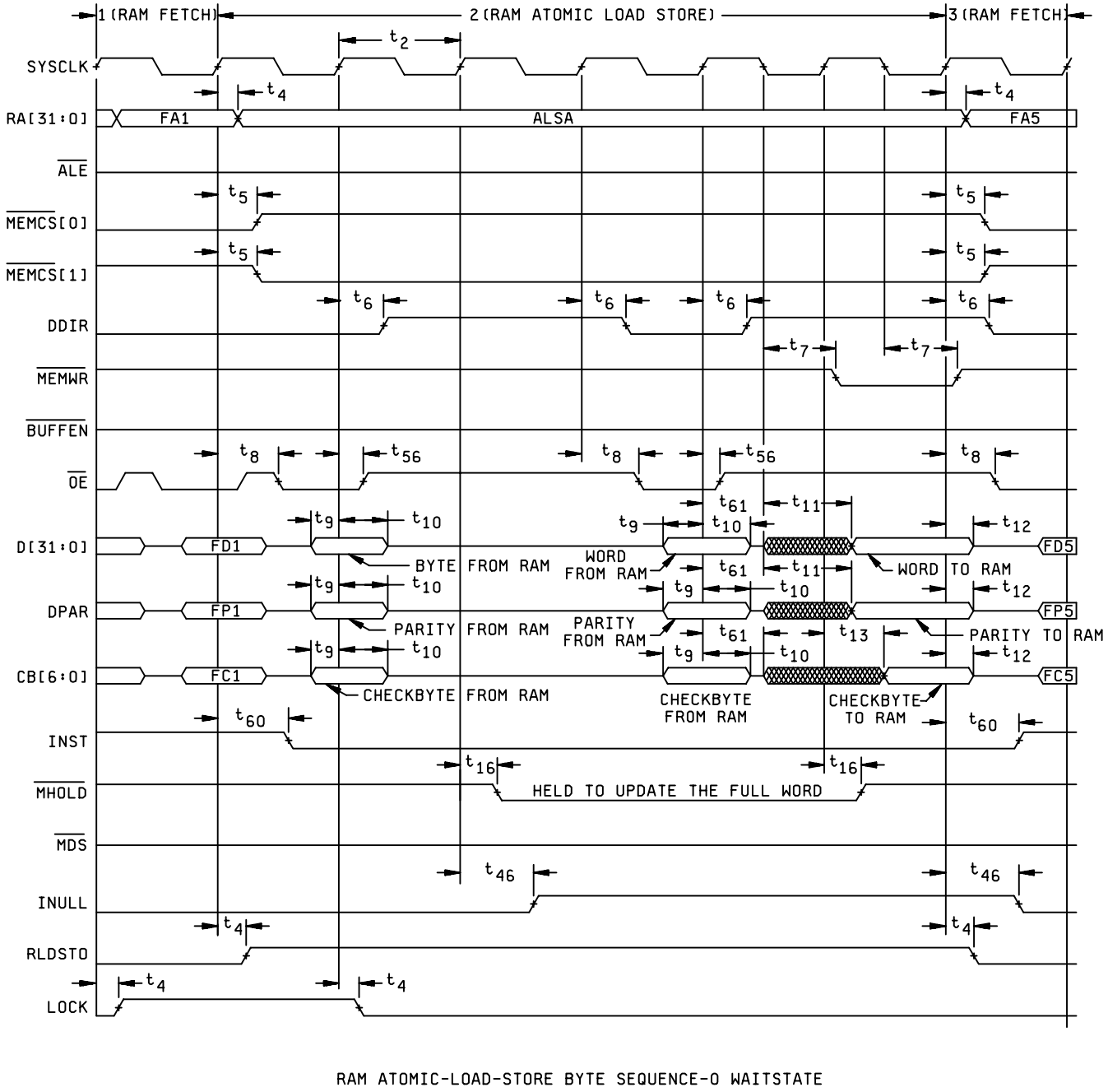
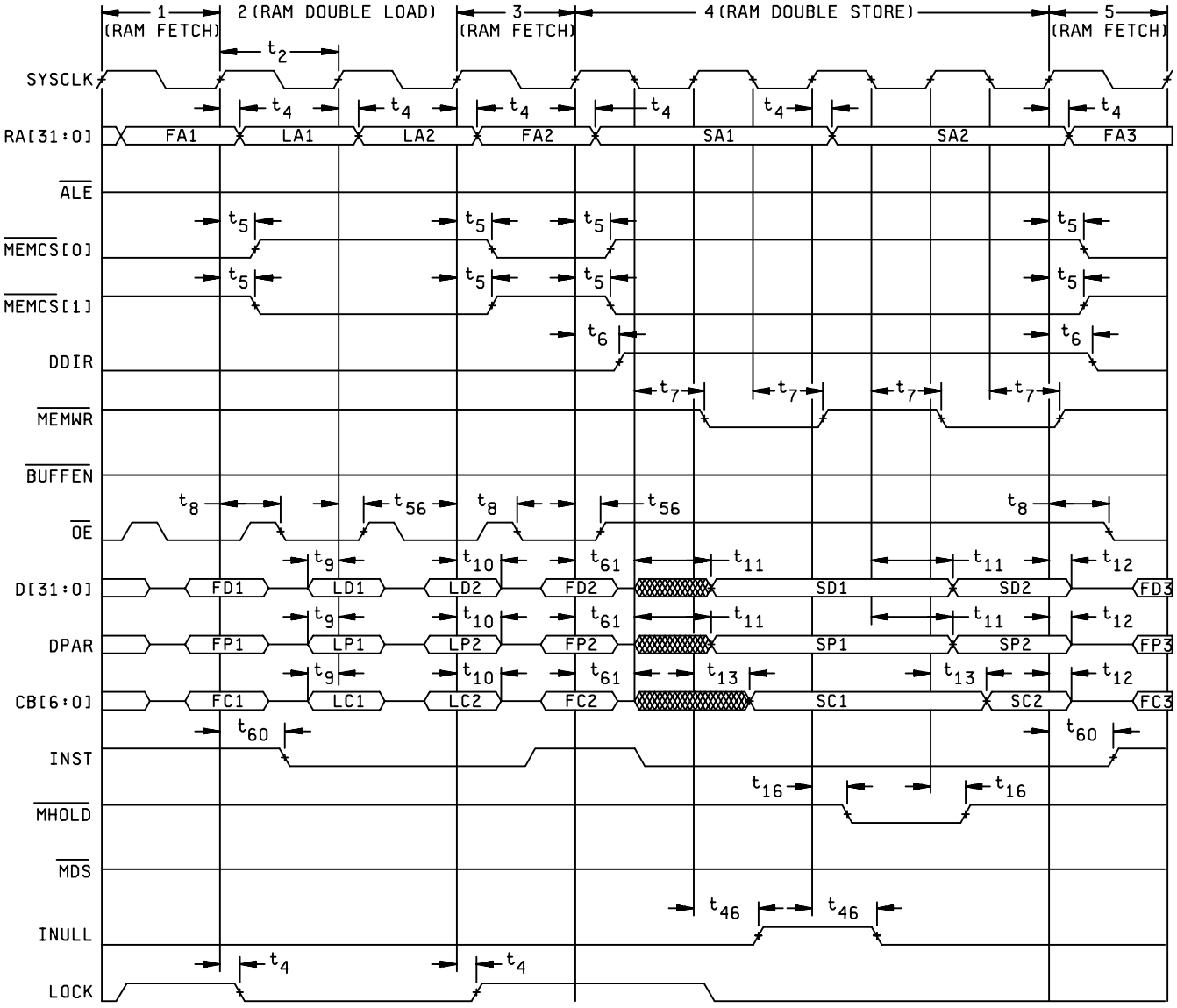
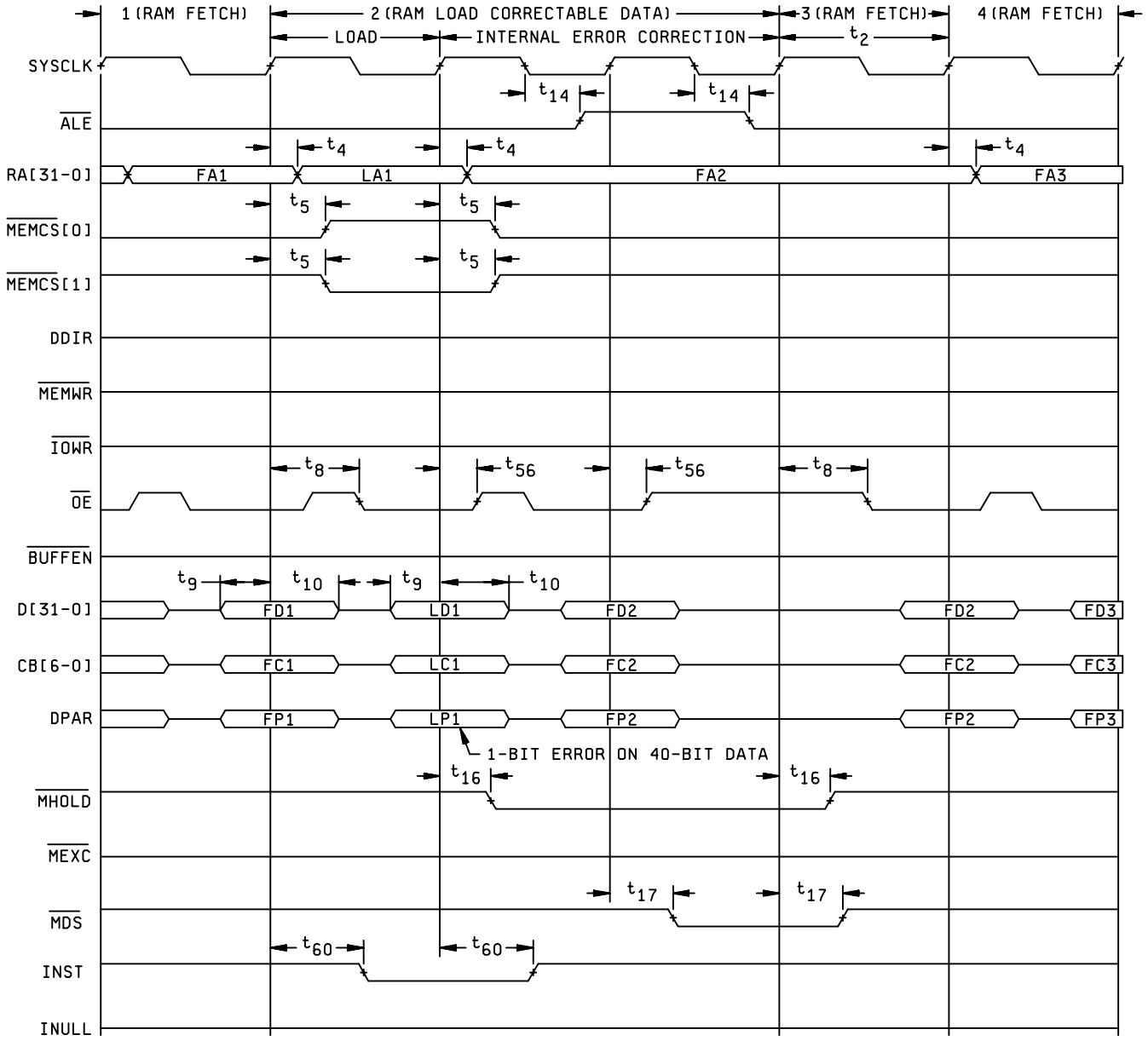


FIGURE 5. Timing waveforms - Continued.



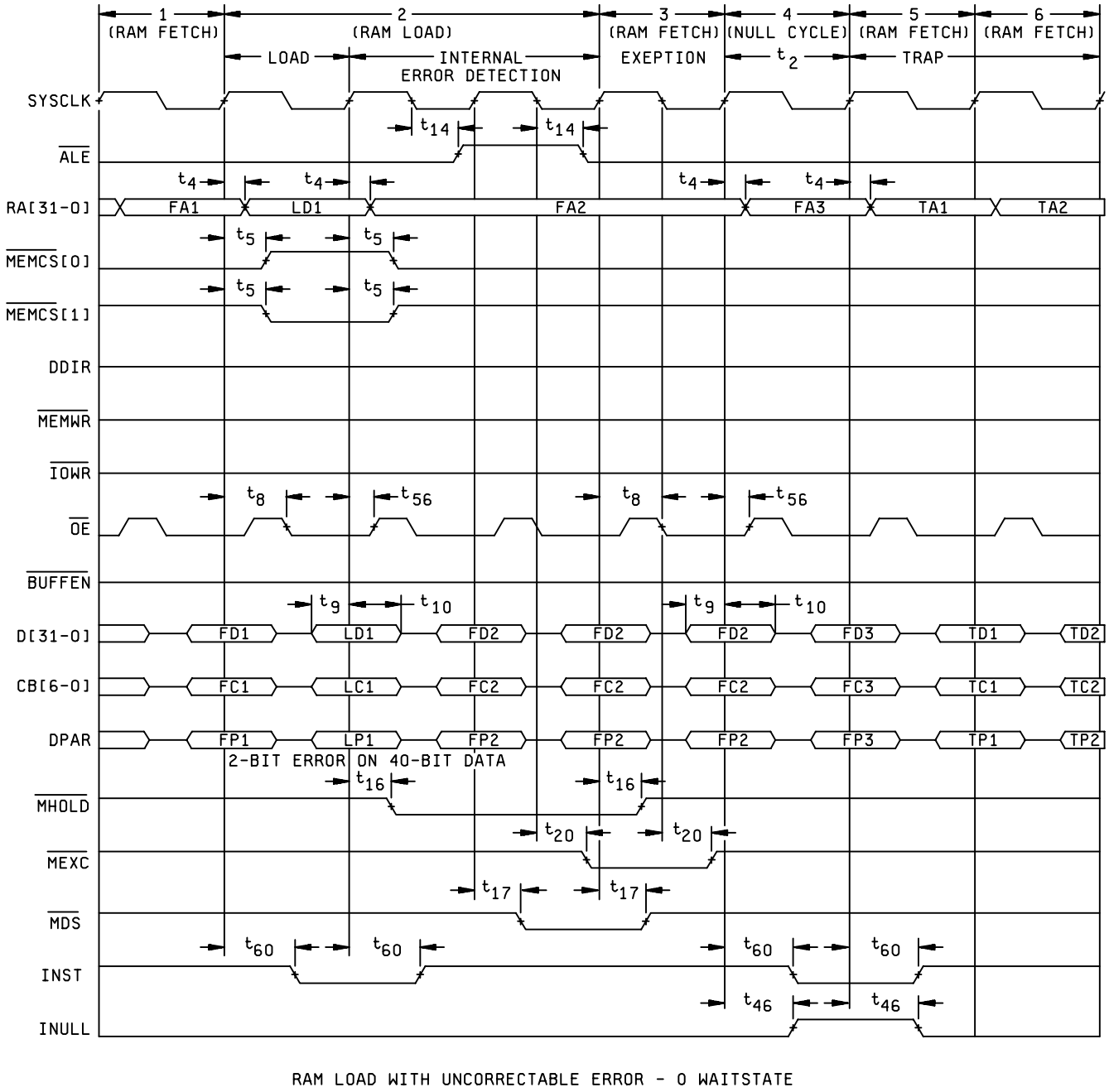
RAM LOAD-DOUBLE AND RAM STORE-DOUBLE SEQUENCE - 0 WAITSTATE

FIGURE 5. Timing waveforms - Continued.



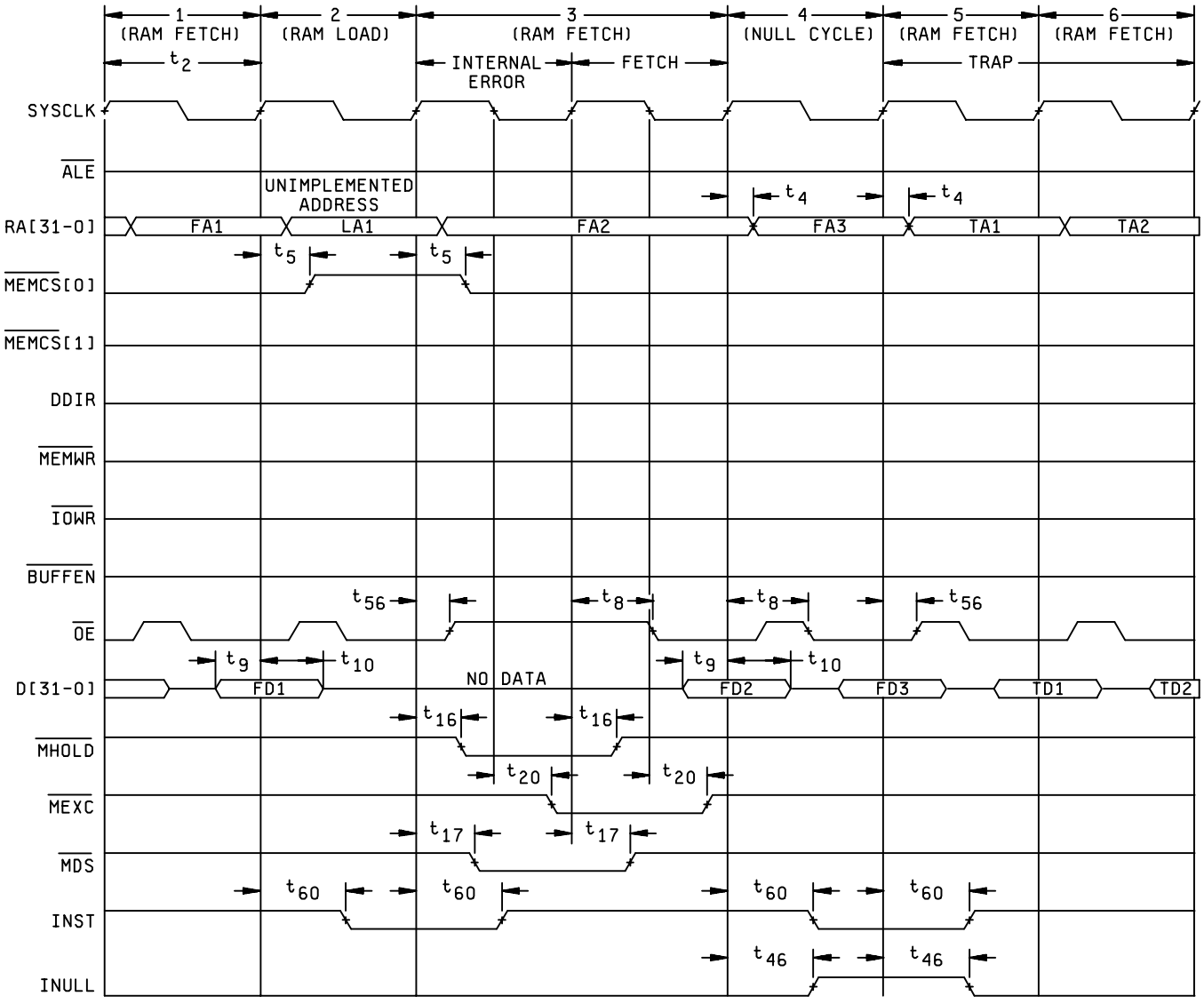
RAM LOAD WITH CORRECTABLE ERROR - 0 WAITSTATE

FIGURE 5. Timing waveforms - Continued.



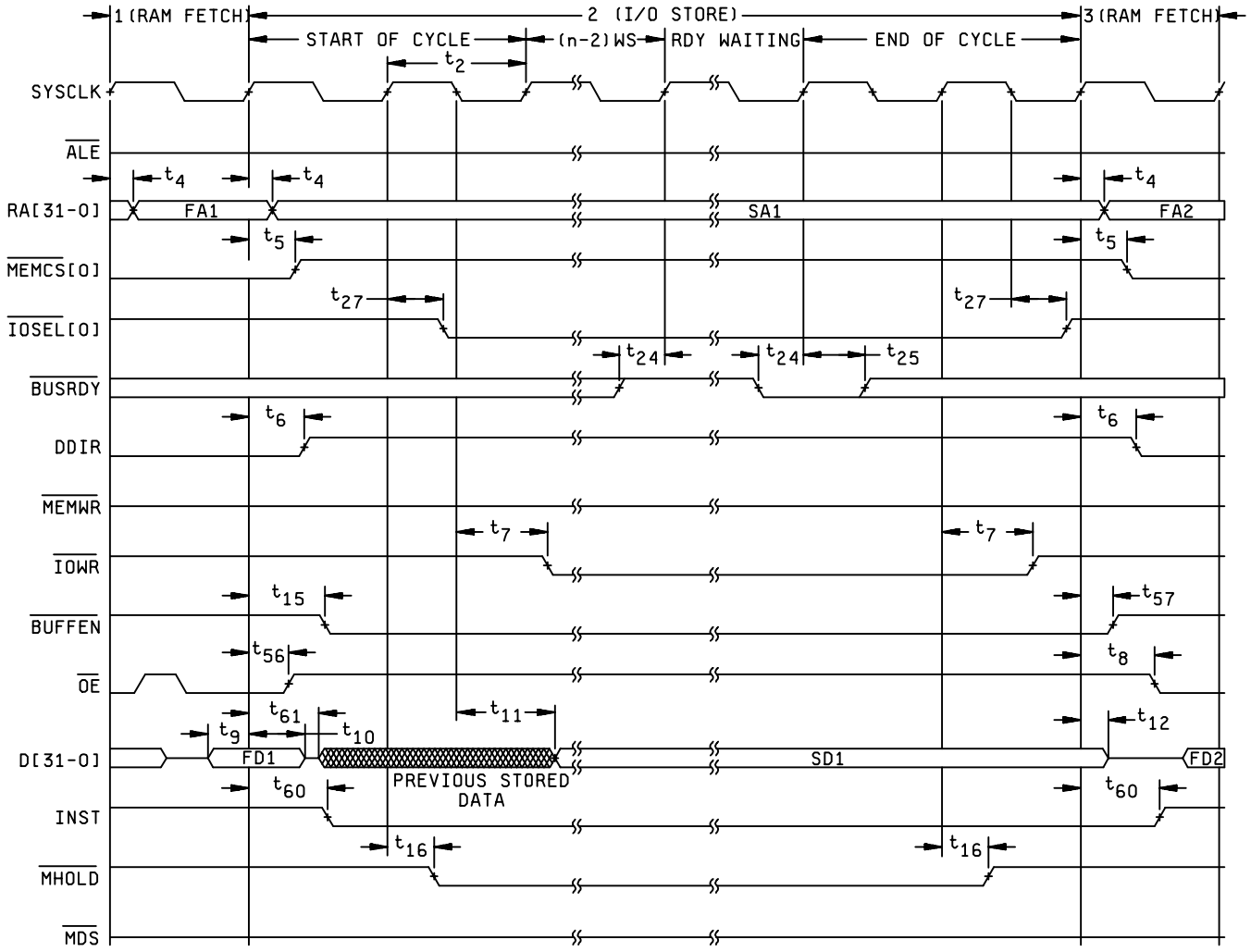
RAM LOAD WITH UNCORRECTABLE ERROR - 0 WAITSTATE

FIGURE 5. Timing waveforms - Continued.



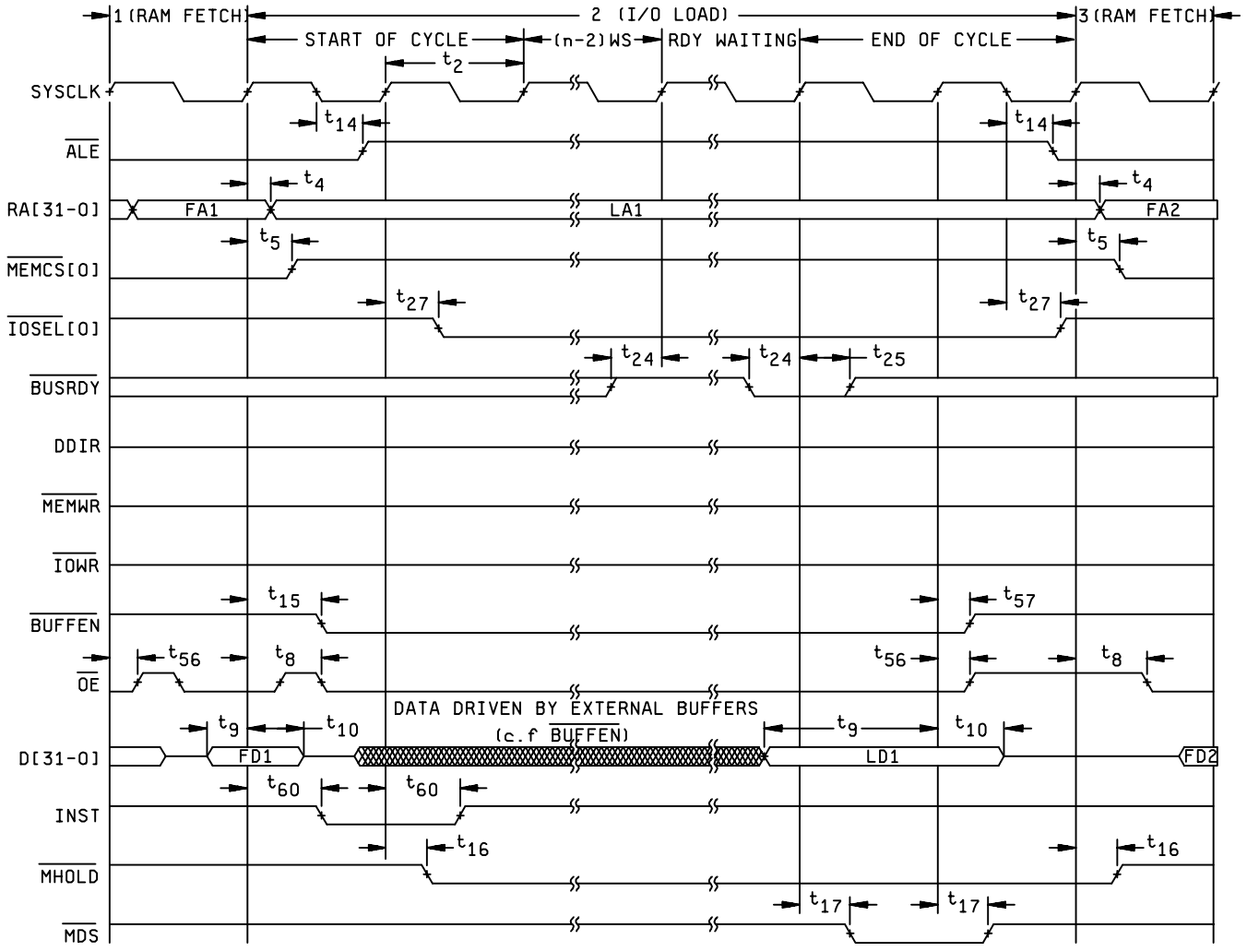
RAM LOAD WITH UNIMPLEMENTED AREA ACCESS - 0 WAITSTATE

FIGURE 5. Timing waveforms - Continued.



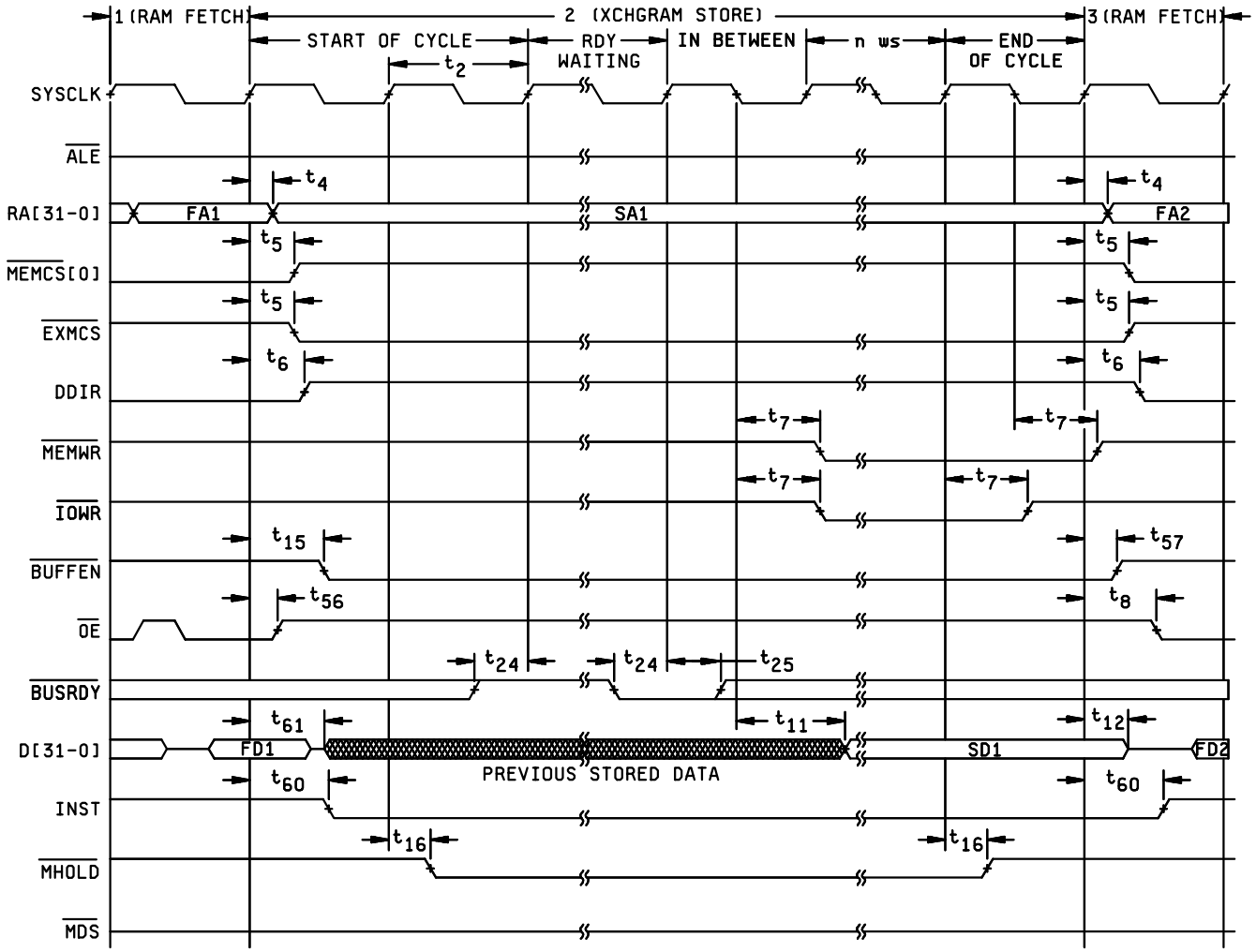
I/O STORE SEQUENCE WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES (TIMING FOR 0 OR 1 WAITSTATE = TIMING FOR 2 WAITSTATES)

FIGURE 5. Timing waveforms - Continued.



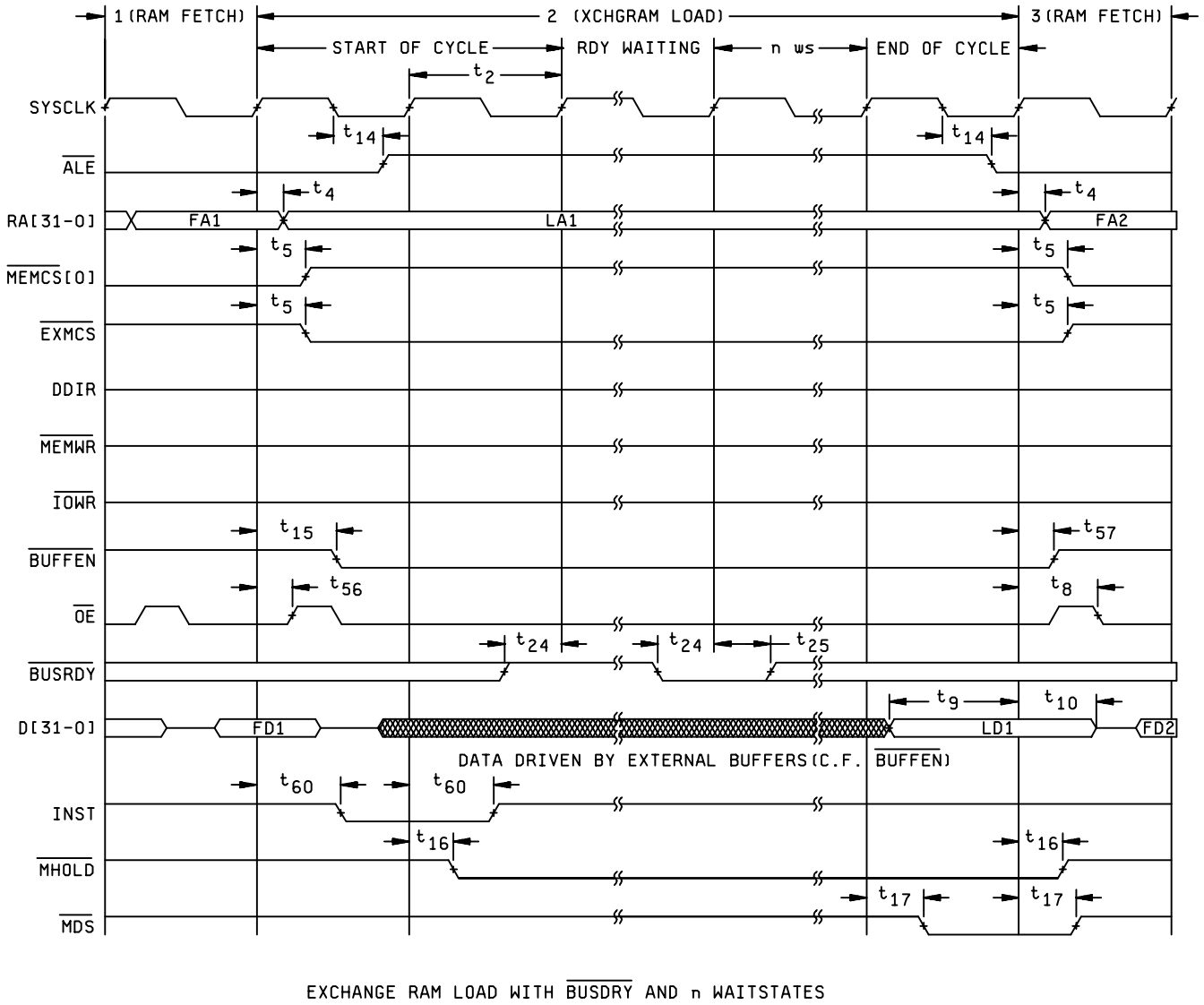
I/O LOAD SEQUENCE WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES (TIMING FOR 0 OR 1 WS = TIMING FOR 2 WS)

FIGURE 5. Timing waveforms - Continued.



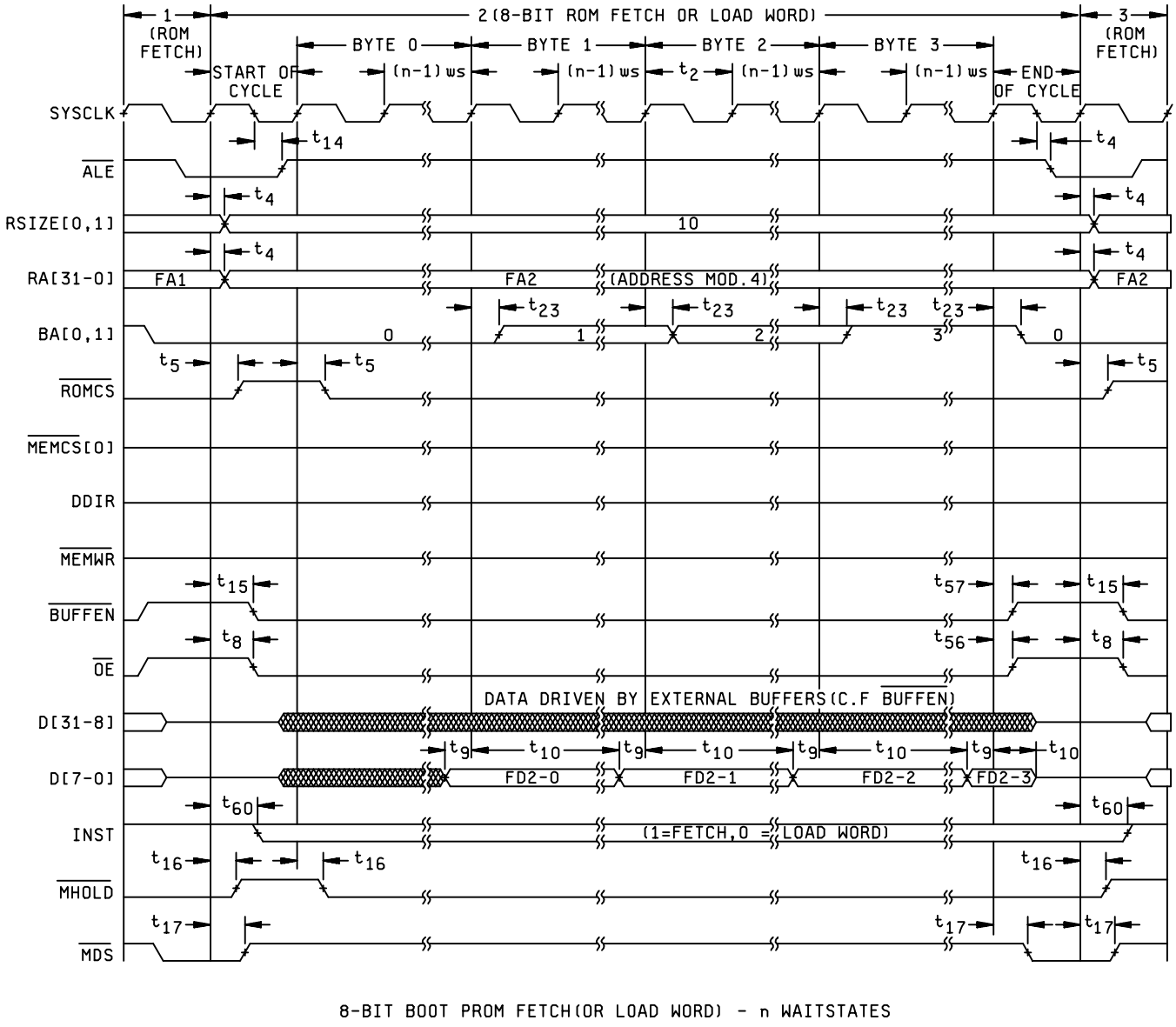
EXCHANGE RAM STORE WITH $\overline{\text{BUSDRY}}$ AND n WAITSTATES

FIGURE 5. Timing waveforms - Continued.



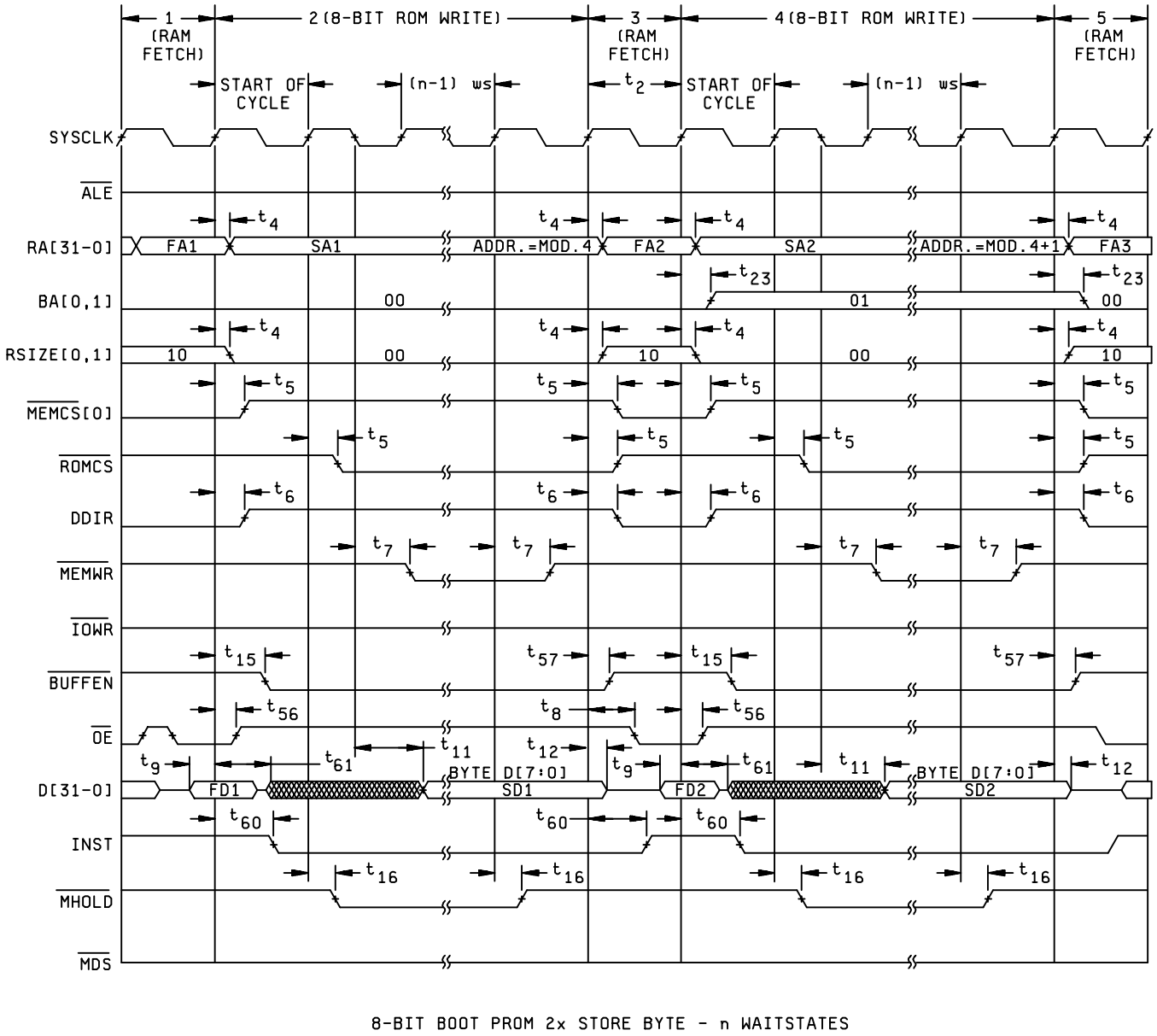
EXCHANGE RAM LOAD WITH $\overline{\text{BUSDRY}}$ AND n WAITSTATES

FIGURE 5. Timing waveforms - Continued.



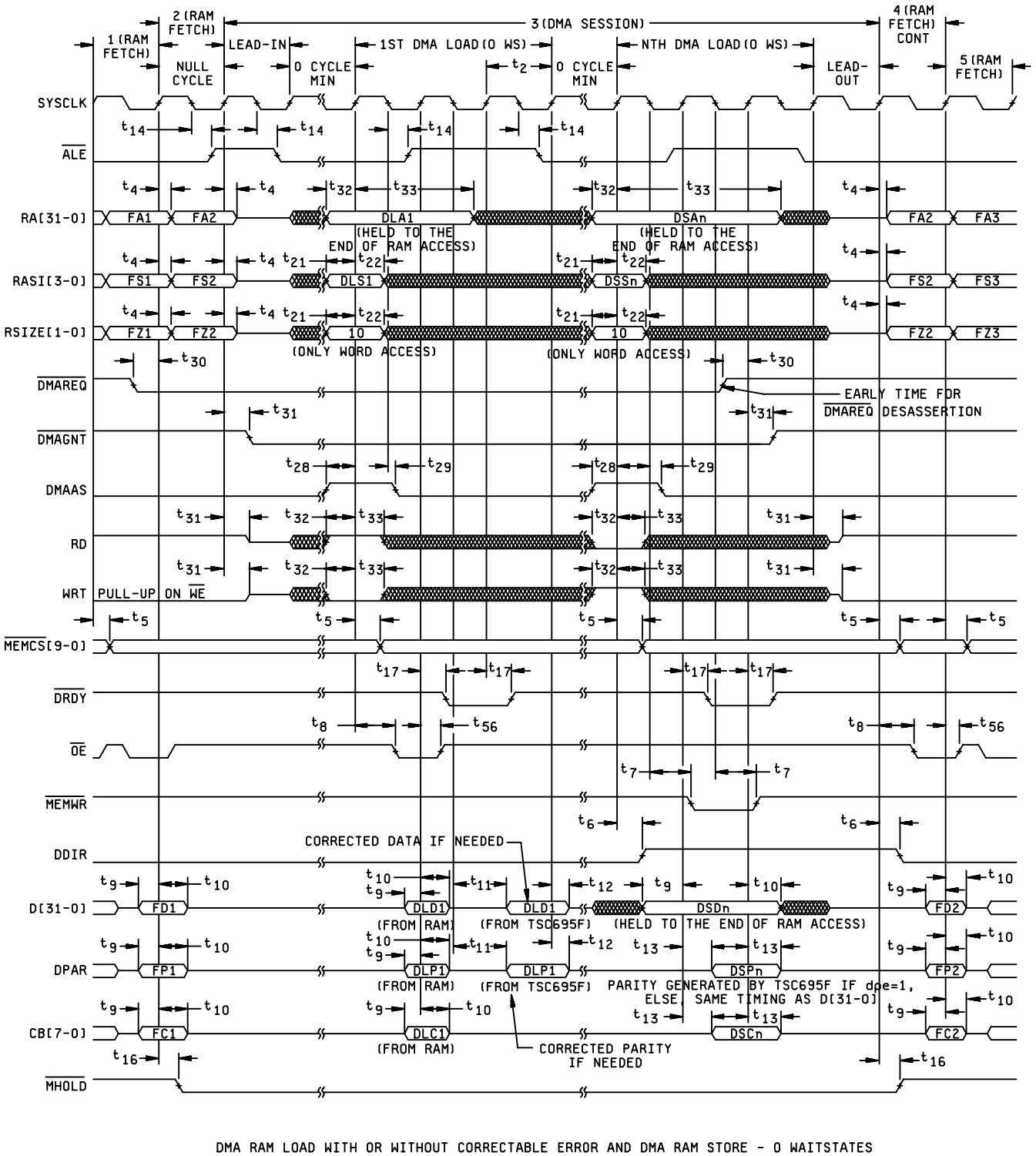
8-BIT BOOT PROM FETCH (OR LOAD WORD) - n WAITSTATES

FIGURE 5. Timing waveforms - Continued.



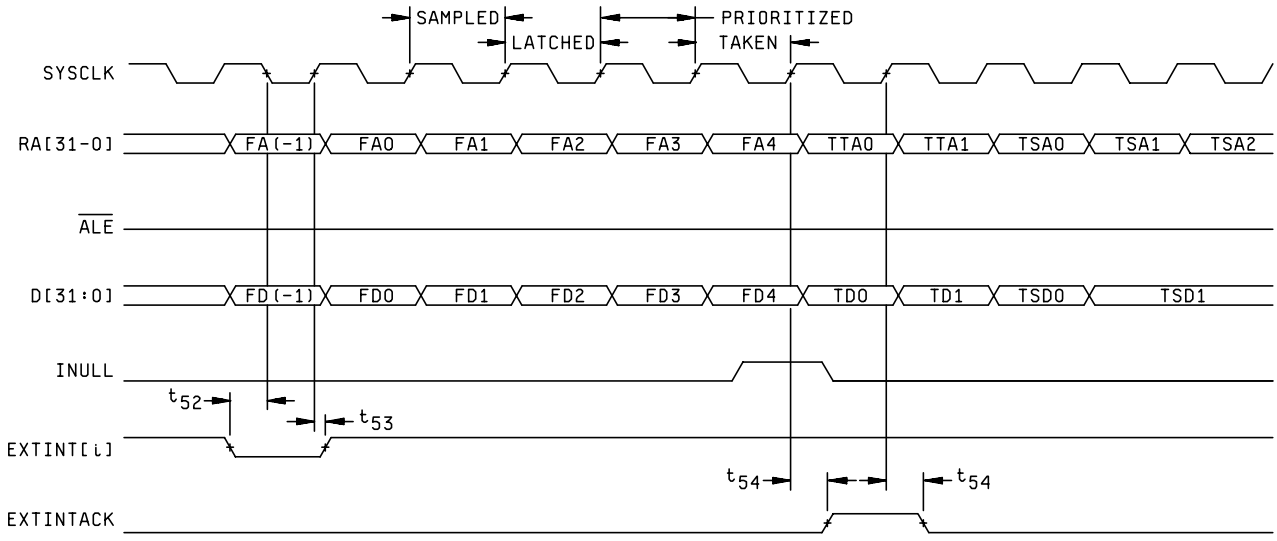
8-BIT BOOT PROM 2x STORE BYTE - n WAITSTATES

FIGURE 5. Timing waveforms - Continued.



DMA RAM LOAD WITH OR WITHOUT CORRECTABLE ERROR AND DMA RAM STORE - 0 WAITSTATES

FIGURE 5. Timing waveforms - Continued.



EDGE TRIGGERED INTERRUPT TIMING

FIGURE 5. Timing waveforms - Continued.

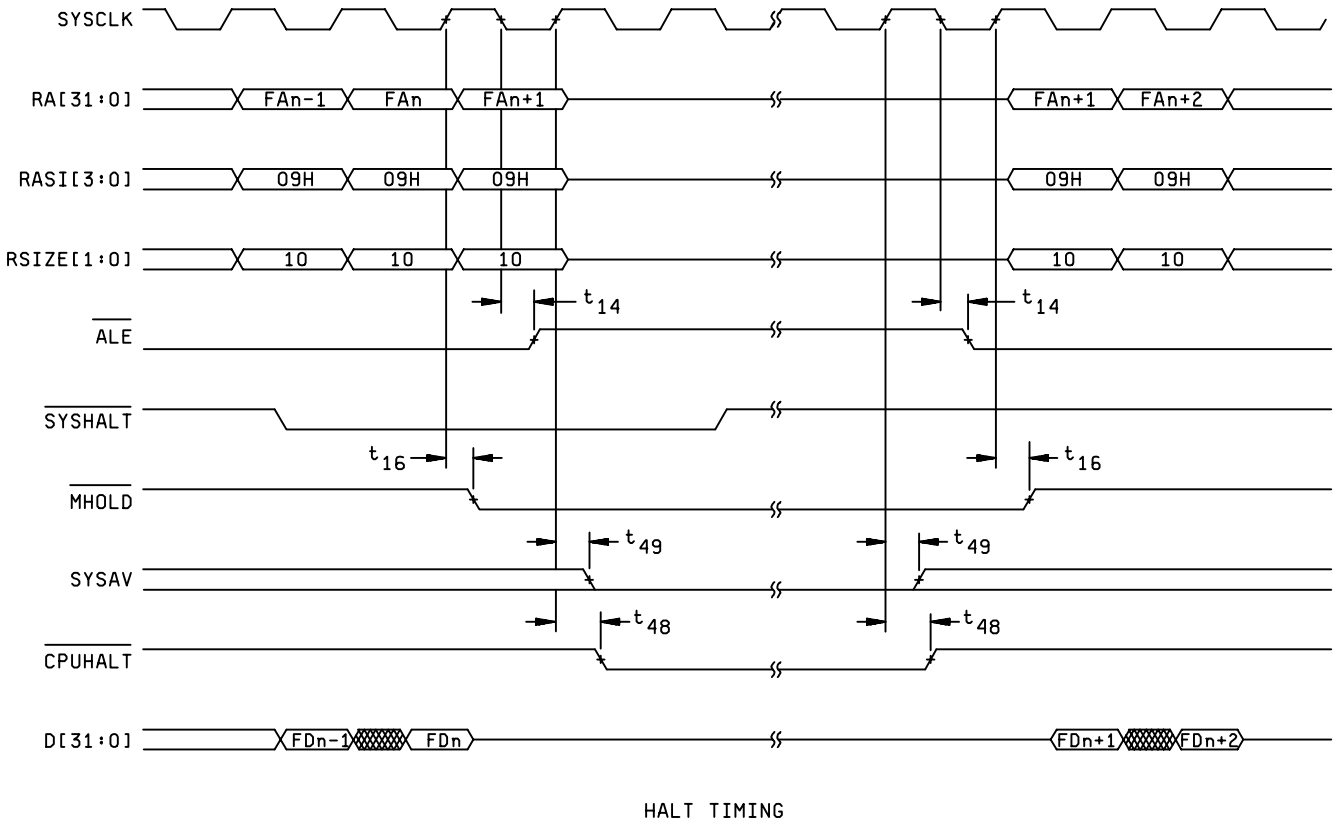
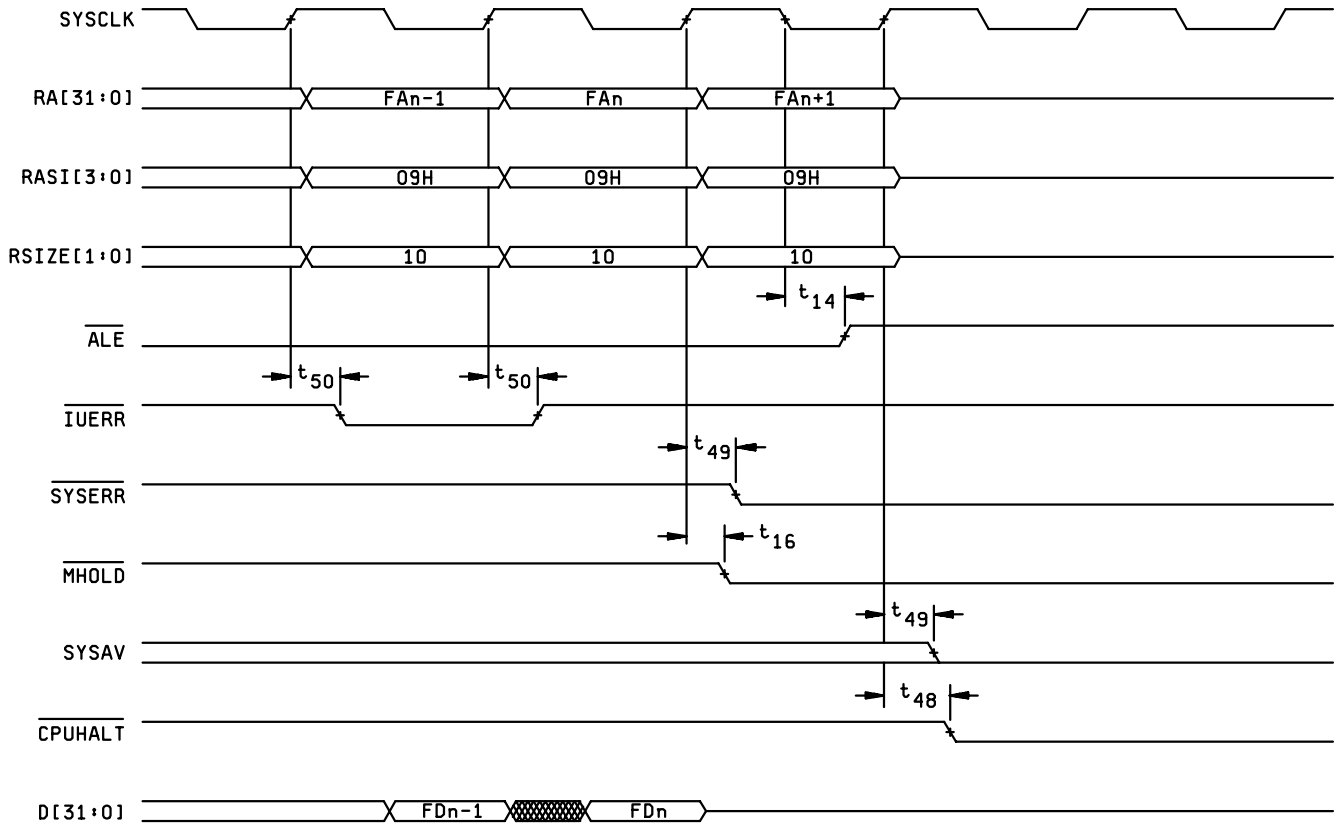
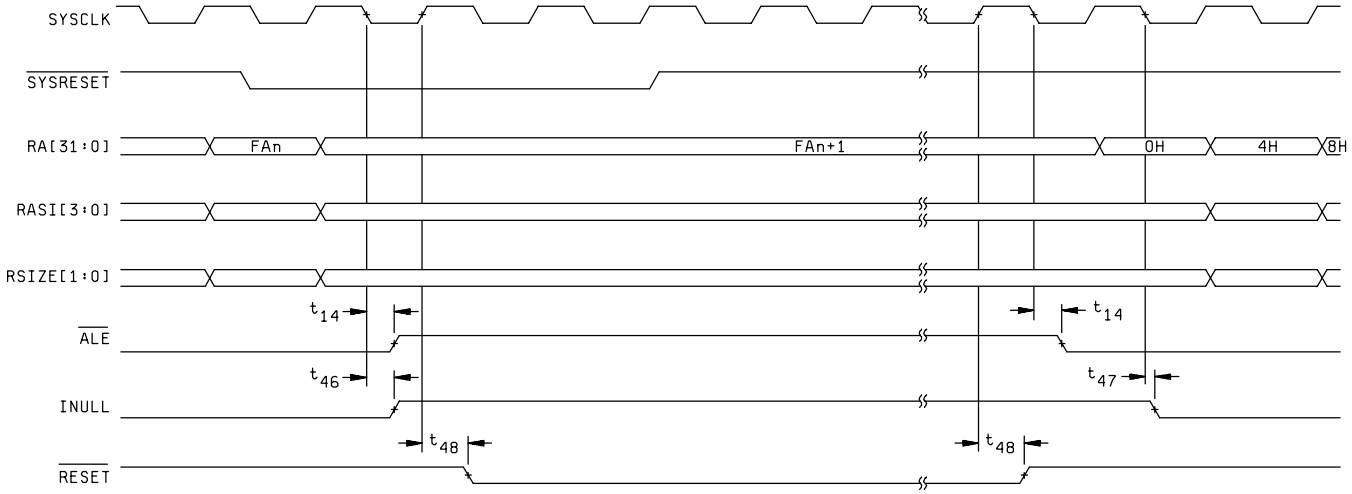


FIGURE 5. Timing waveforms - Continued.



EXTERNAL ERROR WITH HALT TIMING

FIGURE 5. Timing waveforms - Continued.



RESET TIMING

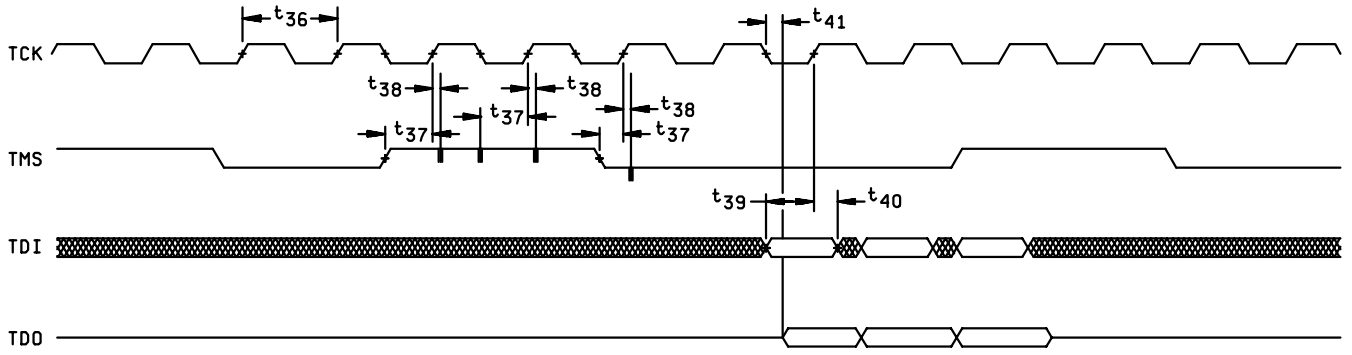


FIGURE 5. Timing waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall verify the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available for review from the approved sources of supply. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 3 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits are as specified in table IIB herein and shall be required where specified in table I.

TABLE IIB. Delta limits.

Parameter 1/	Limit	Unit
V_{OH}	±0.1	V
V_{OL}	±0.1	V
I_{IH}	±0.1	µA
I_{IL}	±0.1	µA
I_{OZH}	±0.1	µA
I_{OZL}	±0.1	µA

1/ The parameters shall be recorded before and after the required burn-in and life test to determine the delta limits.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Terminal descriptions.

Pin name	Type 1/	Description
		IU and FPU Signals
RA[31:0]	I/O	Registered address bus. The address bus for the device is an output bus. Inside the processor, the IU address bus is used to perform decoding, to generate select signals and to check against the memory access protection scheme. It is also used to address the system registers. To save board space, the address bus is sent out registered for external resources. This means that internal D-type flip-flop's are implemented inside the device to memorize the IU address bus at each rising edge of SYSCLK enabled by $\overline{ALE}$ signal. This registered address bus is always driven by the device even during system registers accesses. In case of DMA session, the address bus for the device is an input bus. The DMA unit must drives itself the registered address bus for the available parts of the processor during a DMA session and for the external resources (SRAM's, ROM's, I/O's ....). Organization and addressing of data in memory follows the "Big-Endian" convention wherein lower addresses contain the higher-order bytes. Attempting to access misaligned data will generate a memory-address-not-aligned trap (tt = 7).
RAPAR	I/O	Registered address bus parity. This output is the odd parity over the 32-bit IU address bus. To save board space, this signal is sent out registered and has the same timing as RA[31:0]. In case of DMA session, this signal must be driven by the DMA unit if DMA parity is enabled. This input requires the same timing as RA[31:0].
RASI[3:0]	I/O	4-bit registered address space identifier. These four bits constitute the Address Space Identifier (ASI), which identifies the memory address space to which the instruction or data access is being directed. The ASI bits are provided to detect supervisor or user mode, instruction or data access. Inside the processor, these identifiers are used to control accesses to on-chip peripherals. To save board space, these outputs are sent out registered and has the same timing as RA[31:0]. In case of DMA session, these signals must be driven by the DMA unit. These inputs require the same timing as RA[31:0].
RSIZE[1:0]	I/O	2-bit registered bus transaction size. The coding on these pins specifies the size of the data being transferred during an instruction or a data fetch. To save board space, these outputs are sent out registered and has the same timing as RA[31:0].
RASPAR	I/O	Registered ASI and SIZE parity. This output is the odd parity over the RASI[3:0] and the RSIZE[1:0] signals. To save board space, this output is sent out registered and has the same timing as RA[31:0]. In case of DMA session, this signal must be driven by the DMA unit if DMA parity is enabled. This input requires the same timing as RA[31:0].
CPAR	I/O	Control bus parity. This output is the odd parity over the RLDSTO, DXFER, LOCK, WRT, RD and $\overline{WE}$ signals. This signal is sent out unregistered and must be latched externally before it is used. In case of DMA session, this signal must be driven by the DMA unit if DMA parity is enabled.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
IU and FPU Signals – Continued		
D[31:0]	I/O	32-bit data bus. These signals form a 32-bit bidirectional data bus that serves as the interface between the device and external memory. The data bus is not driven by the device during system registers accesses, it is only driven during the execution of integer and floating-point store instructions and the store cycle of atomic-load-store instructions on external memory. Store data is valid during the second data cycle of a store single access, the second and third data cycle of a store double access, and the third data cycle of an atomic-load-store access. Alignment for load and store instructions is performed by the processor. Doublewords are aligned on 8-byte boundaries, words on 4-byte boundaries, and halfwords on 2-byte boundaries. If a doubleword, word, or halfword load or store instruction generates an improperly aligned address, a memory address not aligned trap will occur. Instructions and operands are always expected to reside in a 32-bit wide memory. D[31] corresponds to the most significant bit of the most significant byte of a 32-bit word going to or from memory.
CB[6:0]	I/O	7-bit check-bit bus. CB[6:0] is the EDAC checkword over the 33-bit data bus consisting of D[31:0] and the parity bit (DPAR). When the device performs a write operation to the main memory, it will assert the EDAC checkword on the CB[6:0]. During read access from the main memory, CB[6:0] are input signals and will be used for checking and correction of the data word and the parity bit. During read access to areas which do not generate a parity bit, the device will latch the data from the accessed address and drive the correct parity bit on the DPAR pin.
DPAR	I/O	Data bus parity. This pin is used by the device to check and generate the odd parity over the 32-bit data bus during write cycles. DPAR = not (D[31] xor D[30] xor .... xor D[1] xor D[0]) In case of DMA session, this signal must be driven by the DMA unit if DMA parity is enabled.
RLDSTO	I/O	Registered atomic load-store. This signal is used to identify an atomic load-store to the system and is asserted by the IU during all the data cycles (the load cycle and both store cycles) of atomic load-store instructions. To save board space, LDSTO is sent out registered. In case of DMA session, this signal must be driven unlatched by the DMA unit.
$\overline{\text{ALE}}$	O	Address latch enable. This output is asserted when the internal address bus from the IU is to be latched. This latch operation is assumed by the internal latch. In case of DMA session, this signal is intended to be used to enable the clock input (SYSCLK) of an external flip-flop used to latch the generated address from DMA unit.
DXFER	I/O	Data transfer. DXFER is used to differentiate between the addresses being sent out for instruction fetches and the addresses of data fetches. DXFER is asserted by the processor during the address cycles of all bus data transfer cycles, including both cycles of store single and all three cycles of store double and atomic load-store. DXFER is sent out unregistered and must be latched externally before it is used. A DMA unit must supply this signal during a DMA session.
LOCK	I/O	Bus lock. LOCK is asserted by the processor when it needs to retain control of the bus (address and data) for multiple cycle transactions (Load Double, Store Single and Double, Atomic Load-Store). The bus will not be granted to another bus master as long as LOCK is asserted. Note that $\overline{\text{MHOLD}}$, when it reflects the internal signal "Bus Hold", should not be asserted in the processor clock cycle which follows a cycle in which LOCK is asserted. LOCK is sent out unregistered and must be latched externally before it is used. A DMA unit must supply this signal during a DMA session.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
		IU and FPU Signals – Continued
RD	I/O	Read access. RD is sent out during the address portion of an access to specify whether the current memory access is a read (RD = "1") or a write (RD = "0") operation. RD is set low only during the address cycles of store instructions. For atomic load-store instructions, RD is set high during the load address cycle and set low during the two store address cycles. RD may be used, in conjunction with SIZE[1:0], ASI[7:0], and LDSTO, to determine the type and to check the read/write access rights of bus transactions in the Extended General area. It is sent out unregistered and must be latched externally before it is used. A DMA unit must supply this signal during a DMA session.
$\overline{\text{MHOLD}}$	O	Memory bus hold. The signal is asserted when a “Memory Hold” (MHOLD), or a “Floating Point Hold” (FHOLD) or a “Floating Point Condition Codes Valid” (FCCV) or a Bus Hold (BHOLD) is internally generated. Note that $\overline{\text{MHOLD}}$ must be driven HIGH while $\overline{\text{RESET}}$ is LOW. • "Memory Hold" "Memory Hold" is used to freeze the pipeline to both the IU and FPU accessing a slow memory or during memory exception. The IU and FPU internal outputs return to and stay at the value they had on the rising edge of SYSCLK in the cycle in which "Memory Hold" was asserted. "Memory Hold" is tested on the falling edge (midpoint of cycle) of SYSCLK. The memory wait state controller of the device inserts, in this way, wait states during external accesses. • "Floating-Point Hold" "Floating-Point Hold" is asserted by the FPU if a situation arises in which the FPU cannot continue execution. The FPU checks all dependencies in the decode stage of the instruction and asserts a "Floating-Point Hold" (if necessary) in the next cycle. If the IU receives a "Floating-Point Hold", it freezes the instruction pipeline in the same cycle. Once the conditions causing the "Floating-Point Hold" are resolved, the FPU deasserts its command, releasing the instruction pipeline. A "Floating-Point Hold" is asserted if: - the FPU encounters an STFSR instruction with one or more FPops pending in the queue, - either a resource or operand dependency exists between the FPop being decoded and any FPops already being executed, - the floating-point queue is full. • "Floating-Point Condition Codes Valid" "Floating-Point Condition Codes Valid" is a specialized hold used to synchronize FPU compare instructions with floating-point branch instructions. It is asserted (the normal condition) whenever the "Floating-Point Condition Codes" bits (FCC[1:0]) are valid. The FPU deasserts these bits (= "0") as soon as a floating-point compare instruction enters the floating-point queue, unless an exception is detected. Deasserting the "Floating-Point Condition Codes" bits freezes the IU pipeline, preventing any further compares from entering the pipeline. The "Floating-Point Condition Codes" bits are reasserted when the compare is completed and the condition codes are valid, thus ensuring that the condition codes match the proper compare instruction. • "Bus Hold" "Bus Hold" is asserted during DMA accesses. Assertion of this hold signal will freeze the processor pipeline, so after deassertion of "Bus Hold", external logic must guarantee that the data at all inputs to the device is the same as it was before "Bus Hold" was asserted. This hold signal is tested on the falling edge (midpoint of cycle) of SYSCLK.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
IU and FPU Signals – Continued		
$\overline{WE}$	I/O	Write enable. $\overline{WE}$ is asserted by the IU during the cycle in which the store data is on the data bus. For a store single instruction, this is during the second store address cycle, the second and third store address cycles of store double instructions and the third load-store address cycle of atomic load-store instructions. To avoid writing to memory during memory exceptions, $\overline{WE}$ must be externally qualified by the $\overline{MHOLD}$, when this holding reflects the internal signal "Memory Hold". It is sent out unregistered and must be latched externally before it is used. A DMA unit must supply this signal during a DMA session, asserted low for write and deasserted high for read accesses.
WRT	I/O	Advanced write. WRT is an early write signal, asserted by the processor during the first store address cycle of integer single or double store instructions, the first store address cycle of floating-point single or double store instructions, and the second load-store address cycle of atomic load-store instructions. WRT is sent out unregistered and must be latched externally before it is used. A DMA unit must supply this signal during a DMA session, deasserted low for read and asserted high for write accesses.
$\overline{MDS}$	O	Memory data strobe. $\overline{MDS}$ is asserted by the memory access controller of the device to enable the clock to the IU's instruction register (during an instruction fetch) or to the load result register (during a data fetch) while the pipeline is frozen with an $\overline{MHOLD}$. In a system with slow memories, $\overline{MDS}$ tells the processor when the read data is available on the bus. $\overline{MDS}$ is also used to strobe in the $\overline{MEXC}$ memory exception signal. $\overline{MDS}$ is only asserted when the pipeline is frozen with $\overline{MHOLD}$.
$\overline{MEXC}$	O	Memory exception. Assertion of this signal by the memory access controller of the device initiates a memory exception and indicates to the IU that the memory system was unable to supply a valid instruction or data. If $\overline{MEXC}$ is asserted during an instruction fetch cycle, it generates an instruction access exception trap (tt=1). If asserted during a data cycle, it generates a data access exception trap (tt=9). It denotes a parity error, uncorrectable EDAC error, access violation, bus time-out or system bus error is detected. $\overline{MEXC}$ is used as a qualifier for the $\overline{MDS}$ signal, and is asserted when both $\overline{MHOLD}$ and $\overline{MDS}$ are already asserted. If $\overline{MDS}$ is applied without $\overline{MEXC}$, the device accepts the contents of the data bus as valid. If $\overline{MEXC}$ accompanies $\overline{MDS}$, an exception is generated and the data bus content is ignored. $\overline{MEXC}$ is latched in the IU on the rising edge of SYSCLK and is used in the following cycle. $\overline{MEXC}$ is deasserted in the same clock cycle in which $\overline{MHOLD}$ is deasserted. If this signal is asserted during a DMA transfer, the DMA must withdraw its DMA request and end the DMA cycle.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
Memory and System Interface Signals		
$\overline{\text{PROM8}}$	I	Select 8-bit wide PROM. This input indicates that only 8-bit wide PROM is connected to the device. The eight data lines from the PROM is to be connected to the D[7:0] signals. The processor will perform an 8-bit to 32-bit conversion when the IU reads from the PROM (the conversion is not visible on data bus). There is no EDAC or parity checking on accesses to the PROM when $\overline{\text{PROM8}}$ is asserted, and EDAC and parity bits must be supplied by the PROM when $\overline{\text{PROM8}}$ is deasserted.
BA[1:0]	O	Latched address used for 8-bit wide boot PROM. These outputs are used when 8-bit wide PROM is connected to the device. During a fetch or 32-bit load access to the PROM, the BA[1:0] will be asserted four times in order to get the four bytes needed to generate a 32-bit word.
$\overline{\text{ROMCS}}$	O	PROM chip select. This output is asserted whenever there is an access to the boot ROM and extended PROM areas. It can be connected directly to the PROM chip select pins.
$\overline{\text{ROMWRT}}$	I	ROM write enable. Assertion of this signal will enable the pwr bit of the Memory Configuration Register (MCNFR). This logic allows the on-board programming (write operations) of the boot PROM when EEPROM or FLASH devices are used.
$\overline{\text{MEMCS[9 : 0]}}$	O	Memory chip select. $\overline{\text{MEMCS[9 : 0]}}$ is asserted during an access to the main memory. $\overline{\text{MEMCS[9 : 8]}}$ are redundant signals, used to substitute any of the nominal memory banks when memory connected to any of $\overline{\text{MEMCS[7 : 0]}}$ malfunctions.
$\overline{\text{MEMWR}}$	O	Memory write. $\overline{\text{MEMWR}}$ is asserted during write access (store) to boot PROM area, extended PROM area, RAM area and extended RAM area. It is intended to be used as write strobe to the memory devices.
$\overline{\text{OE}}$	O	Memory output enable. $\overline{\text{OE}}$ is asserted during fetch or load accesses to the main memory. It is intended to be used to control memory devices with output enable features.
$\overline{\text{BUFFEN}}$	O	Data buffer enable. $\overline{\text{BUFFEN}}$ is asserted during memory accesses excepted in RAM area (RAM area does not needs data buffers). It is intended to be used as buffer enable for data, check and parity bit buffers in the boot PROM area, extended PROM area, exchange memory area, extended RAM area, I/O area, extended I/O area and extended general area if these areas share the same buffers.
DDIR	O	Data buffer direction. DDIR is used for determining the direction of the data buffers enabled by $\overline{\text{BUFFEN}}$. It is valid during all memory accesses. The DDIR is asserted high during store operations.
$\overline{\text{DDIR}}$	O	Data buffer direction. $\overline{\text{DDIR}}$ is used for determining the direction of the data buffers enabled by $\overline{\text{BUFFEN}}$. It is valid during all memory accesses. The DDIR is asserted high during fetch or load operations.
$\overline{\text{IOSEL[3 : 0]}}$	O	I/O chip select. These four select signals are used to enable one of four possible I/O address areas.
$\overline{\text{IOWR}}$	O	I/O and exchange memory write strobe. $\overline{\text{IOWR}}$ is asserted during write operations to the I/O area, extended I/O area and the exchange memory area.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
Memory and System Interface Signals - Continued		
$\overline{\text{EXMCS}}$	O	Exchange memory chip select. $\overline{\text{EXMCS}}$ is asserted when the exchange memory is accessed.
$\overline{\text{BUSRDY}}$	I	Bus ready. $\overline{\text{BUSRDY}}$ is to be generated by a unit in the I/O area, exchange memory area or in the extended areas, which requires extended time when accessed in addition to the preprogrammed number of wait states. (Note however that wait states can not be preprogrammed for units in the extended general area, only for extended I/O, boot PROM and RAM).
Error, DMA, Halt, and Check Signals		
$\overline{\text{BUSERR}}$	I	Bus error. $\overline{\text{BUSERR}}$ is to be generated together with $\overline{\text{BUSRDY}}$ by a unit in the I/O area, exchange memory area or in the extended areas if an error is detected by the accessed unit during an access.
$\overline{\text{DMAREQ}}$	I	DMA request. $\overline{\text{DMAREQ}}$ is to be issued by a unit requesting the access to the processor bus as a master. The device can include a DMA session timeout function preventing the DMA unit to lockout the IU/FPU by asserting DMA request for a long time.
$\overline{\text{DMAGNT}}$	O	DMA grant. $\overline{\text{DMAGNT}}$ is generated by the device as a response to a $\overline{\text{DMAREQ}}$. $\overline{\text{DMAGNT}}$ is sent after that the device has asserted a "Bus Hold". A memory cycle started by the processor is not interrupted by a DMA access before it is finished. The DMA unit has access to all system registers and all integrated peripherals of the device. It has also access to the memory controlled by the memory access controller of the device.
DMAAS	I	DMA address strobe. During DMA transfers (when the external DMA is bus master) this input is used to inform the device that the address from the DMA is valid and that the access cycle shall start. DMAAS can be asserted multiple times during DMA grant.
$\overline{\text{DRDY}}$	O	Data ready during DMA access. During DMA read transfers (when the external DMA is bus master) this output is used to inform the DMA unit that the data are valid. During DMA write transfers this signal indicates that data have been written into memory.
$\overline{\text{IUERR}}$	O	IU error. This signal is asserted when the (master) IU enters the "error mode" state. This happens if a synchronous trap occurs while traps are disabled (the %PSR's et bit = 0). Before it enters the error mode state, the device saves the %PC and %nPC and sets the trap type (tt) for the trap causing the error mode into the %TBR. It then asserts the error signal and halts. The only way to restart a processor which is in the error mode state is to trigger a reset by asserting the $\overline{\text{RESET}}$ signal.
$\overline{\text{CPUHALT}}$	O	Processor (IU & FPU) halt and freeze. This output informs that the IU and the FPU are in "halt" mode. It can be used to halt other units in the system. $\overline{\text{CPUHALT}}$ signal is also used to advise the "freeze" mode generated by the OCD.
$\overline{\text{SYSERR}}$	O	System error. This signal is asserted whenever an unmasked error is set in the Error and Reset Status Register (ERRRSR). It stays asserted until the ERRRSR is cleared. The error can originate from either the IU (IU error ar IU hardware error) or the system registers (system hardware error). $\overline{\text{SYSERR}}$ and $\overline{\text{IUERR}}$ are used to signal to the application system.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
Error, DMA, Halt, and Check Signals - Continued		
$\overline{\text{SYSHALT}}$	I	System halt. Assertion of this pin will halt the device, freezing IU/FPU execution. SYSCLK and internal CLK2 are running but all the timers and watchdog are halted and the UART operation is stopped. DMA accesses are allowed during halt mode. When $\overline{\text{SYSHALT}}$ is deasserted, the previous mode is entered.
SYSAV	O	System availability. This signal is asserted whenever the system is available, i.e. when the sysav bit in the ERRRSR is set and the $\overline{\text{CPUHALT}}$ and $\overline{\text{SYSERR}}$ signals are deasserted. The sysav bit is cleared by reset and is programmable by software.
$\overline{\text{NOPAR}}$	I	No parity. Assertion of this signal will disable the parity checking of all signals related to the device internal buses. The parity generation on the data bus (towards and IO units) is not affected by this signal, but note that parity checking is disabled if $\overline{\text{NOPAR}}$ is asserted. This is a static signal and shall not change when running. When this signal is asserted (no parity), it disables the epa and rpa bits of the Memory Configuration Register (MCNFR) and the pa3, pa2, pa1, and pa0 bits of the I/O Configuration Register.
INULL	O	Integer unit nullify cycle. The processor asserts INULL to indicate that the current memory access is being nullified. It is asserted at the beginning of the cycle in which the address being nullified is active. INULL is used to disable memory exception generation for the current memory access. This means that $\overline{\text{MDS}}$ and $\overline{\text{MEXC}}$ is not be asserted for a memory access in which INULL = 1. INULL is asserted under the following conditions: - during the second data cycle of any store instruction (including Atomic Load-Store) to nullify the second occurrence of the store address, - on all traps, to nullify the third instruction fetch after the trapped instruction. For reset, it nullifies the error-producing address, - on a load in which the hardware interlock is activated, - on JMPL and RETT instructions.
INST	O	Instruction fetch. The INST signal is asserted by the IU whenever a new instruction is being fetched. It is used by the FPU to latch the instruction currently on the internal data bus into an FPU instruction buffer. The FPU have two instruction buffers (D1 and D2) to save the last two fetched instructions. When INST is asserted, a new instruction enters buffer D1 and the instruction that was in D1 moves to buffer D2.
FLUSH	O	FPU instruction flush. This signal is asserted by the IU whenever it takes a trap. FLUSH is used by the FPU to flush the instructions in its instruction buffers. These instructions, as well as the instructions annulled in the IU pipeline, are restarted after the trap handler is finished. If the trap was not caused by a floating-point exception, instructions already in the floating-point queue may continue their execution. If the trap was caused by a floating-point exception, the Fpqueue must be emptied before the FPU can resume execution.
DIA	O	Delay instruction annulled. This signal is asserted when the delay instruction is annulled (c.f. delayed control transfer). This signal is used to trace the IU execution pipe.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
Interrupt, Clock, UART, GPI, Timer, TAP, and Test Signals		
RTC	O	Real time clock counter output. This signal is generated when the delay time has elapsed in the "Real Time Clock Timer". This output is asserted high for one SYSCLK period.
RxA/RxB	I	Receive data UART "A" and "B". RxA is the serial data input for channel A of the UART. RxB is the serial data input for channel B of the UART.
TxA/TxB	O	Transmit data UART "A" and "B". TxA is the serial data output for channel A of the UART. TxB is the serial data output for channel B of the UART.
GPI[7:0]	I/O	General purpose interface. Each pin of the GPI is programmable as input or output
GPIINT	O	General purpose interface interrupt. An edge detection (rising or falling) is made on each GPI input pin configured as input. GPIINT is the result of a logical OR of these detections. This output is asserted high for two SYSCLK periods.
EXTINT[4:0]	I	External interrupt. The five external interrupt inputs are programmable to be level or edge sensitive, and active high (rising) or active low (falling).
EXTINTACK	O	External interrupt acknowledge. EXTINTACK is used for giving acknowledge to an interrupting unit which requires such a signal. It is programmable to which of the five external interrupt inputs it is associated. It is issued as soon as the IU has recognized the interrupt.
IWDE	I	Internal watch dog enable. This static signal commands the multiplexer placed in front of the watch dog timeout interrupt of the "Interrupt Pending Register". To use the internal watch dog, IWDE must set to high. This input set to low enables the input EWDINT for an external watch dog and disables entirely the internal watch dog (not running). The value of IWDE is copied into the "System Control Register" bit 15.
EWDINT	I	External watch dog input interrupt. This input enabled by IWDE receives an external watch dog timeout. Another usage of this input can be an NMI. This input must asserted high for a minimum of two SYSCLK periods.
WDCLK	I	Watch dog clock. WDCLK is the WD clock input but this clock can also be used as a clock input for the UART interface. The clock frequency of WDCLK must be less than the clock frequency of SYSCLK, i.e. $f_{WDCLK} < f_{SYSCLK}$.
CLK2	I	Double frequency clock. CLK2 is the input clock to the device. The frequency of this clock must be twice the clock frequency f_{SYSCLK} used to drive the IU and the FPU. Note that some external timings of the device can be affected by the duty cycle of CLK2.
SYSCLK	O	System clock. SYSCLK is a nominally 50% duty-cycle clock generated by the device from CLK2 and is used for clocking the IU and the FPU as well as other system logic. Note that the timing of the device is referenced by SYSCLK.
$\overline{\text{RESET}}$	O	Output reset. $\overline{\text{RESET}}$ will be asserted when the device is to be synchronously reset. This occurs when either $\overline{\text{SYSRESET}}$ is asserted or the device initiates a reset due to an error or a programming command. The minimum pulse width of $\overline{\text{RESET}}$ is 1024 SYSCLK periods to authorize the implementation of FLASH memories in the application.
$\overline{\text{SYSRESET}}$	I	System input reset. Assertion of this pin will reset the device. Following this assertion, $\overline{\text{RESET}}$ is generated for a minimum of 1024 SYSCLK periods. $\overline{\text{SYSRESET}}$ must be asserted for a minimum of 4 SYSCLK periods.

See footnote at end of table.

TABLE III. Terminal descriptions - Continued.

Pin name	Type 1/	Description
Interrupt, Clock, UART, GPI, Timer, TAP, and Test Signals – Continued		
TMODE[1:0]	I	Factory test mode. This test mode is only dedicated for factory test mode. The user functional mode is: TMODE[1:0] = "00".
DEBUG	I	Software debug mode. DEBUG directly enables the setting of halt bits of the "Timer Control Register" to freeze integrated peripherals. - DEBUG + phlt freeze the internal watch dog and the 2 internal timers, - DEBUG + phlt + ahlt freeze the channel A of the internal UART, - DEBUG + phlt + bhlt freeze the channel B of the internal UART. For final application, this pin must be grounded. This allows to keep software included debug facilities.
TCK	I	Test (JTAG) clock. Test clock for scan registers.
$\overline{\text{TRST}}$	I	Test (JTAG) reset. Asynchronous reset for the TAP controller. For final application, this pin must be grounded.
TMS	I	Test (JTAG) mode select. Selects test mode of the TAP controller.
TDI	I	Test (JTAG) data input. Test scan register data input.
TDO	O	Test (JTAG) data output. Test scan register data output.
Power Signals		
V_{CCO}/V_{CCI}		Power. V_{CCO} pins supply the output and bidirectional pins of the device. V_{CCI} pins supply the input and the main internal circuitry of the device.
V_{SSO}/V_{SSI}		Ground. V_{SSO} pins provide ground return for the output and bidirectional pins of the device. V_{SSI} pins provide ground return for the input and the main internal circuitry of the device.

1/ I = Input; O = Ouput.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-08-02

Approved sources of supply for SMD 5962-00540 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0054001QXC	F7400	TSC695F-25MAMQ
5962-0054001VXC	F7400	TSC695F-25SASV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes SA BP70602 44306 NANTES CEDEX 3, France