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# HM5216805 Series, HM5216405 Series

16 M LVTTTL Interface SDRAM  
100 MHz/83 MHz

1-Mword  $\times$  8-bit  $\times$  2-bank/2-Mword  $\times$  4-bit  $\times$  2-bank

# HITACHI

ADE-203-304E (Z)

Rev. 5.0

November 1, 1997

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## Description

All inputs and outputs are referred to the rising edge of the clock input. The HM5216805 Series, HM5216405 Series are offered in 2 banks for improved performance.

## Features

- 3.3V Power supply
- Clock frequency: 100 MHz/83 MHz (max)
- LVTTTL interface
- Single pulsed  $\overline{\text{RAS}}$
- 2 Banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 1/2/4/8/full page)
  - Interleave (BL = 1/2/4/8)
- Programmable  $\overline{\text{CAS}}$  latency: 1/2/3
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh (L-version)

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## HM5216805 Series, HM5216405 Series

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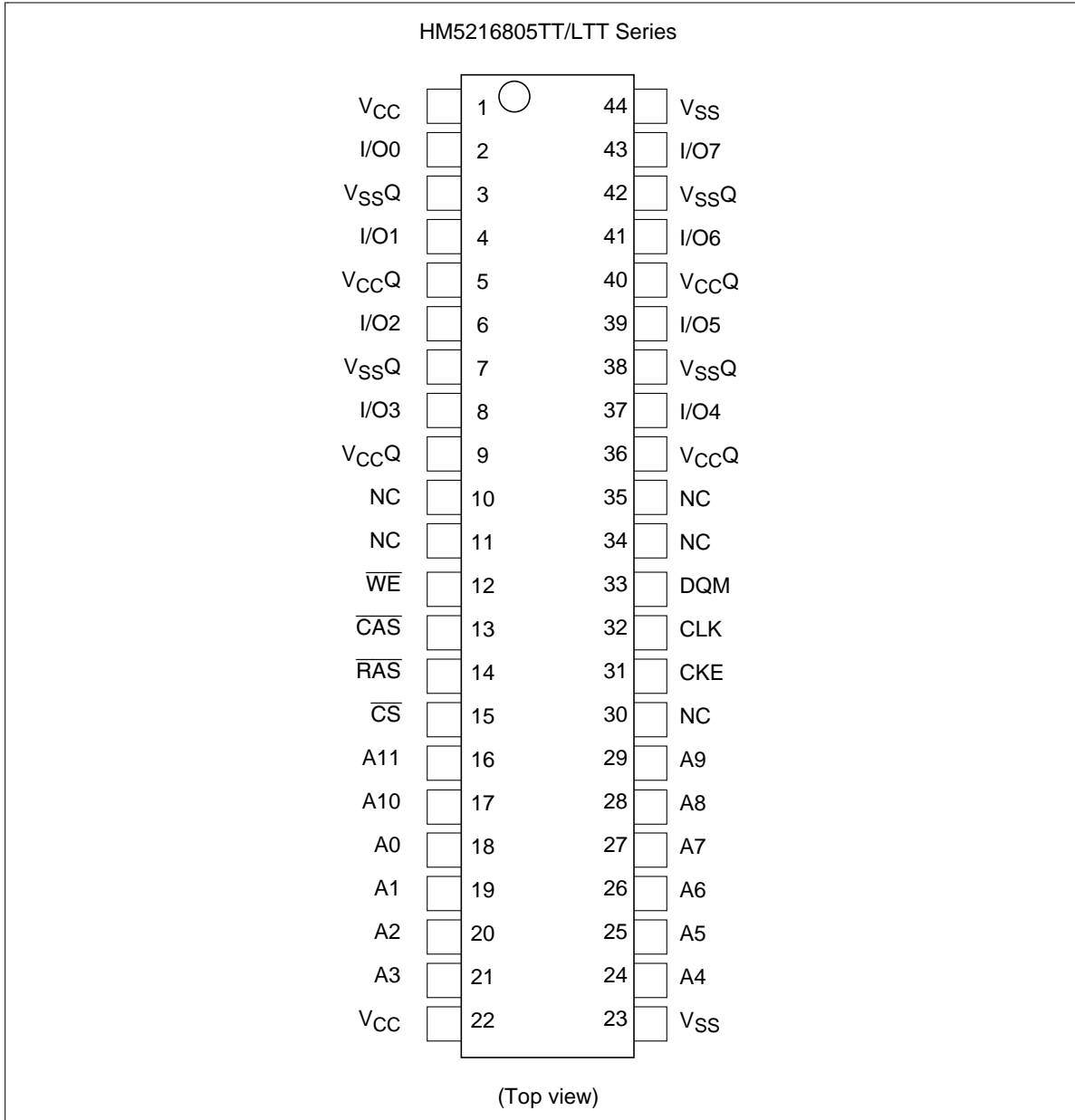
### Ordering Information

Type No.	Frequency	Package
HM5216805TT-10H	100 MHz	400-mil 44-pin plastic TSOP II (TTP-44DE)
HM5216805TT-12	83 MHz	
HM5216805LTT-10H	100 MHz	
HM5216405TT-10H	100 MHz	
HM5216405TT-12	83 MHz	
HM5216405LTT-10H	100 MHz	

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## HM5216805 Series, HM5216405 Series

### Pin Arrangement (HM5216805 Series)



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## HM5216805 Series, HM5216405 Series

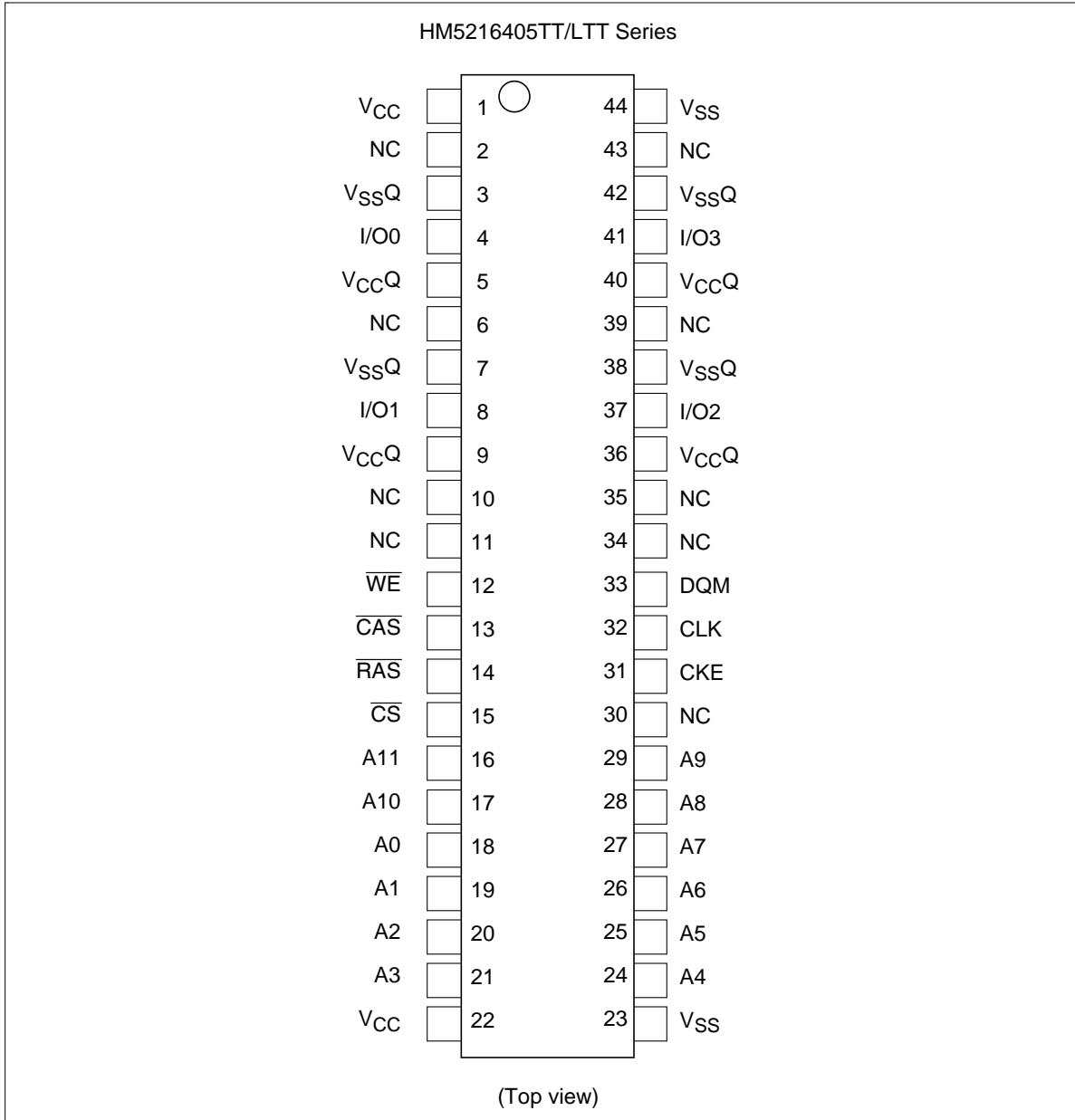
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### Pin Description (HM5216805 Series)

Pin name	Function
A0 to A11	Address input Row address    A0 to A10 Column address A0 to A8 Bank select address    A11
I/O0 to I/O7	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQM	Input/output mask
CLK	Clock input
CKE	Clock enable
$V_{CC}$	Power for internal circuit
$V_{SS}$	Ground for internal circuit
$V_{CCQ}$	Power for I/O pin
$V_{SSQ}$	Ground for I/O pin
NC	No connection

## HM5216805 Series, HM5216405 Series

### Pin Arrangement (HM5216405 Series)



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## HM5216805 Series, HM5216405 Series

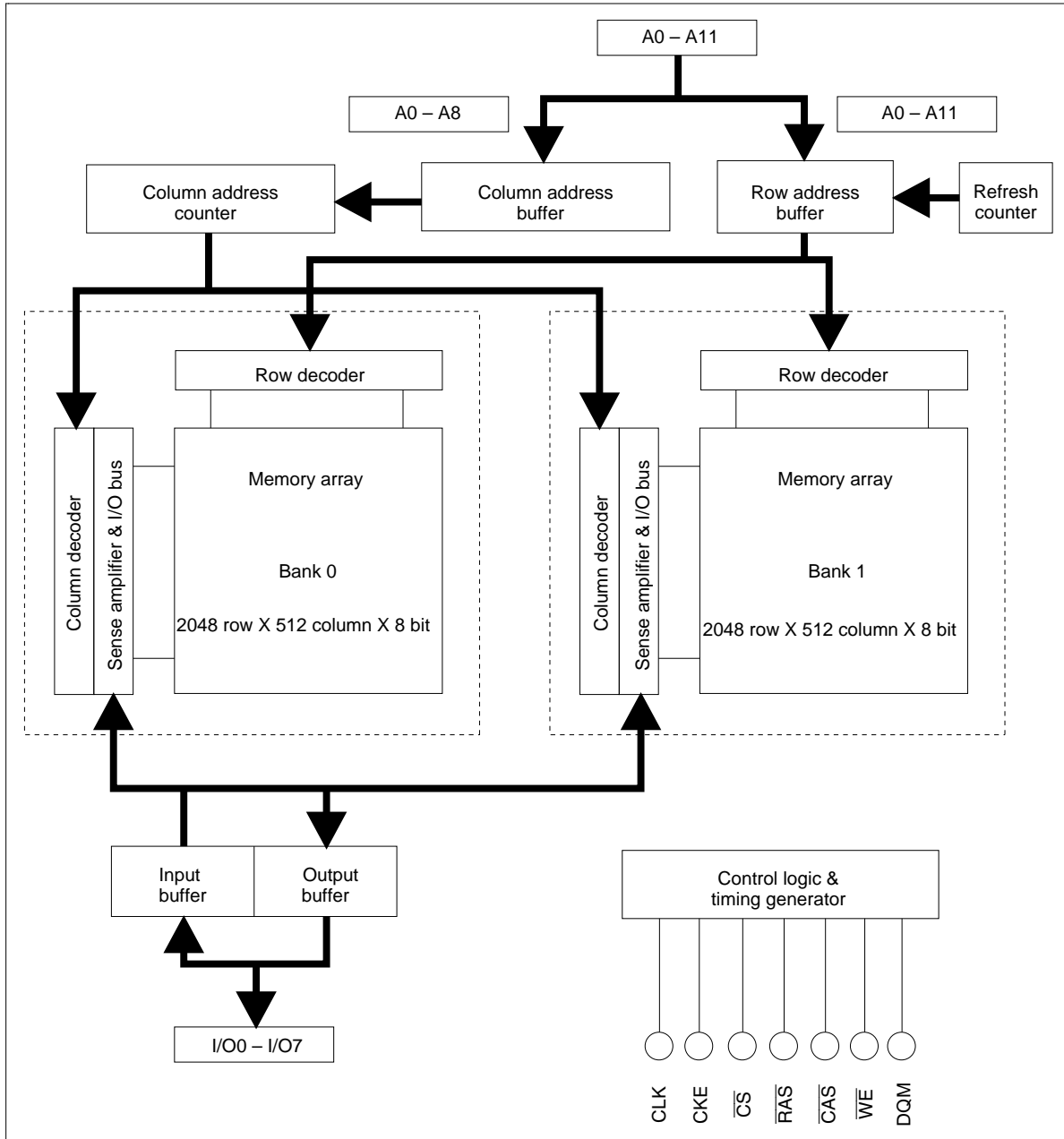
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### Pin Description (HM5216405 Series)

Pin name	Function
A0 to A11	Address input Row address    A0 to A10 Column address A0 to A9 Bank select address    A11
I/O0 to I/O3	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQM	Input/output mask
CLK	Clock input
CKE	Clock enable
$V_{CC}$	Power for internal circuit
$V_{SS}$	Ground for internal circuit
$V_{CCQ}$	Power for I/O pin
$V_{SSQ}$	Ground for I/O pin
NC	No connection

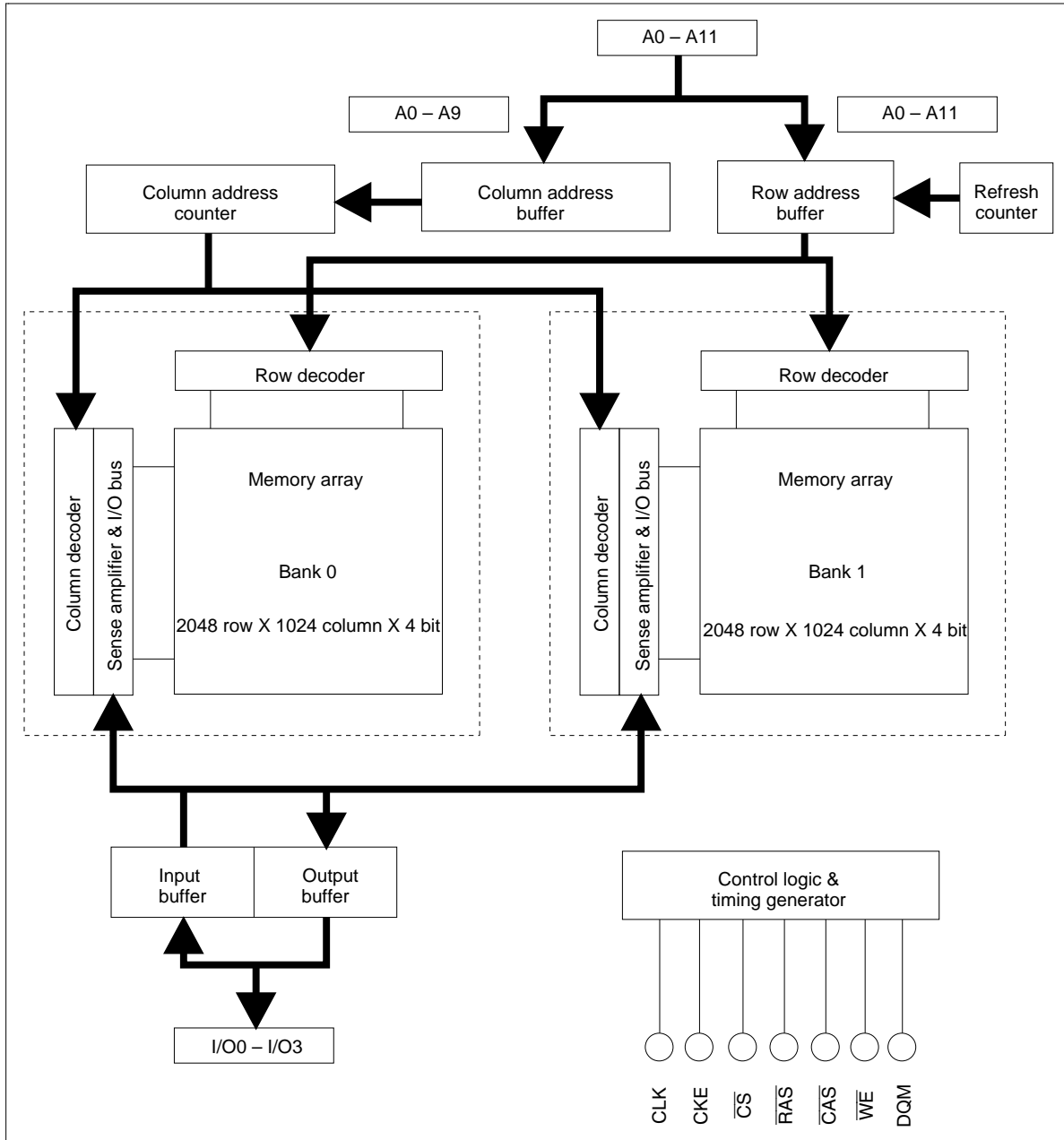
# HM5216805 Series, HM5216405 Series

## Block Diagram (HM5216805 Series)



# HM5216805 Series, HM5216405 Series

## Block Diagram (HM5216405 Series)





### Pin Functions

**CLK (input pin):** CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

**$\overline{CS}$  (input pin):** When  $\overline{CS}$  is Low, the command input cycle becomes valid. When  $\overline{CS}$  is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

**$\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  (input pins):** Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

**A0 to A10 (input pins):** Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) is determined by A0 to A8 or A9 (A8; HM5216805 Series, A9; HM5216405 Series) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11(BS) is precharged.

**A11 (input pin):** A11 is a bank select signal (BS). The memory array of the HM5216805 Series, the HM5216405 Series is divided into bank 0 and bank 1. HM5216805 Series contain 2048 row  $\times$  512 column  $\times$  8 bits. HM5216405 Series contain 2048 row  $\times$  1024 column  $\times$  4 bits. If A11 is Low, bank 0 is selected, and if A11 is High, bank 1 is selected.

**CKE (input pin):** This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

**DQM (input pins):** DQM controls input/output buffers.

Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z.

Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.

**I/O0 to I/O7 (I/O pins):** Data is input to and output from these pins. These pins are the same as those of a conventional DRAM.

**$V_{CC}$  and  $V_{CCQ}$  (power supply pins):** 3.3 V is applied. ( $V_{CC}$  is for the internal circuit and  $V_{CCQ}$  is for the output buffer.)

**$V_{SS}$  and  $V_{SSQ}$  (power supply pins):** Ground is connected. ( $V_{SS}$  is for the internal circuit and  $V_{SSQ}$  is for the output buffer.)

## HM5216805 Series, HM5216405 Series

### Command Operation

#### Command Truth Table

The synchronous DRAM recognizes the following commands specified by the  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and address pins.

Function	Symbol	CKE		CS	RAS	CAS	WE	A11	A10	A0 to A9
		n - 1	n							
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop in full page	BST	H	×	L	H	H	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ . V: Valid address input

**Ignore command [DESL]:** When this command is set ( $\overline{CS}$  is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

**No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

**Burst stop in full-page [BST]:** This command stops a full-page burst operation (burst length = full-page (512; HM5216805 Series, 1024; HM5216405 Series)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for a full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

**Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

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## HM5216805 Series, HM5216405 Series

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**Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8. When the burst length is full-page, this command is illegal.

**Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (A11).

**Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

**Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11 (BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated.

**Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

**Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

**Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

**Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

### DQM Truth Table

Function	Symbol	CKE		DQM
		n – 1	n	
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ .

The HM5216805 Series, HM5216405 Series can mask input/output data by means of DQM. During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the HM5216805 Series, HM5216405 Series operating instructions.

## HM5216805 Series, HM5216405 Series

**CKE Truth Table**

Current state	Function	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address
		n - 1	n					
Active	Clock suspend mode entry	H	L	H	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×
Idle	Auto-refresh command REF	H	H	L	L	L	H	×
Idle	Self-refresh entry SELF	H	L	L	L	L	H	×
Idle	Power down entry	H	L	L	H	H	H	×
		H	L	H	×	×	×	×
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	×
		L	H	H	×	×	×	×
Power down	Power down exit	L	H	L	H	H	H	×
		L	H	H	×	×	×	×

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$ .

**Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

**ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

**READ suspend and READ A suspend:** The data being output is held (and continues to be output).

**WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

**Clock suspend:** During clock suspend mode, keep the CKE to Low.

**Clock suspend mode exit:** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

**IDLE:** In this state, all banks are not selected, and completed precharge operation.

**Auto-refresh command [REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

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## HM5216805 Series, HM5216405 Series

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**Self-refresh entry [SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

**Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

**Self-refresh exit:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

**Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

## HM5216805 Series, HM5216405 Series

### Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after $t_{RP}$
	L	H	H	H	×	NOP	Enter IDLE after $t_{RP}$
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

## HM5216805 Series, HM5216405 Series

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank* <sup>3</sup>
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank* <sup>3</sup>
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank* <sup>3</sup>
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and Precharge* <sup>2</sup>
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

## HM5216805 Series, HM5216405 Series

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank <sup>3</sup>
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	×	×	×	×	DESL	Enter IDLE after $t_{RC}$
	L	H	H	H	×	NOP	Enter IDLE after $t_{RC}$
	L	H	H	L	×	BST	Enter IDLE after $t_{RC}$
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ .

The other combinations are inhibit.

2. An interval of  $t_{DPL}$  is required between the final valid data input and the precharge command.
3. If  $t_{RRD}$  is not satisfied, this operation is illegal.

### From [PRECHARGE]

**To [DESL], [NOP] or [BST]:** When these commands are executed, the synchronous DRAM enters the IDLE state after  $t_{RP}$  has elapsed from the completion of precharge.

### From [IDLE]

**To [DESL], [NOP], [BST], [PRE] or [PALL]:** These commands result in no operation.

**To [ACTV]:** The bank specified by the address pins and the ROW address is activated.

**To [REF], [SELF]:** The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

**To [MRS]:** The synchronous DRAM enters the mode register set cycle.



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## HM5216805 Series, HM5216405 Series

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### From [ROW ACTIVE]

**To [DESL], [NOP] or [BST]:** These commands result in no operation.

**To [READ], [READ A]:** A read operation starts. (However, an interval of  $t_{RCD}$  is required.)

**To [WRIT], [WRIT A]:** A write operation starts. (However, an interval of  $t_{RCD}$  is required.)

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands set the synchronous DRAM to precharge mode. (However, an interval of  $t_{RAS}$  is required.)

### From [READ]

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** Data output by the previous read command continues to be output. After  $\overline{\text{CAS}}$  latency, the data output resulting from the next command will start.

**To [WRIT], [WRIT A]:** These commands stop a burst read, and start a write cycle.

**To [ACTV]:** This command makes other banks bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop a burst read, and the synchronous DRAM enters precharge mode.

### From [READ with AUTO-PRECHARGE]

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

**To [ACTV]:** This command makes other banks bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

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## HM5216805 Series, HM5216405 Series

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### From [WRITE]

**To [DESL], [NOP]:** These commands continue write operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** These commands stop a burst and start a read cycle.

**To [WRIT], [WRIT A]:** These commands stop a burst and start the next write cycle.

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop burst write and the synchronous DRAM then enters precharge mode.

### From [WRITE with AUTO-PRECHARGE]

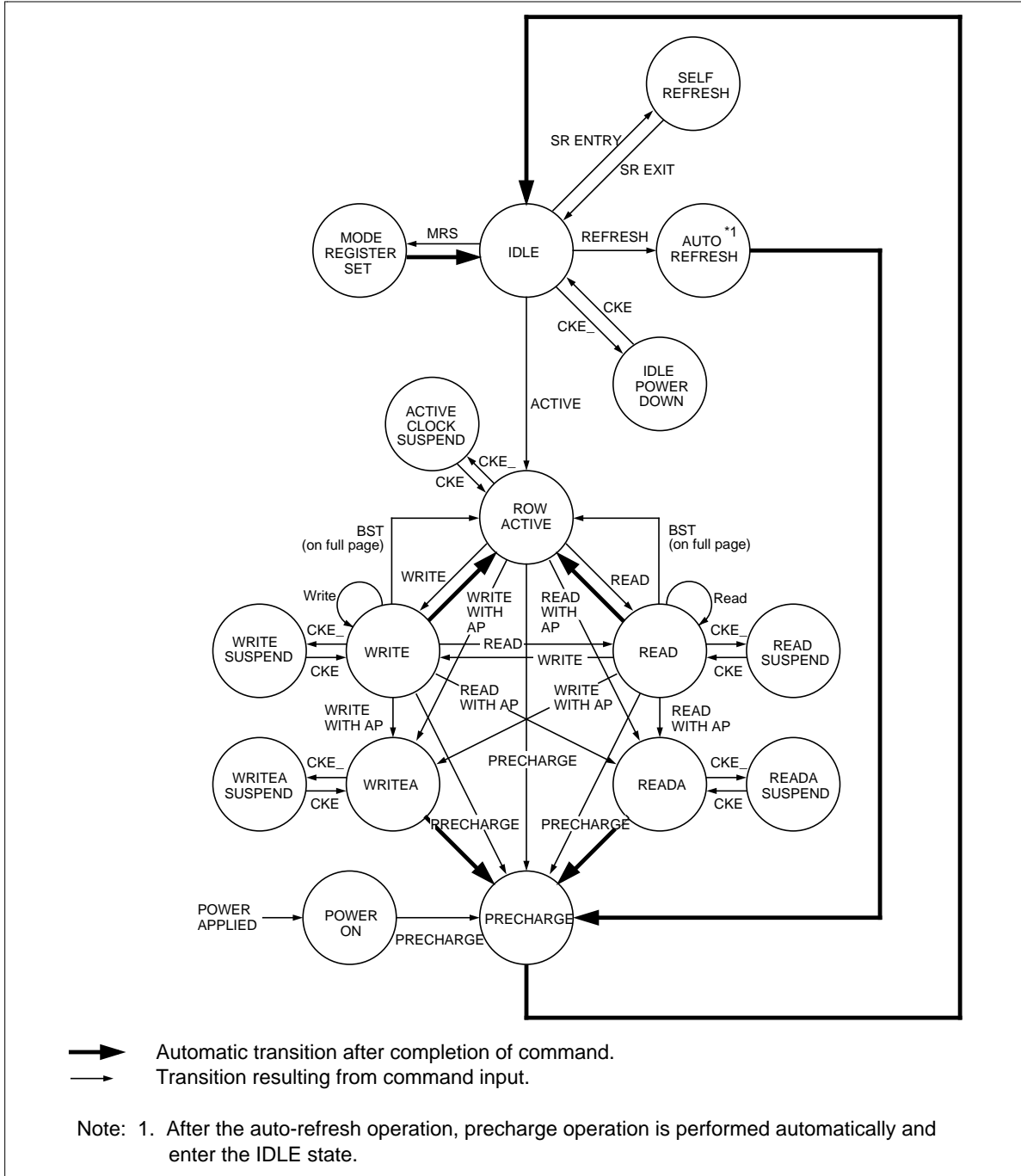
**To [DESL], [NOP]:** These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RC}$  is required.) Attempting to make the currently active bank active results in an illegal command.

### From [REFRESH]

**To [DESL], [NOP]:** After an auto-refresh cycle (after  $t_{RC}$ ), the synchronous DRAM automatically enters the IDLE state.

Simplified State Diagram



## HM5216805 Series, HM5216405 Series

### Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

**A11, A10, A9, A8 (OPCODE):** The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

**Burst read and BURST WRITE:** Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

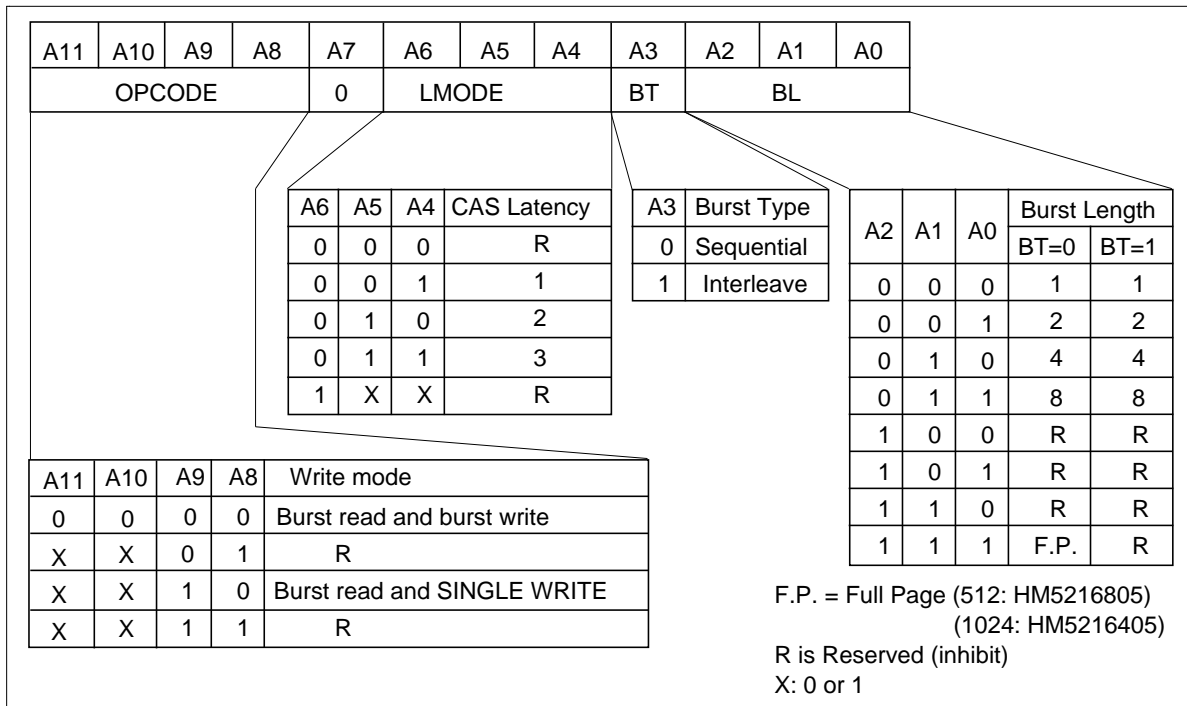
**Burst read and SINGLE WRITE:** Data is only written to the column address specified during the write cycle, regardless of the burst length.

**A7:** Keep this bit Low at the mode register set cycle.

**A6, A5, A4 (LMODE):** These pins specify the  $\overline{\text{CAS}}$  latency.

**A3 (BT):** A burst type is specified. When full-page burst is performed, only “sequential” can be selected.

**A2, A1, A0 (BL):** These pins specify the burst length.



## HM5216805 Series, HM5216405 Series

### Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

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## HM5216805 Series, HM5216405 Series

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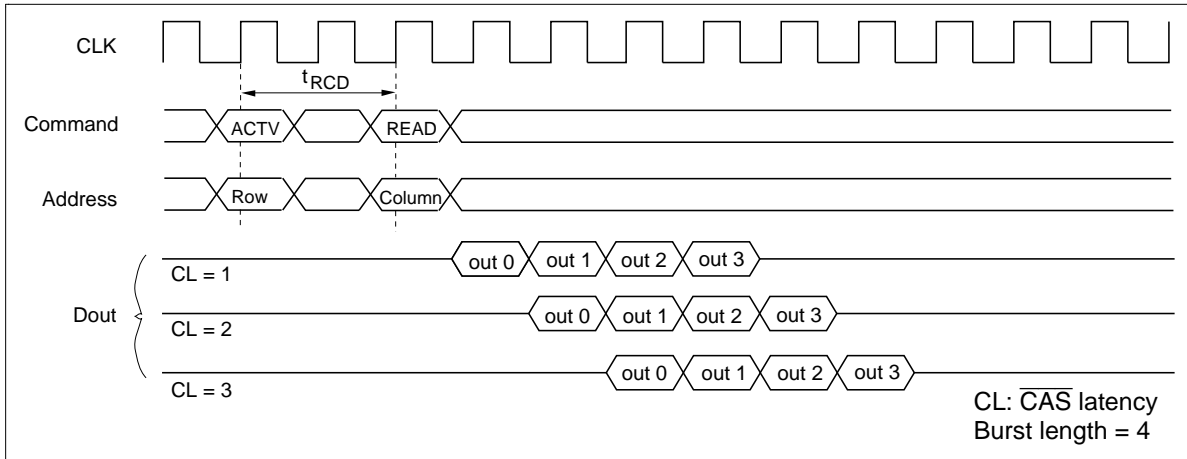
### Operation of HM5216805 Series, HM5216405 Series

#### Read/Write Operations

**Bank active:** Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A11 pin, and the row address (AX0 to AX10) is activated by the A0 to A10 pins at the bank active command cycle. An interval of  $t_{RCD}$  is required between the bank active command input and the following read/write command input.

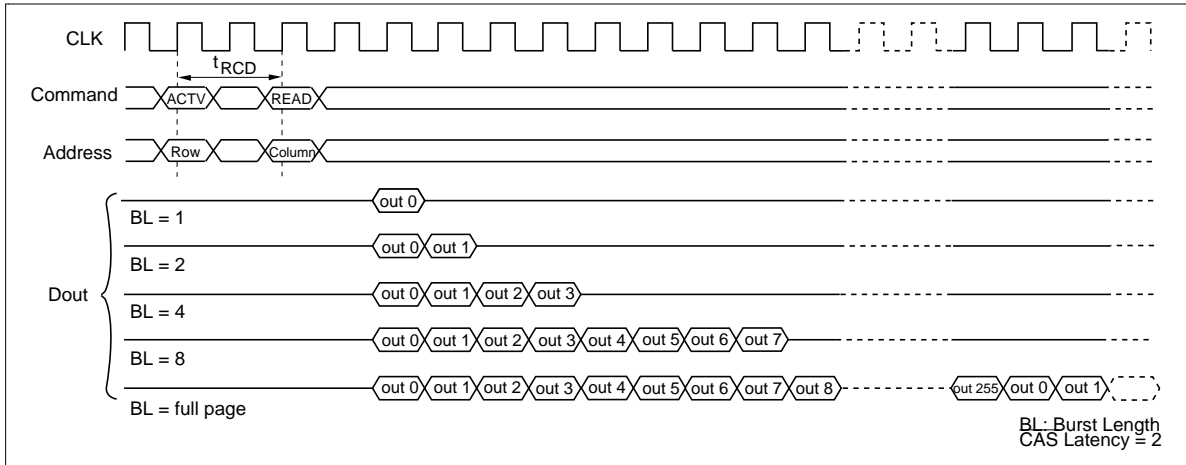
**Read operation:** A read operation starts when a read command is input. Output buffer becomes Low-Z in the ( $\overline{\text{CAS}}$  Latency - 1) cycle after read command set. HM5216805 Series, HM5216405 Series can perform a burst read operation. The burst length can be set to 1, 2, 4, 8 or full-page (512; HM5216805 Series, 1024; HM5216405 Series). The start address for a burst read is specified by the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (A11) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the  $\overline{\text{CAS}}$  Latency. The  $\overline{\text{CAS}}$  Latency can be set to 1, 2 or 3. When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output. When the burst length is full-page (512; HM5216805 Series, 1024; HM5216405 Series), data is repeatedly output until the burst stop command is input. The CAS latency and burst length must be specified at the mode register.

#### $\overline{\text{CAS}}$ Latency



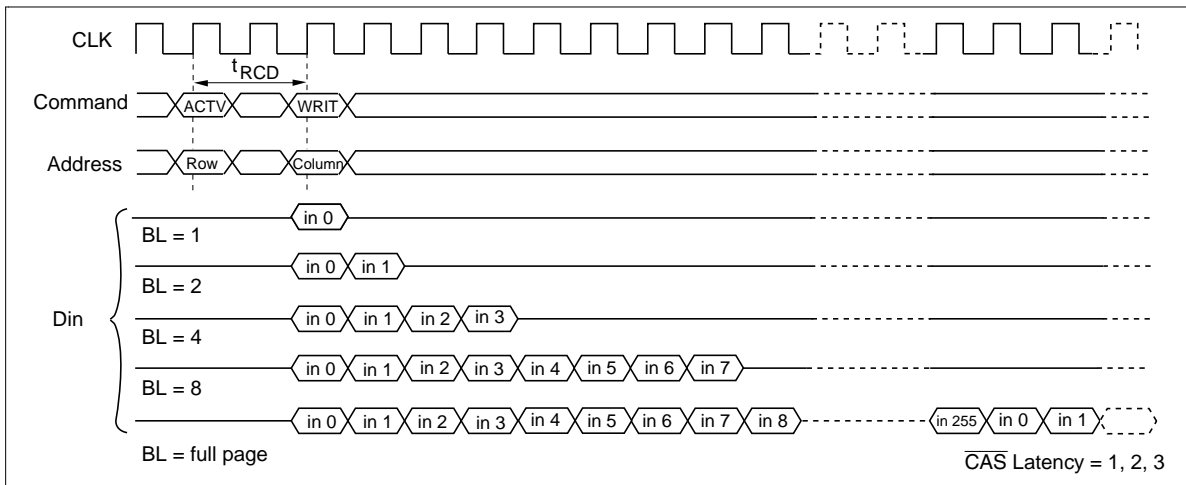
## HM5216805 Series, HM5216405 Series

### Burst Length



**Write operation:** Burst write or single write mode is selected by the OPCODE (A11, A10, A9, A8) of the mode register.

**Burst write:** A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4 or 8 and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (A11) at the write command set cycle.

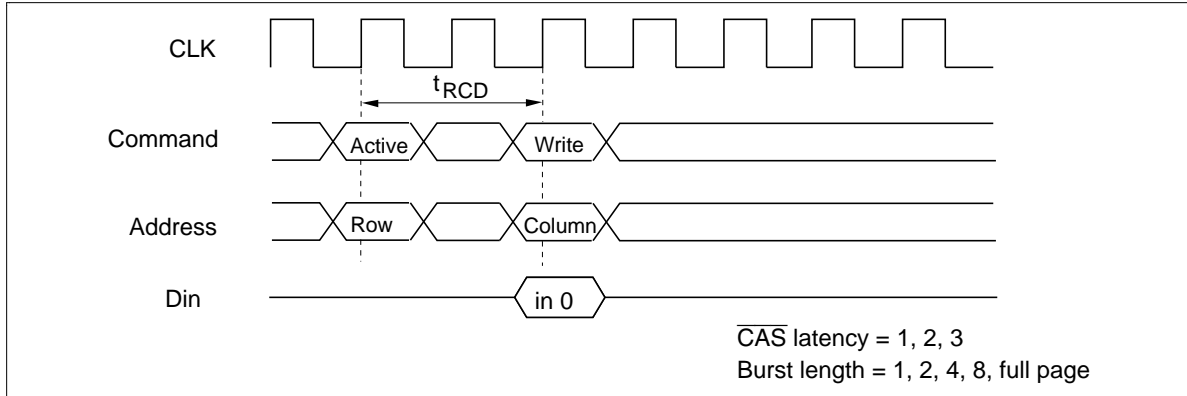


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## HM5216805 Series, HM5216405 Series

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**Single write:** A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY8; HM5216805 Series, AY0 to AY9; HM5216405 Series) and the bank select address (A11) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).



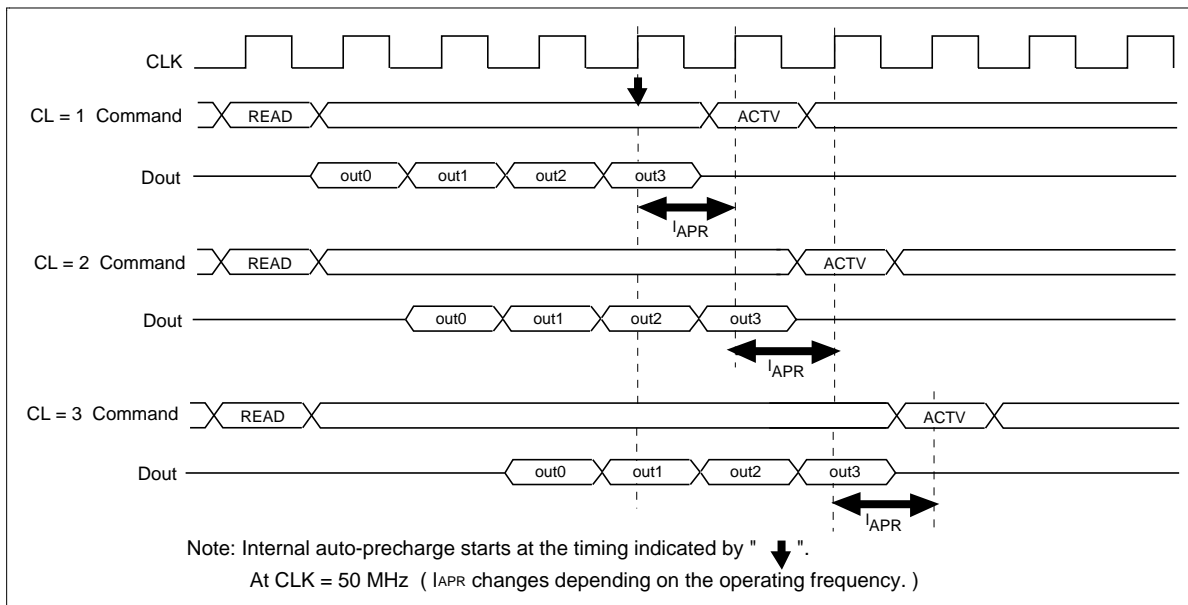


## HM5216805 Series, HM5216405 Series

### Auto-precharge

**Read with auto-precharge:** In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by  $I_{APR}$  is required before execution of the next command.

$\overline{\text{CAS}}$ latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output
1	same cycle as the final data is output



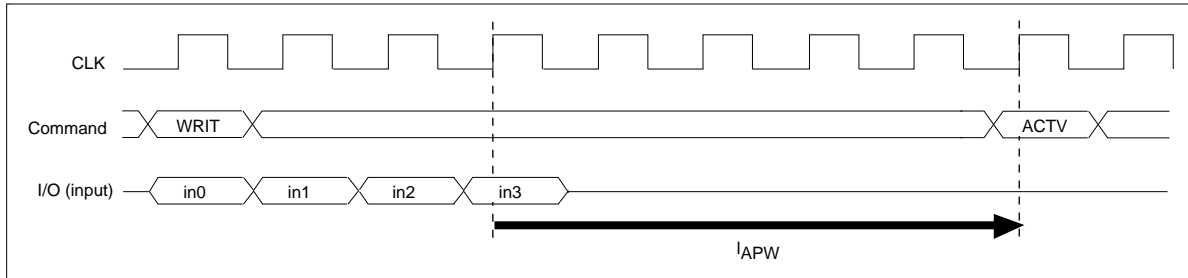
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## HM5216805 Series, HM5216405 Series

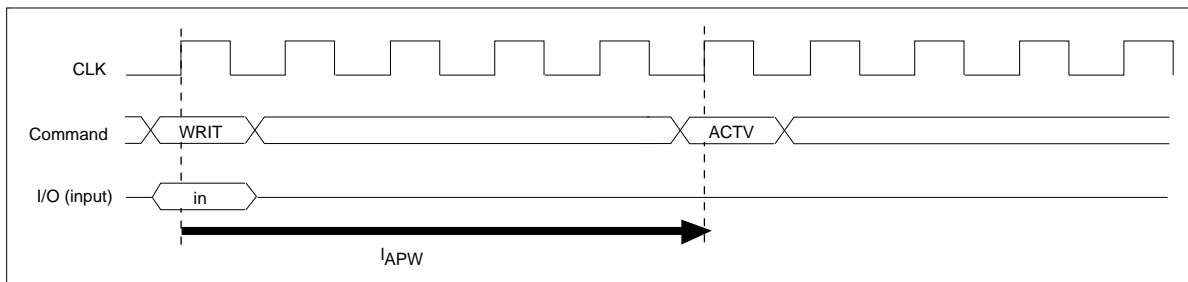
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**Write with auto-precharge:** In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of  $t_{APW}$  is required between the final valid data input and input of the next command.

### Burst Write (Burst Length = 4)



### Single Write



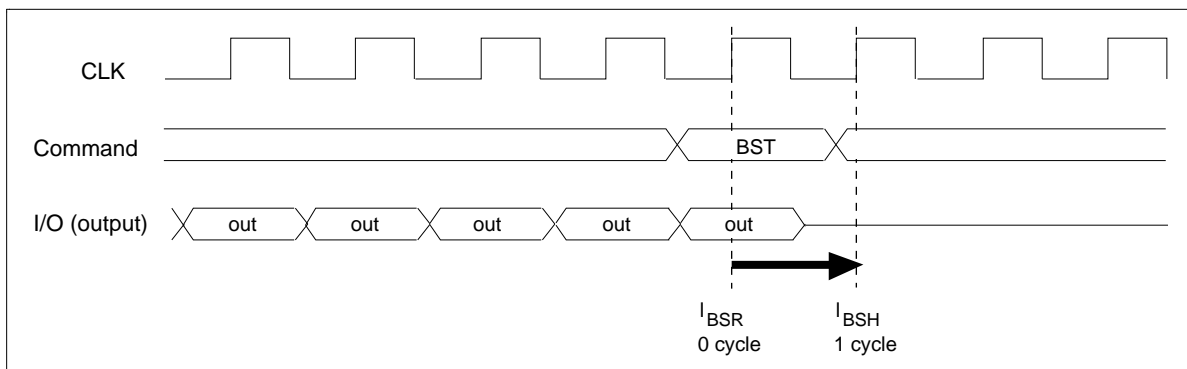
## HM5216805 Series, HM5216405 Series

### Full-page Burst Stop

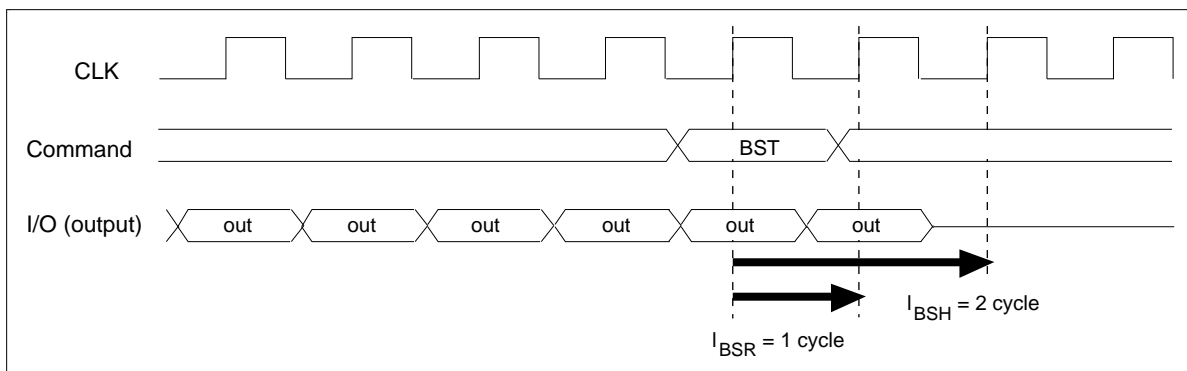
**Burst stop command during burst read:** The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the  $\overline{\text{CAS}}$  latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4 and 8.

$\overline{\text{CAS}}$ latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	2	3

#### $\overline{\text{CAS}}$ Latency = 1, Burst Length = full page

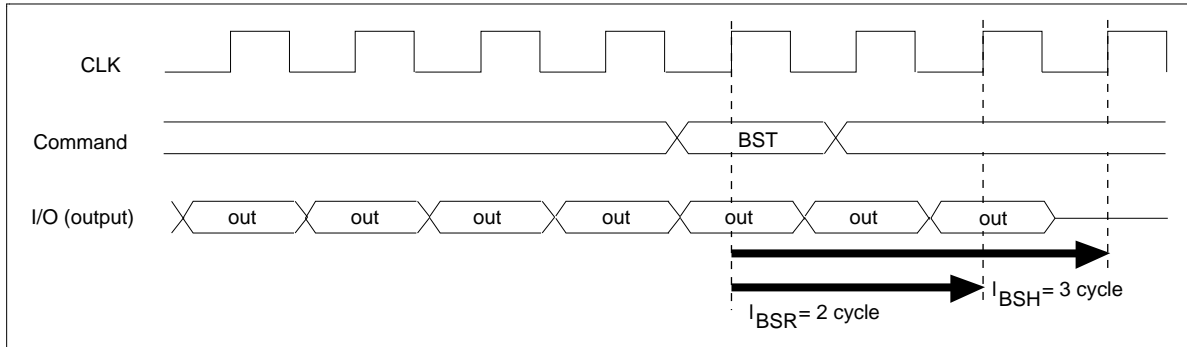


#### $\overline{\text{CAS}}$ Latency = 2, Burst Length = full page



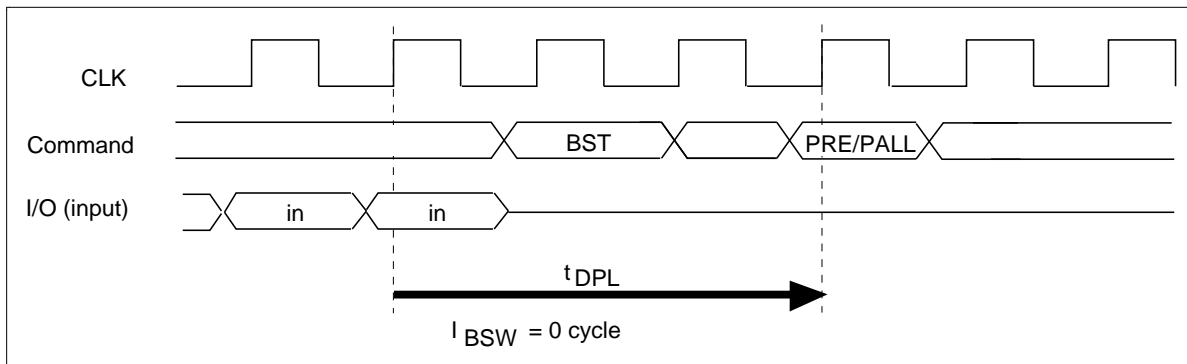
## HM5216805 Series, HM5216405 Series

$\overline{\text{CAS}}$  Latency = 3, Burst Length = full page



**Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command, and in subsequent cycles. In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4 and 8. And an interval of  $t_{DPL}$  is required between the BST command and the next precharge command.

**Burst Length = full page**

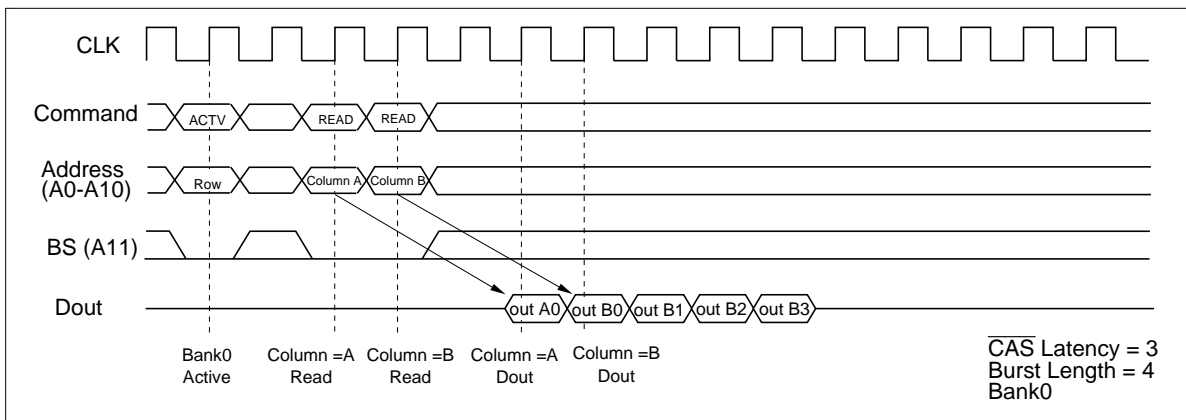


**Command Intervals**

**Read command to Read command interval**

**Same bank, same ROW address:** When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

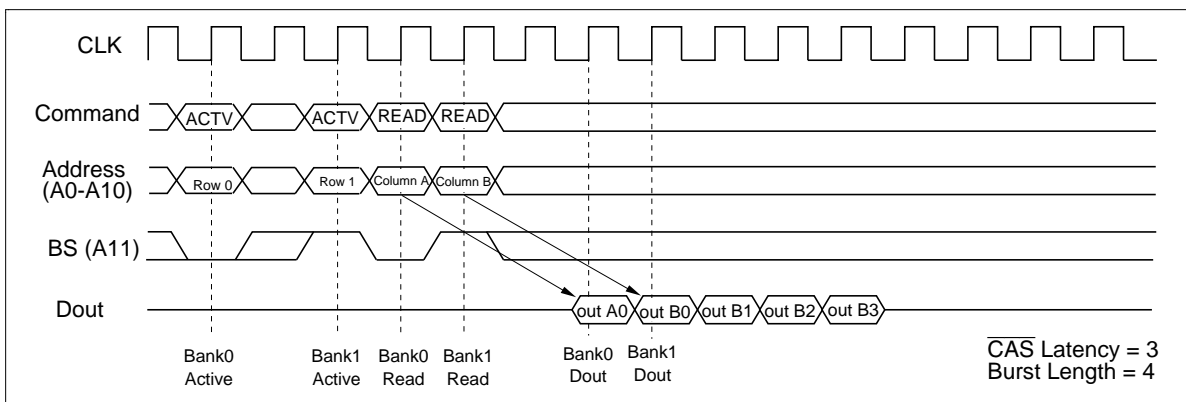
**READ to READ Command Interval (same ROW address in same bank)**



**Same bank, different ROW address:** When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

**Different bank:** When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

**READ to READ Command Interval (different bank)**

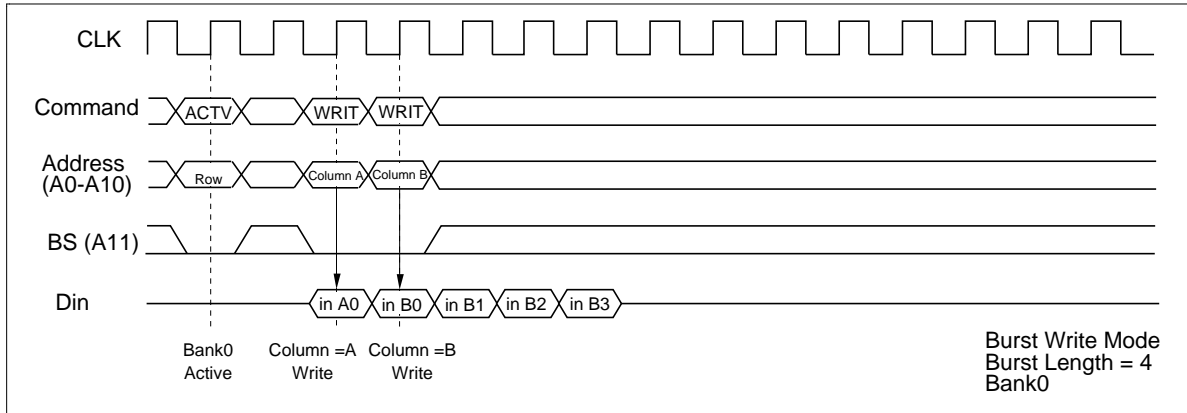


## HM5216805 Series, HM5216405 Series

### Write command to Write command interval

**Same bank, same ROW address:** When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

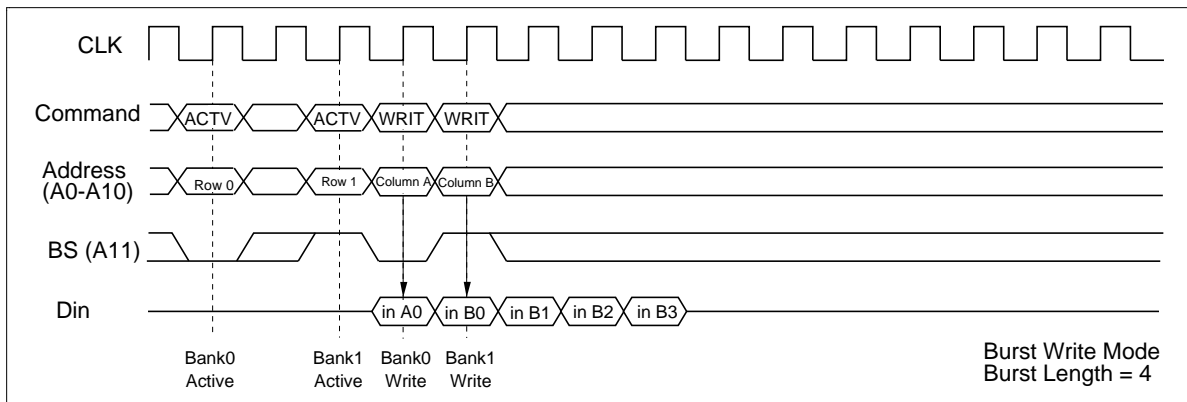
#### WRITE to WRITE Command Interval (same ROW address in same bank)



**Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

**Different bank:** When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

#### WRITE to WRITE Command Interval (different bank)

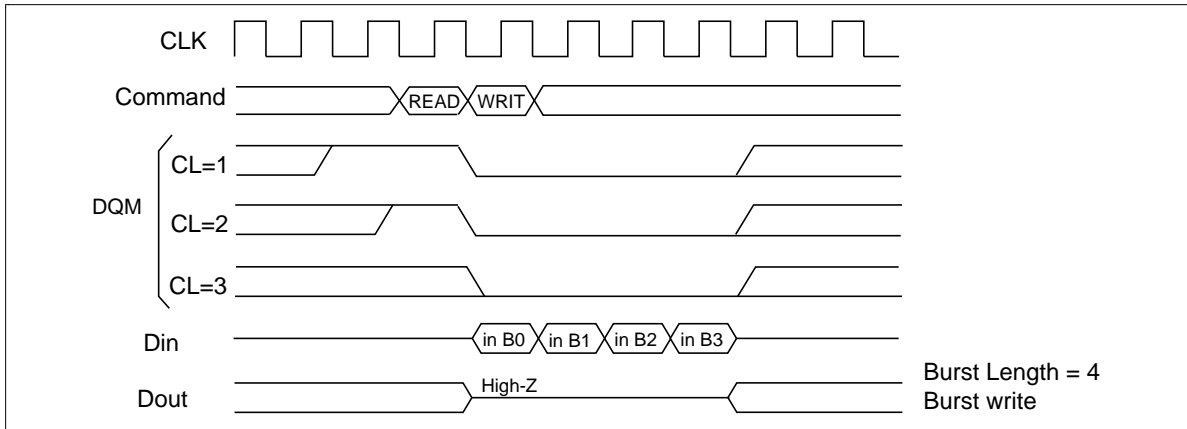


## HM5216805 Series, HM5216405 Series

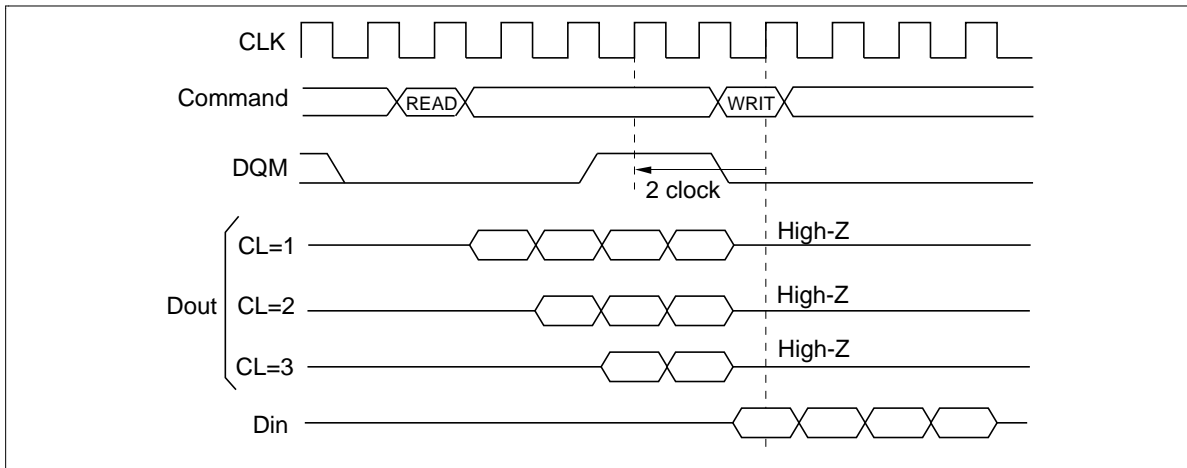
### Read command to Write command interval

**Same bank, same ROW address:** When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM must be set High so that the output buffer becomes High-Z before data input.

#### READ to WRITE Command Interval-1



#### READ to WRITE Command Interval-2



**Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

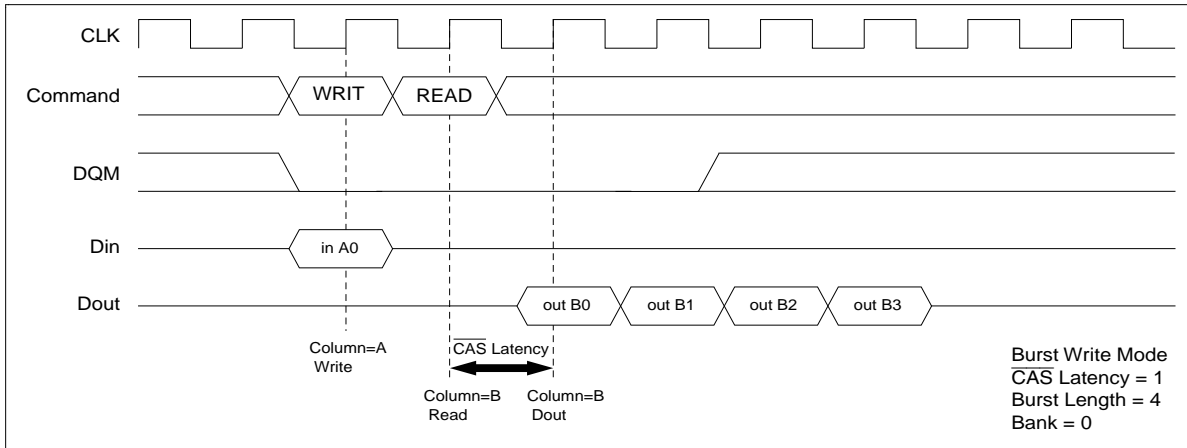
**Different bank:** When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

## HM5216805 Series, HM5216405 Series

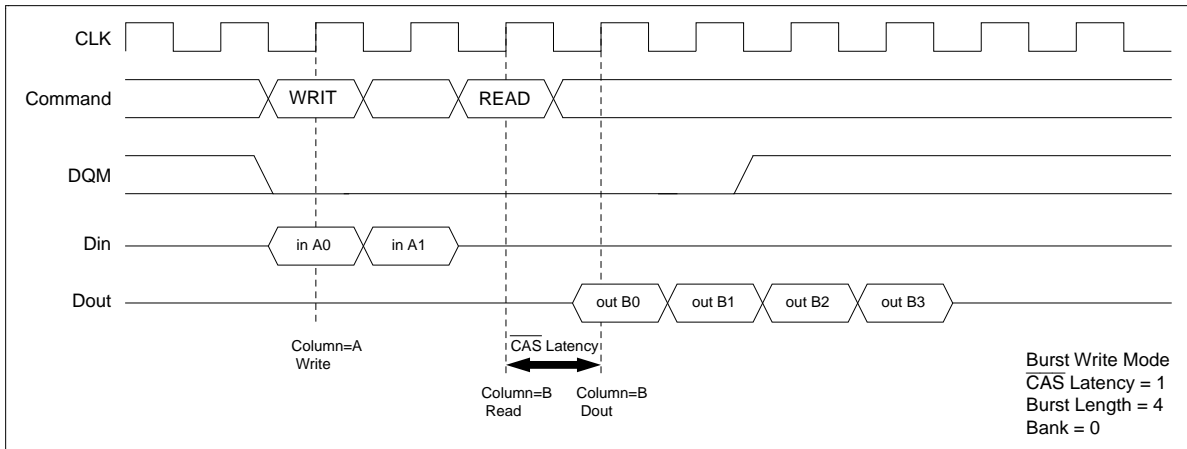
### Write command to Read command interval

**Same bank, same ROW address:** When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

#### WRITE to READ Command Interval-1



#### WRITE to READ Command Interval-2



**Same bank, different ROW address:** When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

**Different bank:** When the bank changes, the read command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

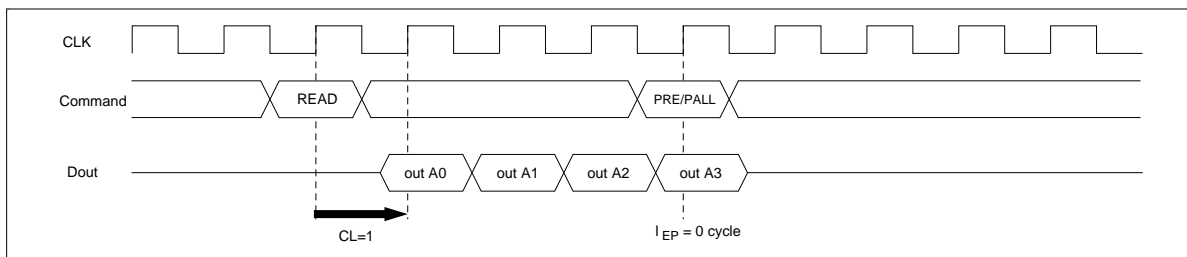


## HM5216805 Series, HM5216405 Series

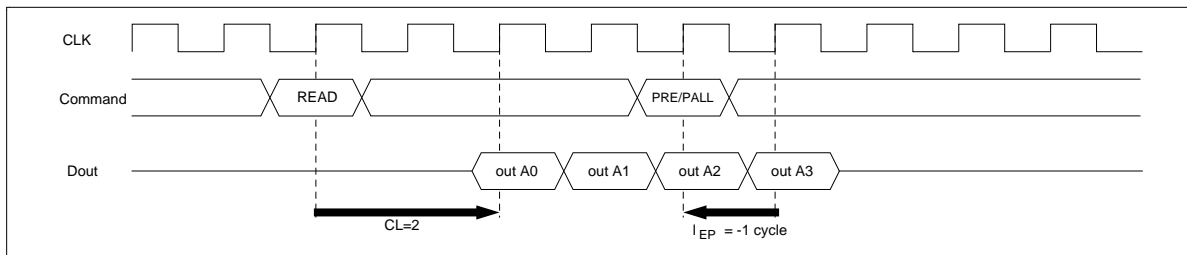
**Read command to Precharge command interval (same bank):** When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by  $t_{HZP}$ , there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by  $t_{EP}$  must be assured as an interval from the final data output to precharge command execution.

**READ to PRECHARGE Command Interval (same bank): To output all data**

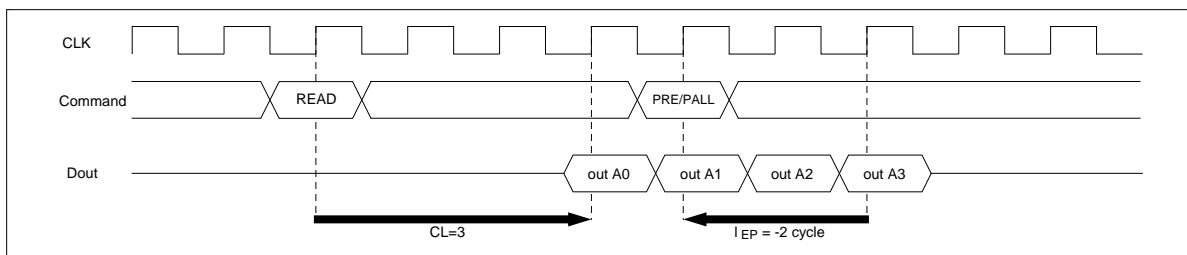
**$\overline{\text{CAS}}$  Latency = 1, Burst Length = 4**



**$\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



**$\overline{\text{CAS}}$  Latency = 3, Burst Length = 4**



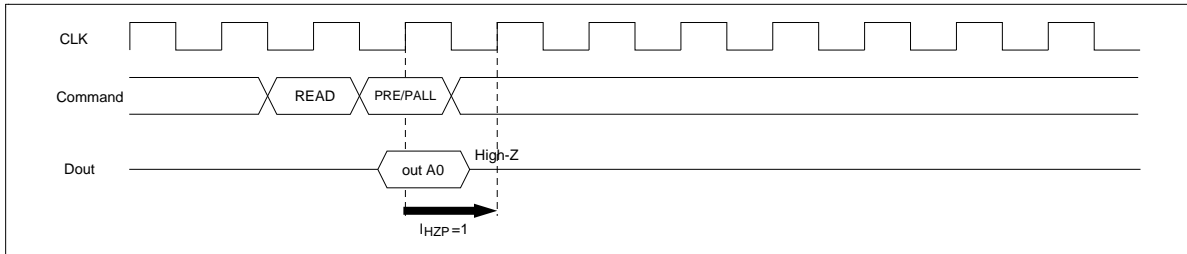
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## HM5216805 Series, HM5216405 Series

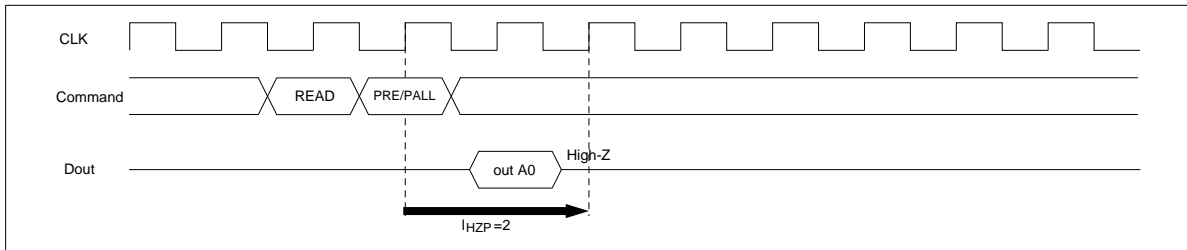
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**READ to PRECHARGE Command Interval (same bank): To stop output data**

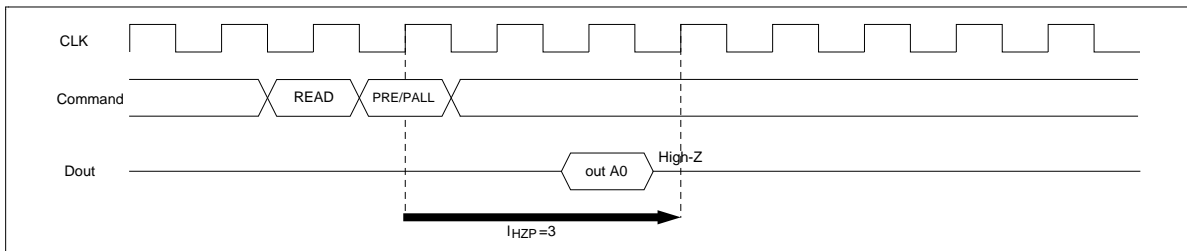
**$\overline{\text{CAS}}$  Latency = 1, Burst Length = 1, 2, 4, 8**



**$\overline{\text{CAS}}$  Latency = 2, Burst Length = 1, 2, 4, 8**



**$\overline{\text{CAS}}$  Latency = 3, Burst Length = 1, 2, 4, 8**

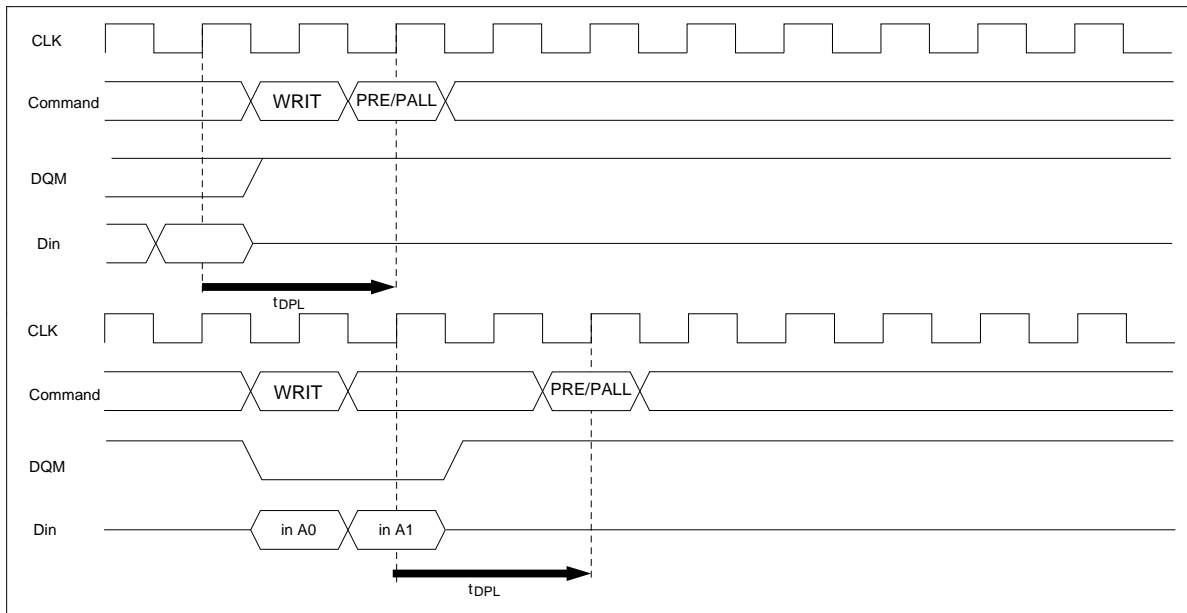


## HM5216805 Series, HM5216405 Series

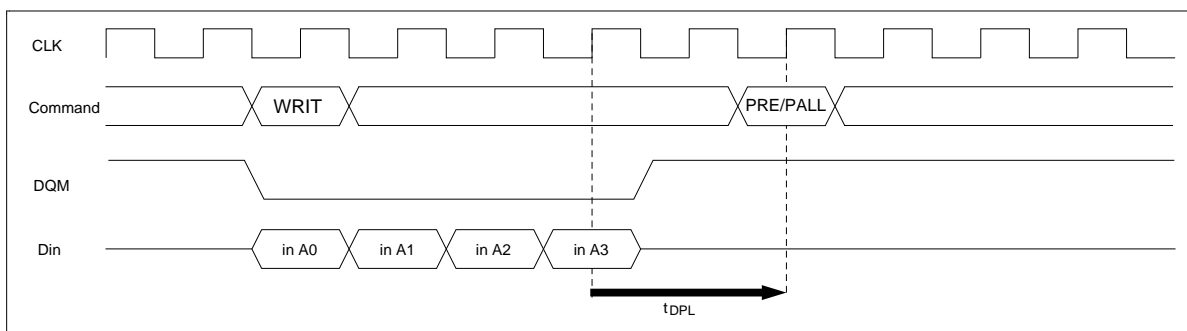
**Write command to Precharge command interval (same bank):** When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the cycle defined by  $t_{DPL}$ .

**WRITE to PRECHARGE Command Interval (same bank)**

**Burst Length = 4 (To stop write operation)**



**Burst Length = 4 (To write all data)**



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## HM5216805 Series, HM5216405 Series

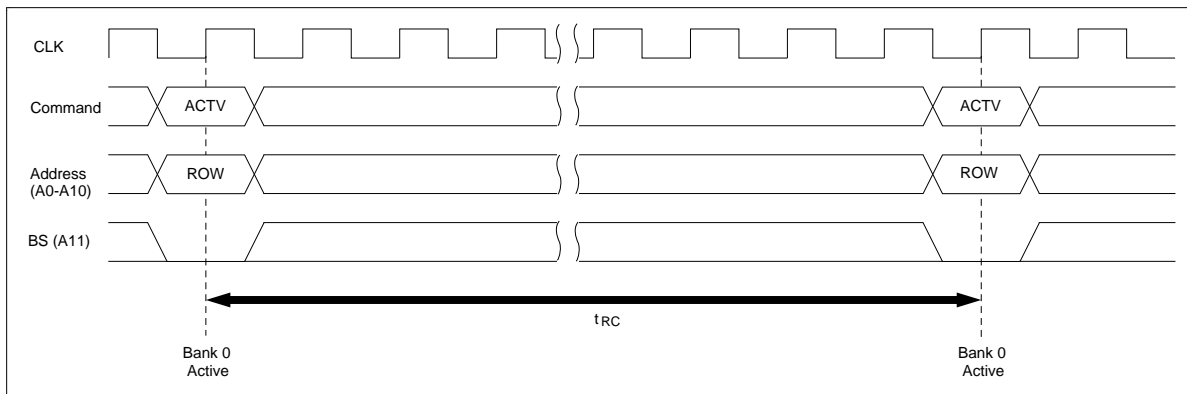
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### Bank active command interval

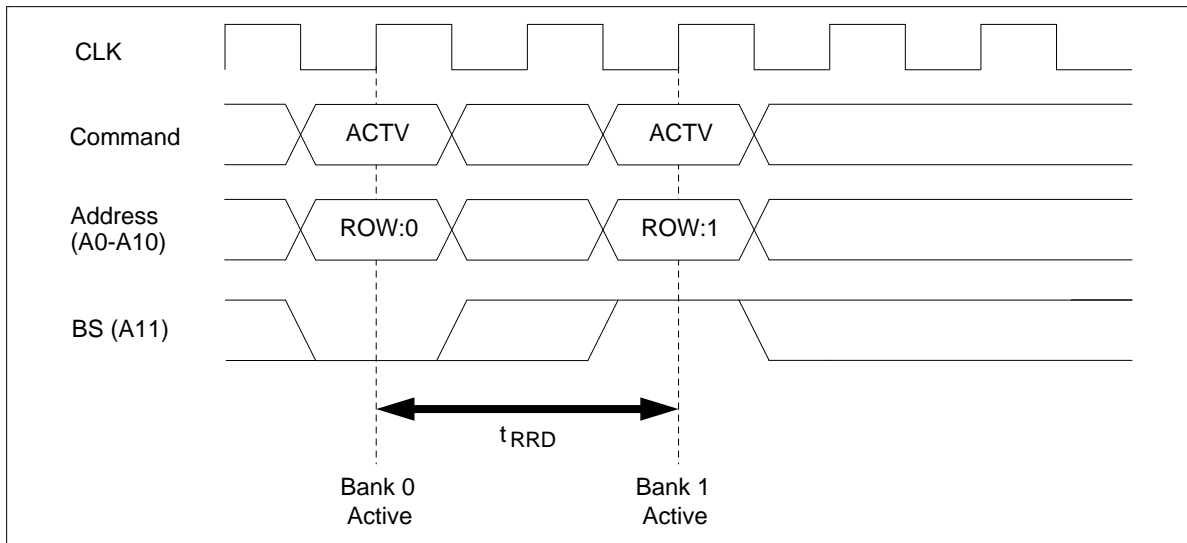
**Same bank:** The interval between the two bank-active commands must be no less than  $t_{RC}$ .

**In the case of different bank-active commands:** The interval between the two bank-active commands must be no less than  $t_{RRD}$ .

### Bank active to bank active for same bank



### Bank active to bank active for different bank

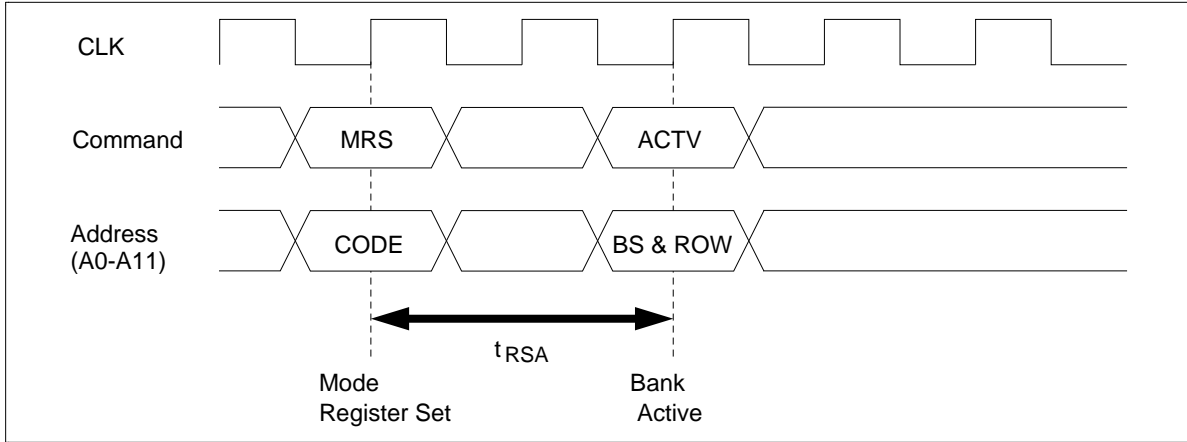


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## HM5216805 Series, HM5216405 Series

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**Mode register set to Bank-active command interval:** The interval between setting the mode register and executing a bank-active command must be no less than  $t_{RSA}$ .



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## HM5216805 Series, HM5216405 Series

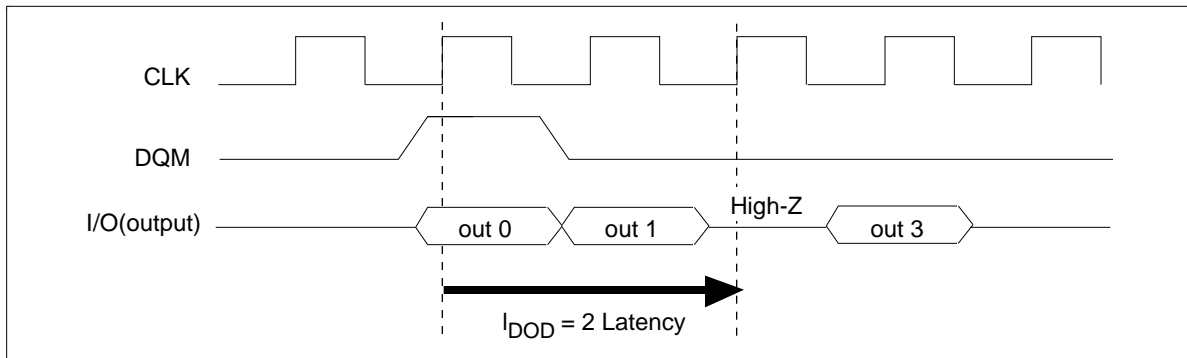
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### DQM Control

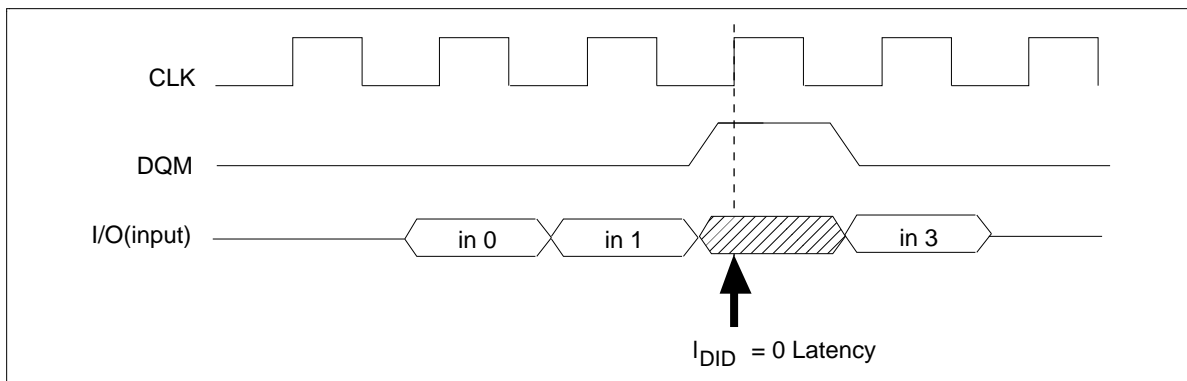
The DQM mask the lower and upper bytes of the I/O data, respectively. The timing of DQM is different during reading and writing.

**Reading:** When data is read, the output buffer can be controlled by DQM.

By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2.



**Writing:** Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0.



### Refresh

**Auto-refresh:** All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4,096 cycles/64 ms. (4,096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

**Self-refresh:** After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. If you use distributed auto-refresh mode with 15.6  $\mu$ s interval in normal read/write cycle, auto-refresh should be executed within 15.6  $\mu$ s immediately after exiting from and before entering into self refresh mode. If you use address refresh or burst auto-refresh mode in normal read/write cycle, 4096 cycles of distributed auto-refresh with 15.6  $\mu$ s interval should be executed within 64 ms immediately after exiting from and before entering into self refresh mode.

### Others

**Power-down mode:** The synchronous DRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

**Clock suspend mode:** By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

**Power-up sequence:** During power-up sequence, the DQM and the CKE must be set to High. When 200  $\mu$ s has past after power on, all banks must be precharged using the precharge command. After  $t_{RP}$  delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

## HM5216805 Series, HM5216405 Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +4.6	V	1
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +4.6	V	1
Short circuit output current	$I_{out}$	50	mA	
Power dissipation	$P_T$	1.0	W	
Operating temperature	$T_{opr}$	0 to +70	°C	
Storage temperature	$T_{stg}$	-55 to +125	°C	

Note: 1. Respect to  $V_{SS}$

### Recommended DC Operating Conditions ( $T_a = 0$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	$V_{CC}, V_{CCQ}$	3.0	3.6	V	1
	$V_{SS}, V_{SSQ}$	0	0	V	
Input high voltage	$V_{IH}$	2.0	4.6	V	1, 2
Input low voltage	$V_{IL}$	-0.3	0.8	V	1, 3

Notes: 1. All voltage referred to  $V_{SS}$   
 2.  $V_{IH}$  (max) = 5.5 V for pulse width  $\leq 5$  ns  
 3.  $V_{IL}$  (min) = -1.0 V for pulse width  $\leq 5$  ns



## HM5216805 Series, HM5216405 Series

**DC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}, V_{SSQ} = 0\text{ V}$ )

Parameter	Symbol	HM5216805/HM5216405				Unit	Test conditions	Notes
		-10H		-12				
		Min	Max	Min	Max			
Operating current	$I_{CC1}$	—	100	—	85	mA	$t_{RC} = \text{min}$ Burst length = 1	1, 2, 4
Standby current (Bank Disable)	$I_{CC2}$	—	3	—	3	mA	$\text{CKE} = V_{IL}$ , $t_{CK} = \text{min}$	5
		—	2	—	2	mA	$\text{CKE} = V_{IL}$ $\text{CLK} = V_{IL}$ or $V_{IH}$ Fixed	6
		—	40	—	35	mA	$\text{CKE} = V_{IH}$ , NOP command $t_{CK} = \text{min}$	3
Active standby current (Bank active)	$I_{CC3}$	—	7	—	7	mA	$\text{CKE} = V_{IL}$ , $t_{CK} = \text{min}$ , I/O = High-Z	1, 2
		—	45	—	40	mA	$\text{CKE} = V_{IH}$ , NOP command $t_{CK} = \text{min}$ , I/O = High-Z	1, 2, 3
Burst operating current (CAS latency = 1)	$I_{CC4}$	—	65	—	55	mA	$t_{CK} = \text{min}$ BL = 4	1, 2, 4
		(CAS latency = 2)	—	100	—	85	mA	
		(CAS latency = 3)	—	150	—	125	mA	
Refresh current	$I_{CC5}$	—	85	—	70	mA	$t_{RC} = \text{min}$	
Self refresh current	$I_{CC6}$	—	2	—	2	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2\text{ V}$	7
Self refresh current (L-version)	$I_{CC6}$	—	250	—	—	$\mu\text{A}$	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2\text{ V}$	7
Input leakage current	$I_{LI}$	-10	10	-10	10	$\mu\text{A}$	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	$I_{LO}$	-10	10	-10	10	$\mu\text{A}$	$0 \leq V_{out} \leq V_{CC}$ I/O = disable	
Output high voltage	$V_{OH}$	2.4	—	2.4	—	V	$I_{OH} = -2\text{ mA}$	
Output low voltage	$V_{OL}$	—	0.4	—	0.4	V	$I_{OL} = 2\text{ mA}$	

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## HM5216805 Series, HM5216405 Series

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- Notes:
1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  (max) is specified at the output open condition.
  2. One bank operation.
  3. Input signal transition is once per two CLK cycles.
  4. Input signal transition is once per one CLK cycle.
  5. After power down mode set, CLK operating current.
  6. After power down mode set, no CLK operating current.
  7. After self refresh mode set, self refresh current.

### Capacitance ( $T_a = 25^\circ\text{C}$ , $V_{CC}$ , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	2	5	pF	1, 3
Input capacitance (Signals)	$C_{i2}$	2	5	pF	1, 3
Output capacitance (I/O)	$C_o$	4	7	pF	1, 2, 3

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
  2.  $DQM = V_{IH}$  to disable Dout.
  3. This parameter is sampled and not 100% tested.

## HM5216805 Series, HM5216405 Series

**AC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}, V_{SSQ} = 0\text{ V}$ )

Parameter	Symbol	HM5216805/HM5216405				Unit	Notes
		-10H		-12			
		Min	Max	Min	Max		
System clock cycle time ( $\overline{\text{CAS}}$ latency = 1)	$t_{\text{CK}}$	30	—	36	—	ns	1
( $\overline{\text{CAS}}$ latency = 2)	$t_{\text{CK}}$	15	—	18	—		
( $\overline{\text{CAS}}$ latency = 3)	$t_{\text{CK}}$	10	—	12	—		
CLK high pulse width	$t_{\text{CKH}}$	3	—	4	—	ns	1
CLK low pulse width	$t_{\text{CKL}}$	3	—	4	—	ns	1
Access time from CLK ( $\overline{\text{CAS}}$ latency = 1)	$t_{\text{AC}}$	—	27	—	32	ns	1, 2
( $\overline{\text{CAS}}$ latency = 2)	$t_{\text{AC}}$	—	9.0	—	12		
( $\overline{\text{CAS}}$ latency = 3)	$t_{\text{AC}}$	—	7.5	—	9		
Data-out hold time	$t_{\text{OH}}$	3	—	3	—	ns	1, 2
CLK to Data-out low impedance	$t_{\text{LZ}}$	0	—	0	—	ns	1, 2, 3
CLK to Data-out high impedance ( $\overline{\text{CAS}}$ latency = 1)	$t_{\text{HZ}}$	—	13	—	15	ns	
( $\overline{\text{CAS}}$ latency = 2, 3)	$t_{\text{HZ}}$	—	7	—	9	ns	1, 4
Data-in setup time	$t_{\text{DS}}$	2	—	3	—	ns	1
Data in hold time	$t_{\text{DH}}$	1	—	1	—	ns	1
Address setup time	$t_{\text{AS}}$	2	—	3	—	ns	1
Address hold time	$t_{\text{AH}}$	1	—	1	—	ns	1
CKE setup time	$t_{\text{CES}}$	2	—	3	—	ns	1, 5
CKE setup time for power down exit	$t_{\text{CESP}}$	2	—	3	—	ns	1
CKE hold time	$t_{\text{CEH}}$	1	—	1	—	ns	1
Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM) setup time	$t_{\text{CS}}$	2	—	3	—	ns	1
Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM) hold time	$t_{\text{CH}}$	1	—	1	—	ns	1

## HM5216805 Series, HM5216405 Series

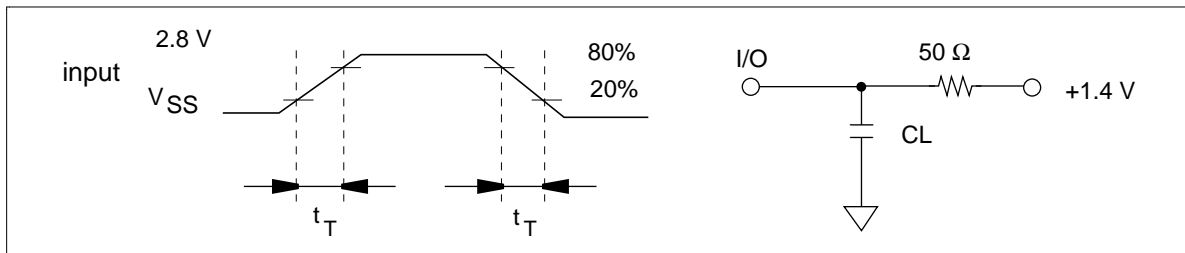
AC Characteristics ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}, V_{SSQ} = 0\text{ V}$ ) (cont)

Parameter	Symbol	HM5216805/HM5216405				Unit	Notes
		-10H		-12			
		Min	Max	Min	Max		
Ref/Active to Ref/Active command period	$t_{RC}$	90	—	100	—	ns	1
Active to Precharge command period	$t_{RAS}$	60	120000	70	120000	ns	1
Active to precharge on full page mode	$t_{RASC}$	—	120000	—	120000	ns	1
Active command to column command (same bank)	$t_{RCD}$	30	—	30	—	ns	1
Precharge to active command period	$t_{RP}$	30	—	30	—	ns	1
Write recovery or data-in to precharge lead time	$t_{DPL}$	15	—	15	—	ns	1
Active (a) to Active (b) command period	$t_{RRD}$	20	—	20	—	ns	1
Transition time (rise to fall)	$t_T$	1	5	1	5	ns	
Refresh period	$t_{REF}$	—	64	—	64	ms	

- Notes: 1. AC measurement assumes  $t_T = 1\text{ ns}$ . Reference level for timing of input signals is 1.40 V.  
 2. Access time is measured at 1.40 V. Load condition is  $C_L = 50\text{ pF}$  with current source.  
 3.  $t_{LZ}$  (max) defines the time at which the outputs achieves the low impedance state.  
 4.  $t_{HZ}$  (max) defines the time at which the outputs achieves the high impedance state.  
 5.  $t_{CES}$  defines CKE setup time to CKE rising edge except power down exit command.

### Test Conditions

- Input and output timing reference level: 1.4 V
- Input waveform and output load: See following figures



## HM5216805 Series, HM5216405 Series

### Relationship Between Frequency and Minimum Latency

Parameter	Symbol	HM5216805/HM5216405						Notes
		-10H			-12			
		100 10	66 15	33 30	83 12	55 18	28 36	
Frequency (MHz)								
$t_{ck}$ (ns)								
Active command to column command (same bank)	$t_{RCD}$	3	2	1	3	2	1	1
Active command to active command (same bank)	$t_{RC}$	9	6	3	9	6	3	= [ $t_{RAS}$ + $t_{RP}$ ] 1
Active command to precharge command (same bank)	$t_{RAS}$	6	4	2	6	4	2	1
Precharge command to active command (same bank)	$t_{RP}$	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)	$t_{DPL}$	2	1	1	2	1	1	1
Active command to active command (different bank)	$t_{RRD}$	2	2	1	2	2	1	1
Self refresh exit time	$I_{SREX}$	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	$I_{APW}$	5	3	2	5	3	2	= [ $t_{DPL}$ + $t_{RP}$ ]
Self refresh exit to command input	$I_{SEC}$	9	6	3	9	6	3	= [ $t_{RC}$ ]
Precharge command to high impedance ( $\overline{CAS}$ latency = 3)	$I_{HZP}$	3	3	3	3	3	3	
( $\overline{CAS}$ latency = 2)	$I_{HZP}$	—	2	2	—	2	2	
( $\overline{CAS}$ latency = 1)	$I_{HZP}$	—	—	1	—	—	1	
Last data out to active command (auto precharge) (same bank)	$I_{APR}$	1	1	1	1	1	1	
Last data out to precharge (early precharge) ( $\overline{CAS}$ latency = 3)	$I_{EP}$	-2	-2	-2	-2	-2	-2	
( $\overline{CAS}$ latency = 2)	$I_{EP}$	—	-1	-1	—	-1	-1	
( $\overline{CAS}$ latency = 1)	$I_{EP}$	—	—	0	—	—	0	
Column command to column command	$I_{CCD}$	1	1	1	1	1	1	
Write command to data in latency	$I_{WCD}$	0	0	0	0	0	0	
DQM to data in	$I_{DID}$	0	0	0	0	0	0	
DQM to data out	$I_{DOD}$	2	2	2	2	2	2	
CKE to CLK disable	$I_{CLE}$	1	1	1	1	1	1	

## HM5216805 Series, HM5216405 Series

### Relationship Between Frequency and Minimum Latency (cont)

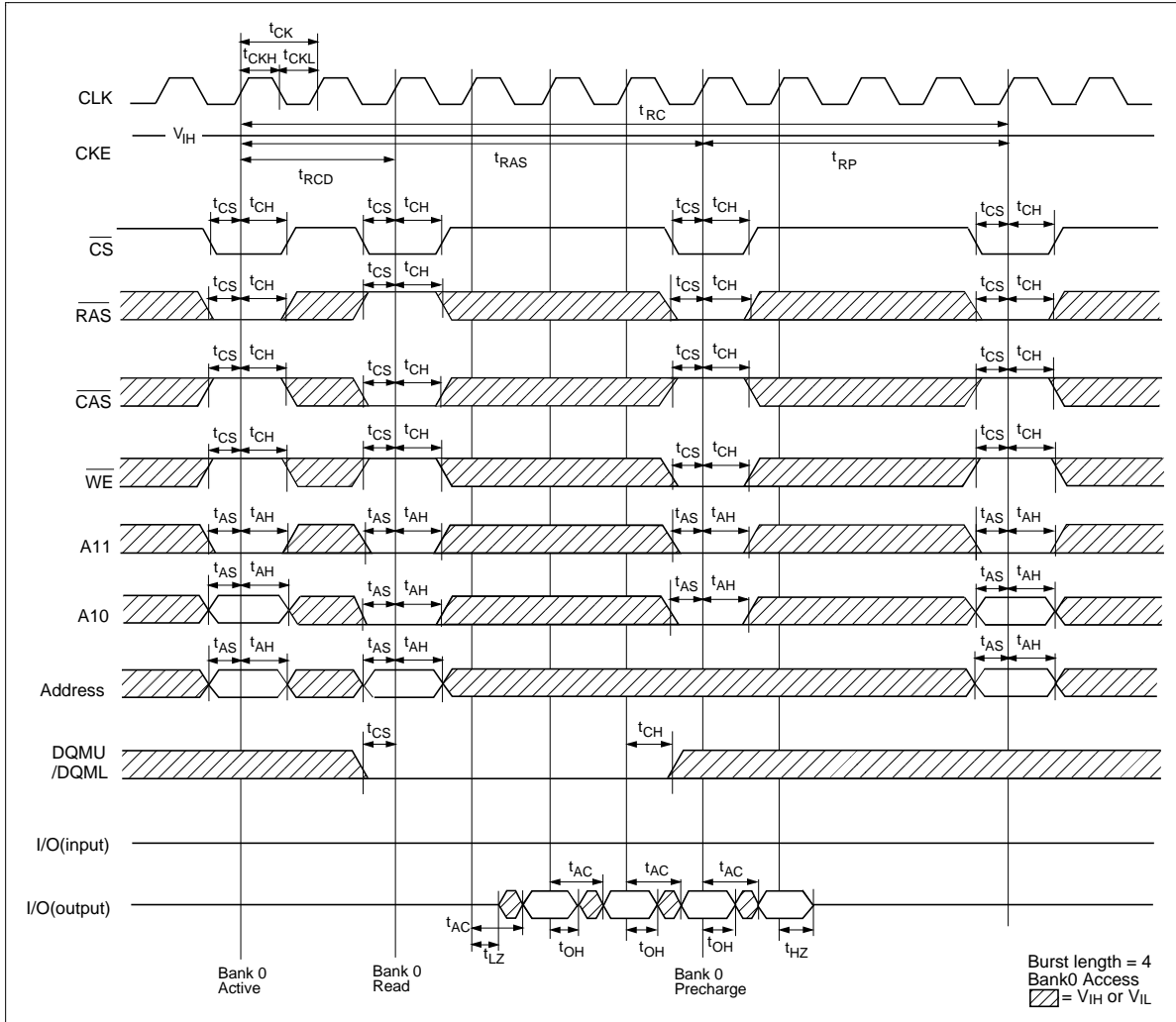
Parameter	Symbol	HM5216805/HM5216405						Notes
		-10H			-12			
		100 10	66 15	33 30	83 12	55 18	28 36	
Register set to active command	$t_{RSA}$	1	1	1	1	1	1	
CS to command disable	$I_{CDD}$	0	0	0	0	0	0	
Power down exit to command input	$I_{PEC}$	1	1	1	1	1	1	
Burst stop to output valid data hold ( $\overline{CAS}$ latency = 3)	$I_{BSR}$	2	2	2	2	2	2	
( $\overline{CAS}$ latency = 2)	$I_{BSR}$	—	1	1	—	1	1	
( $\overline{CAS}$ latency = 1)	$I_{BSR}$	—	—	0	—	—	0	
Burst stop to output high impedance ( $\overline{CAS}$ latency = 3)	$I_{BSH}$	3	3	3	3	3	3	
( $\overline{CAS}$ latency = 2)	$I_{BSH}$	—	2	2	—	2	2	
( $\overline{CAS}$ latency = 1)	$I_{BSH}$	—	—	1	—	—	1	
Burst stop to write data ignore	$I_{BSW}$	0	0	0	0	0	0	

Notes: 1.  $t_{RCD}$  to  $t_{RRD}$  are recommended value.

2. When self refresh exit is executed, CKE should be kept "H" longer than  $I_{SREX}$  from exit cycle.

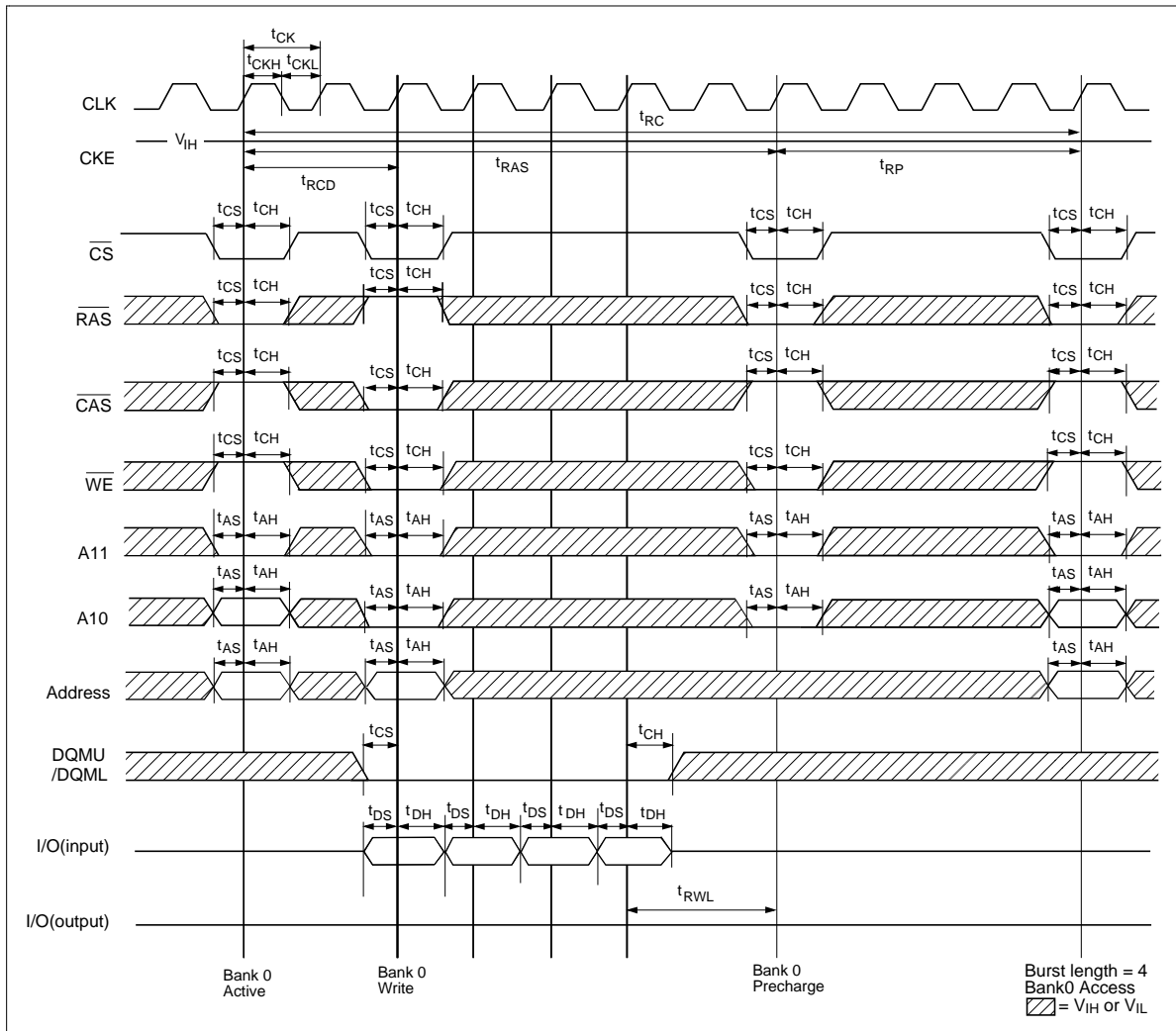
Timing Waveforms

Read Cycle



# HM5216805 Series, HM5216405 Series

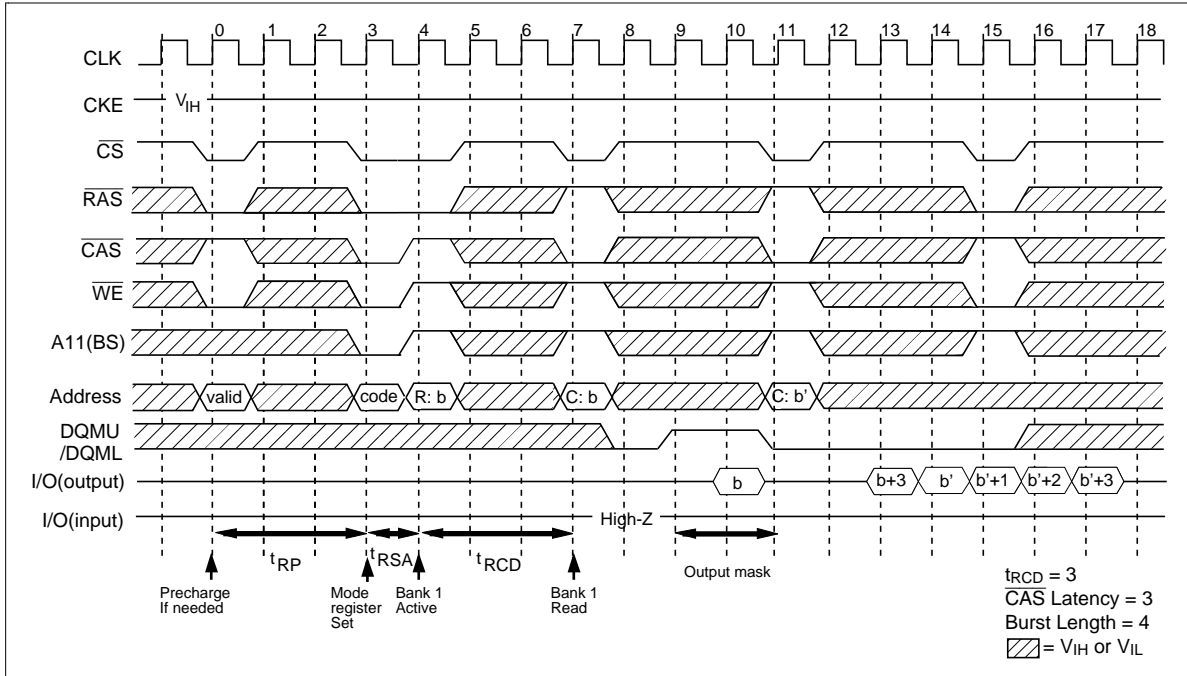
## Write Cycle





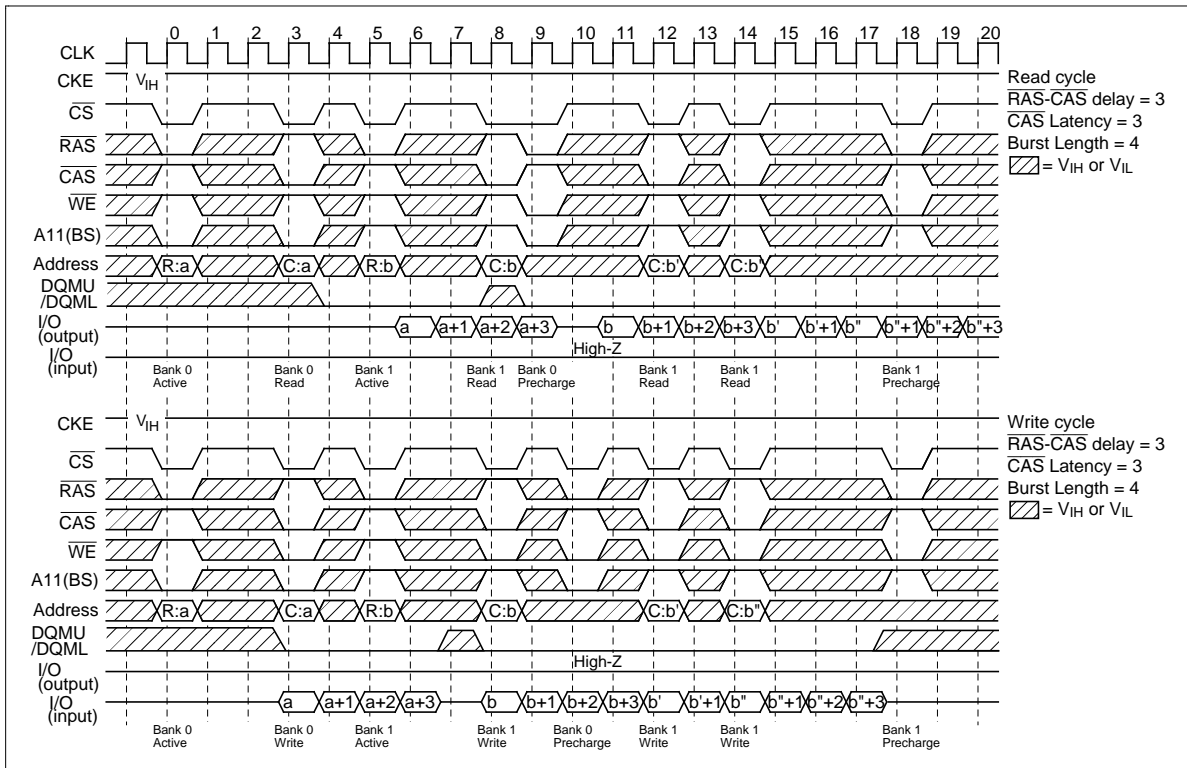
# HM5216805 Series, HM5216405 Series

## Mode Register Set Cycle



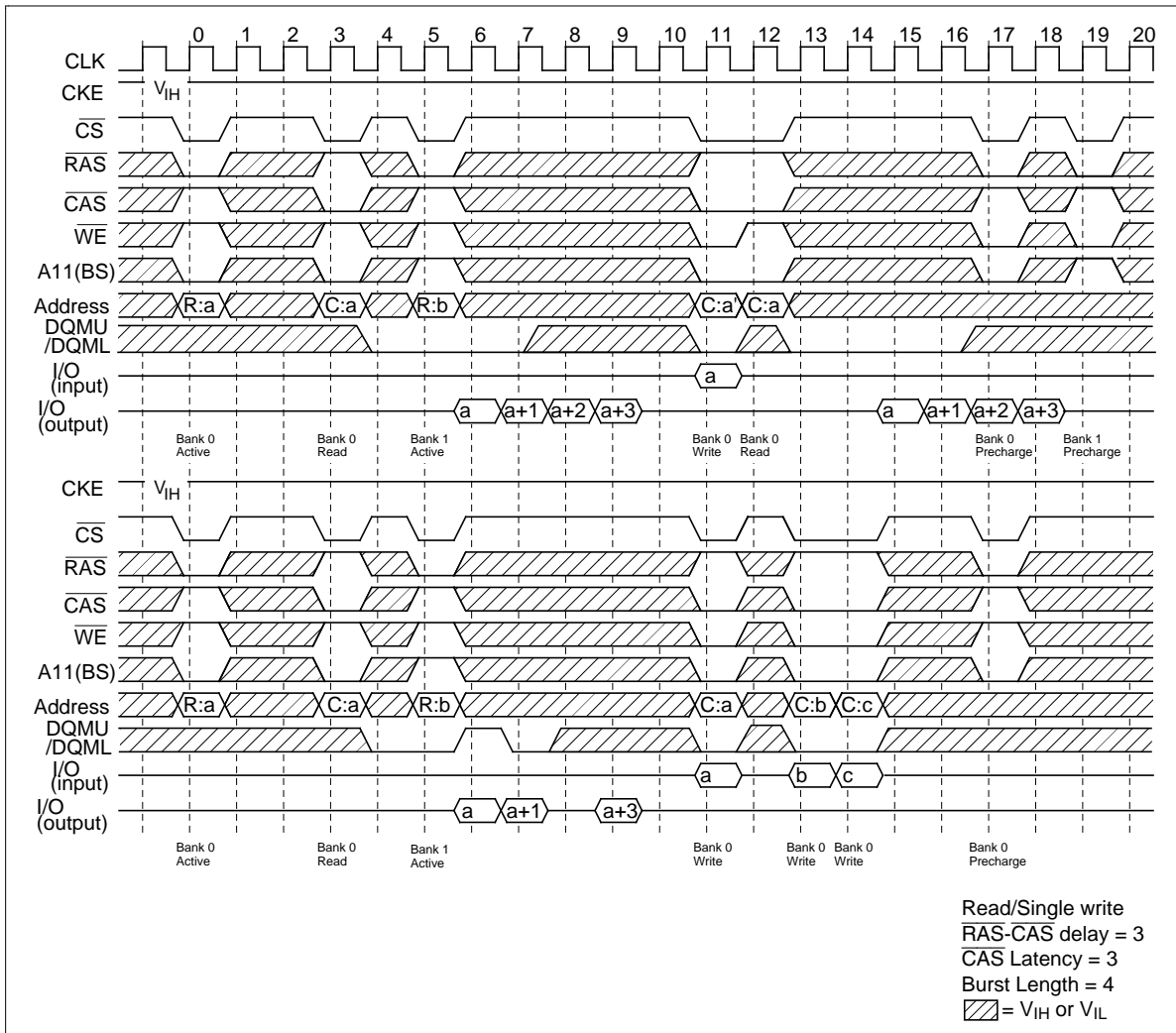
# HM5216805 Series, HM5216405 Series

## Read Cycle/Write Cycle



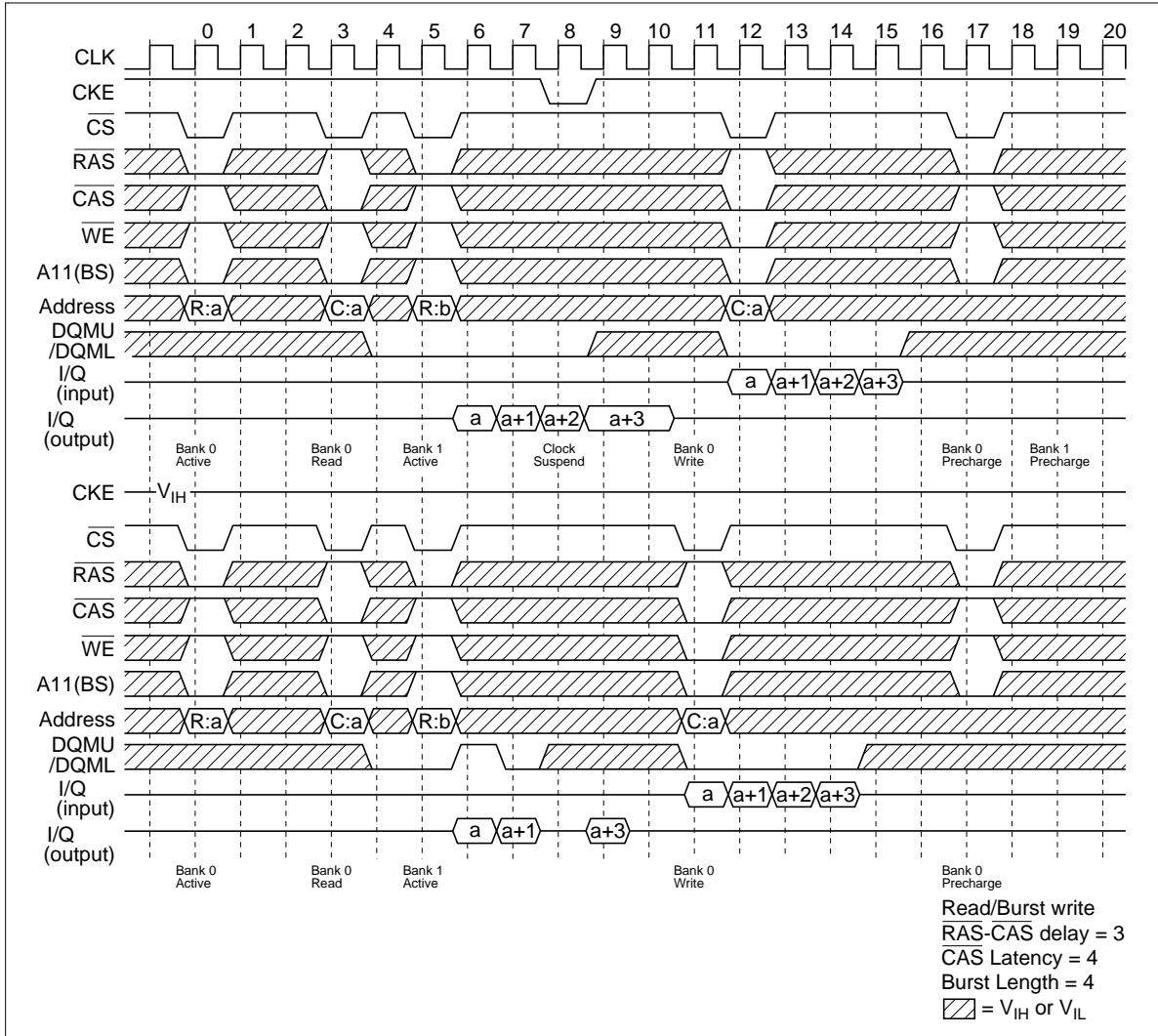
# HM5216805 Series, HM5216405 Series

## Read/Single Write Cycle



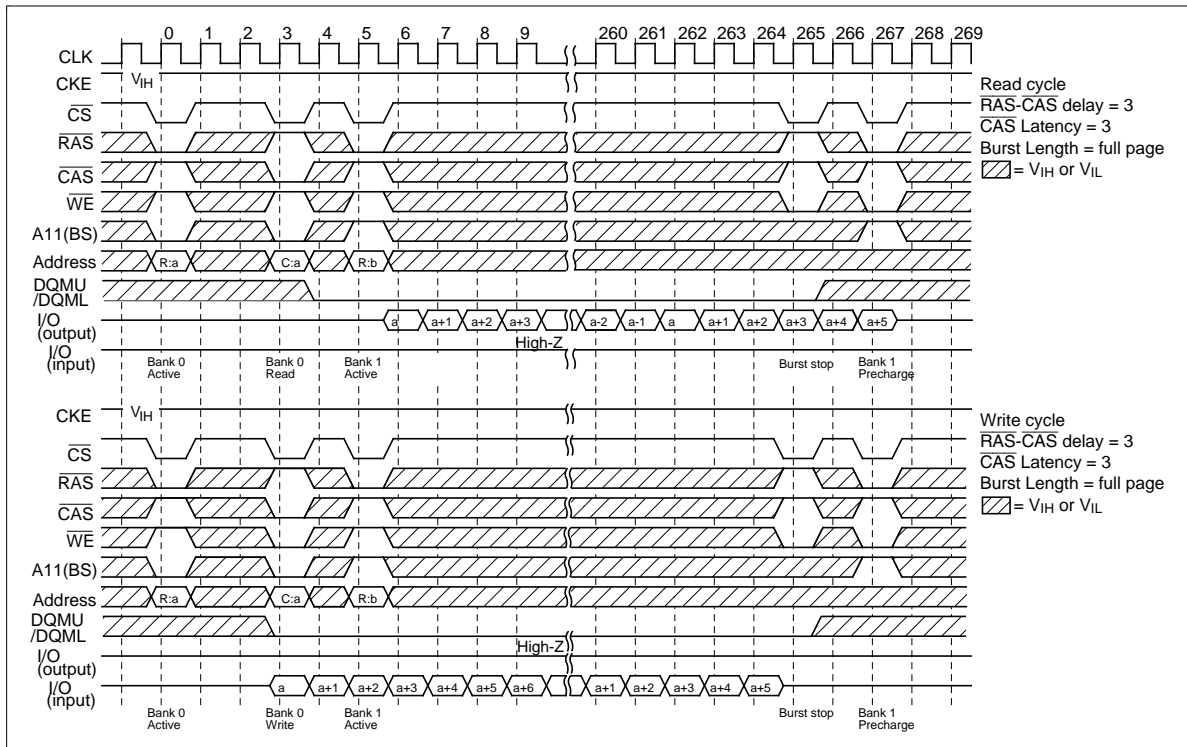
# HM5216805 Series, HM5216405 Series

## Read/Burst Write Cycle



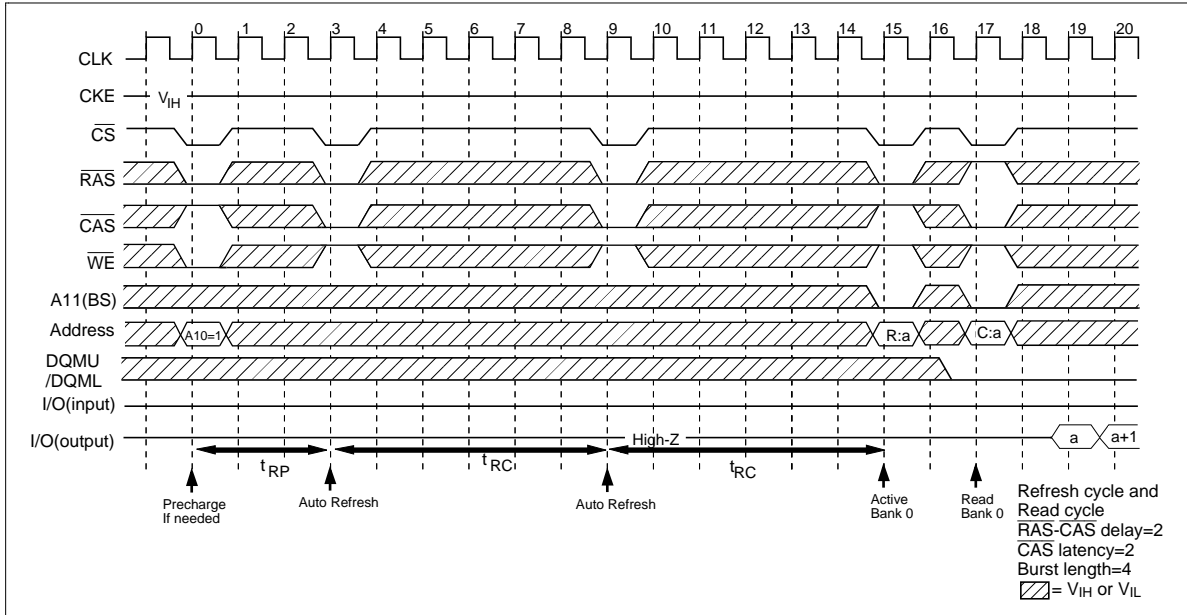
# HM5216805 Series, HM5216405 Series

## Full Page Read/Write Cycle

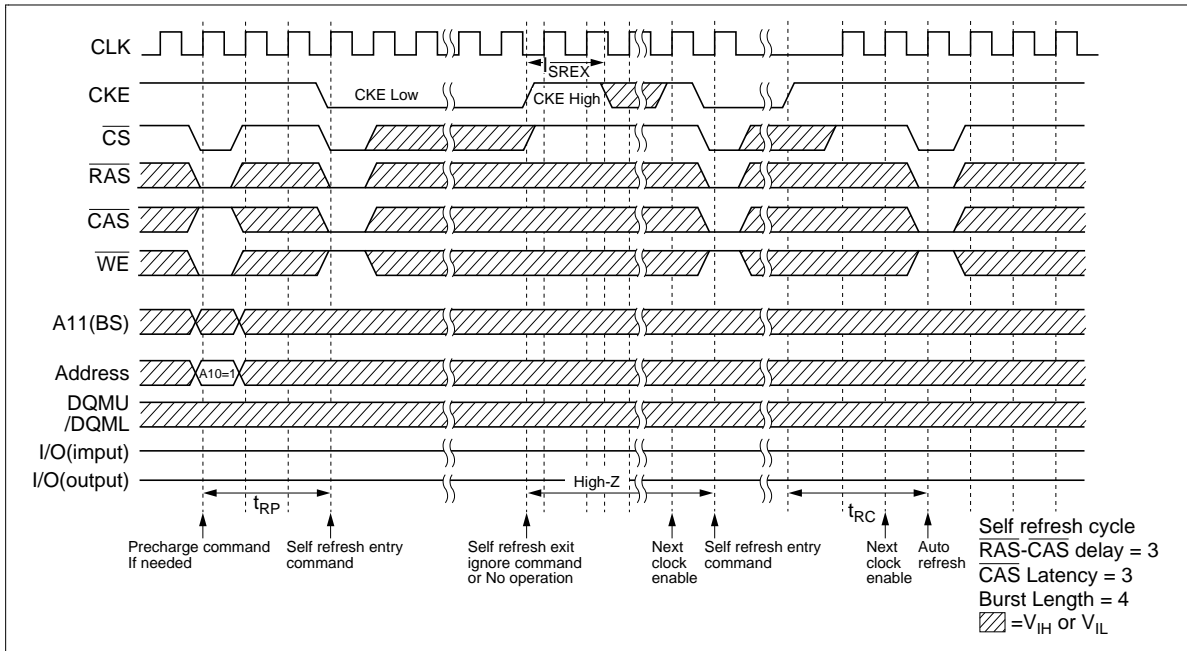


# HM5216805 Series, HM5216405 Series

## Auto Refresh Cycle

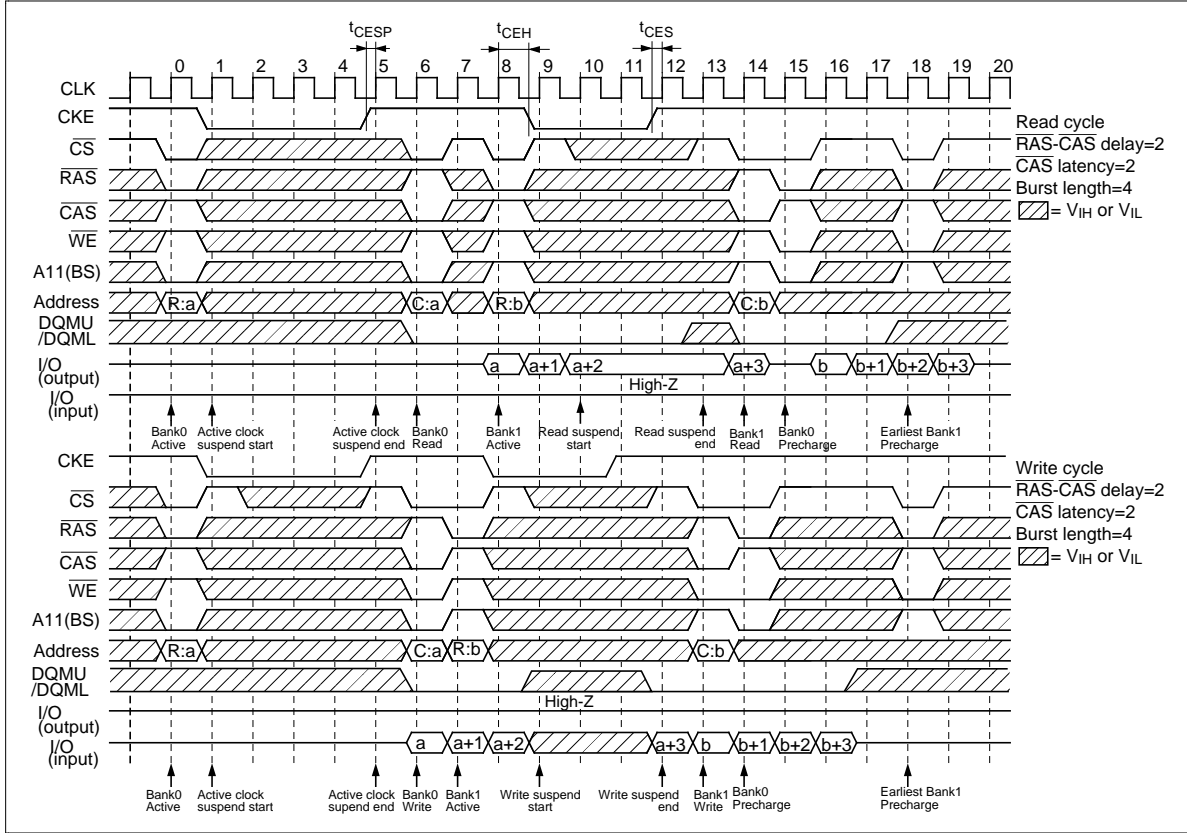


## Self Refresh Cycle



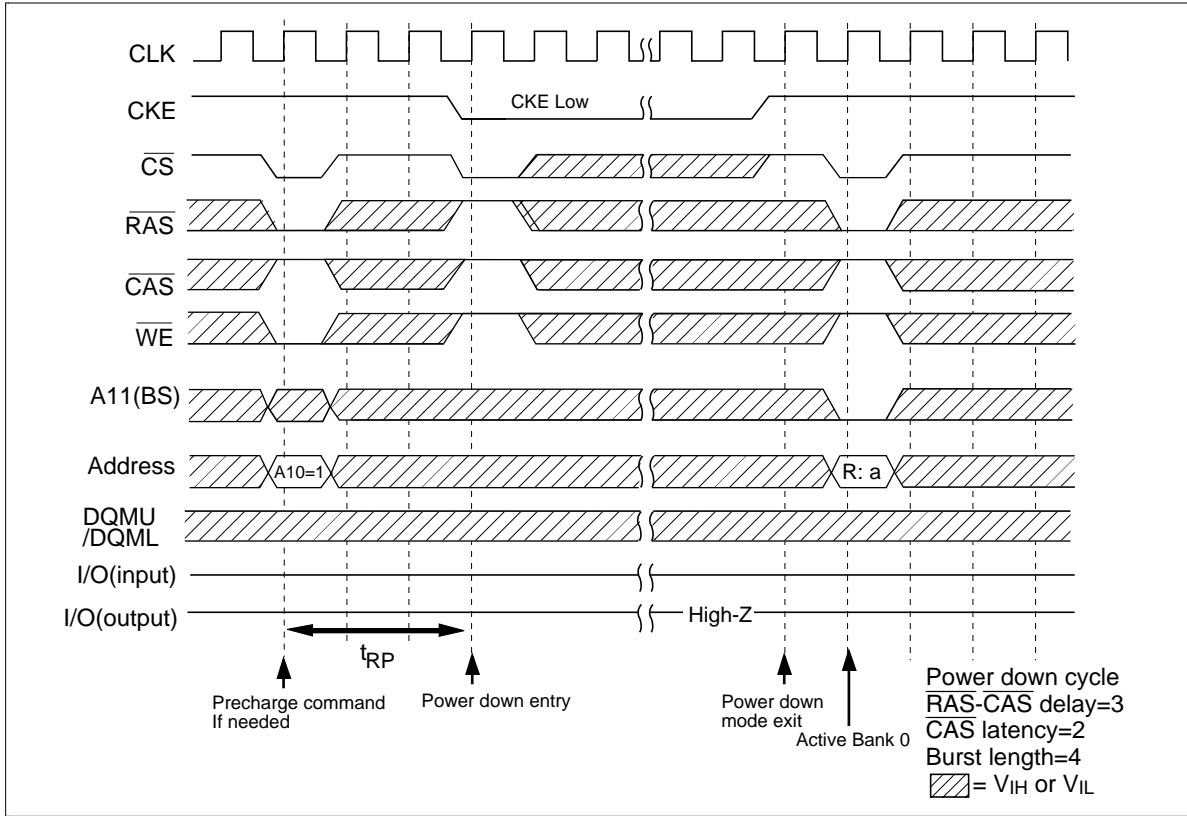
# HM5216805 Series, HM5216405 Series

## Clock Suspend Mode

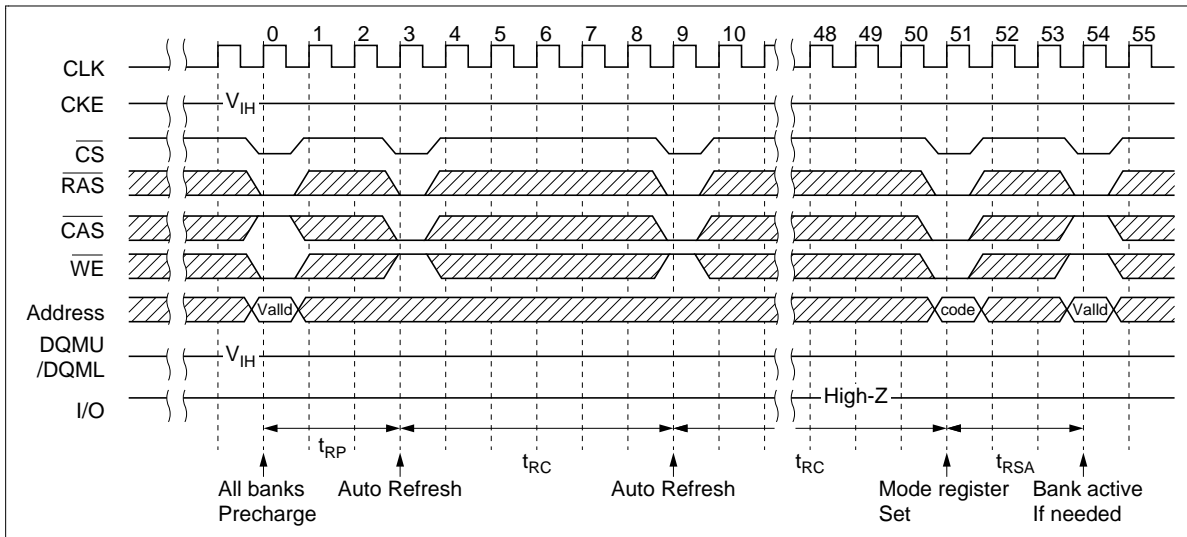


# HM5216805 Series, HM5216405 Series

## Power Down Mode



## Power Up Sequence

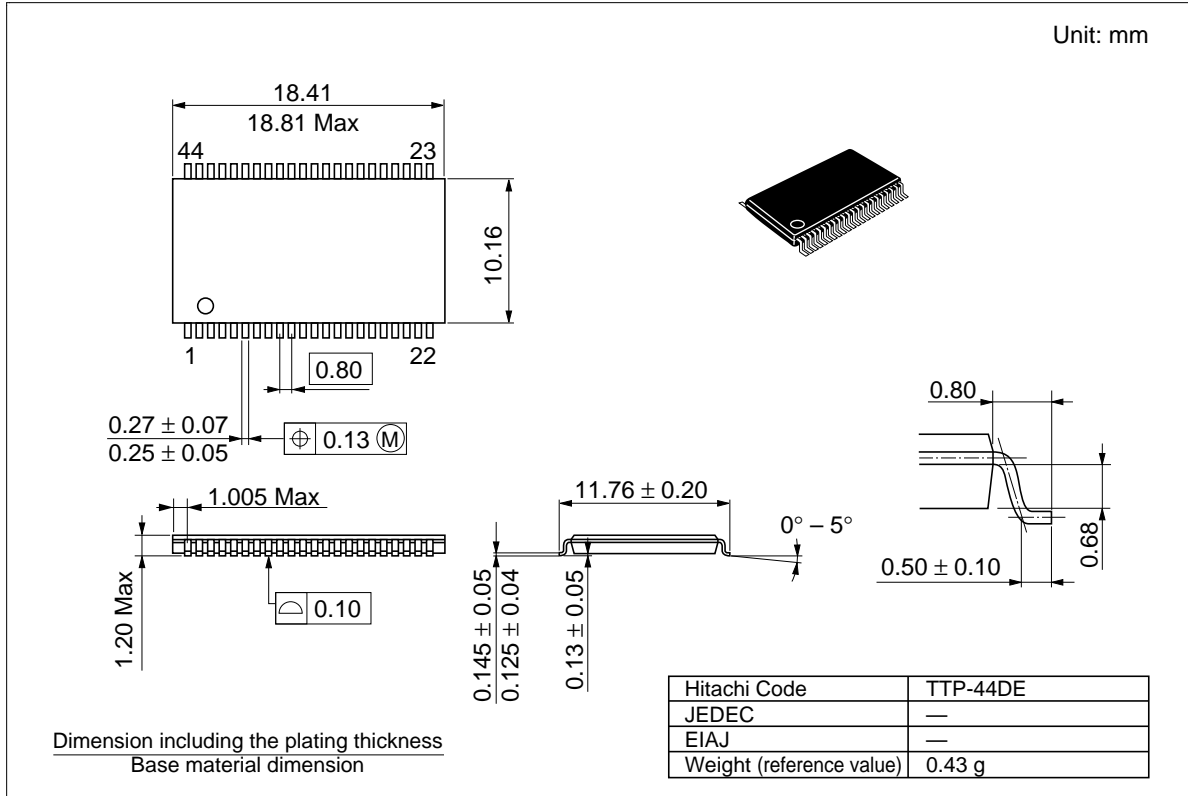




# HM5216805 Series, HM5216405 Series

## Package Dimensions

HM5216805TT/HM5216405TT Series (TTP-44DE)



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## HM5216805 Series, HM5216405 Series

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## HM5216805 Series, HM5216405 Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Nov. 4, 1994	Initial issue	S. Ishikawa	T. Kizaki
0.1	Feb. 22, 1995	Addition of Full-page Burst Stop Command Truth Table Addition of BST: H/X/L/H/H/L/X/X/X Addition of description for burst stop in full page Function Truth Table Addition of BST: L/H/H/L/X Change of Simplified State Diagram and Mode Register Configuration DC Characteristics I <sub>CC2</sub> max: 40/35/30 mA to 30/25/20 mA I <sub>CC3</sub> max: 40/35/30 mA to 35/30/25 mA AC Characteristics t <sub>RWL</sub> min: 20/24/30 ns to 15/18/22.5 ns Relationship Between Frequency and Minimum Latency t <sub>RWL</sub> : 2/2/1/2/2/1/2/2/1 to 2/1/1/2/1/1/2/1/1 Addition of I <sub>BSR</sub> (CL = 3): 2/2/2/2/2/2/2/2 Addition of I <sub>BSR</sub> (CL = 2): —/1/1/—/1/1/—/1/1 Addition of I <sub>BSR</sub> (CL = 1): —/—/0/—/—/0/—/—/0 Addition of I <sub>BSS</sub> (CL = 3): 3/3/3/3/3/3/3/3 Addition of I <sub>BSS</sub> (CL = 2): —/2/2/—/2/2/—/2/2 Addition of I <sub>BSS</sub> (CL = 1): —/—/1/—/—/1/—/—/1 Addition of I <sub>BSW</sub> : 0/0/0/0/0/0/0/0 Timing Waveforms: Addition of Full Page Read/Write cycle	S. Ishikawa	T. Kizaki
0.2	Aug. 4, 1995	Unification of HM5216805 Series and HM5216405 Series Operation of HM5216805 Series, HM5216405 Series Addition of figure for READ to WRITE Command Interval (2) Absolute Maximum Ratings: Addition of note1 AC Characteristics t <sub>AC</sub> (CL = 1) max: 28/32/36 ns to 27/32/36 ns t <sub>AC</sub> (CL = 2) max: 13/15/17 ns to 12/15/17 ns t <sub>CESP</sub> min: 5/5/5 ns to 2/3/3 ns Relationship Between Frequency and Minimum Latency Addition of I <sub>SREX</sub> : 2/2/2/2/2/2/2/2 I <sub>APW</sub> : 5/4/2/5/4/2/5/4/2 to 5/3/2/5/3/2/5/3/2 Addition of notes3 Timing Waveforms Change of Self Refresh Cycle	S. Ishikawa	T. Kizaki
1.0	Oct. 20, 1995	Correct errors DC Characteristics I <sub>CC2</sub> max: 30/25/20 mA to 40/35/30 mA I <sub>CC3</sub> max: 35/30/25 mA to 45/40/35 mA AC Characteristics t <sub>HZ</sub> min: 2/3/3 ns to 2/2/2 ns Relationship Between Frequency and Minimum Latency Change of notes 2	K. Nishimoto	T. Kizaki

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## HM5216805 Series, HM5216405 Series

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Rev.	Date	Contents of Modification	Drawn by	Approved by
2.0	Dec. 10, 1996	Addition of HM5216805/5216405-10H Series Capacitance $C_{11}, C_{12}$ : — typ to 2 min $C_{13}$ : — typ to 2 min AC Characteristics Addition of $t_{AC}$ (CL = 2) (HM5216805/5216405-10H) max: 9.0/12/17 ns $t_{AC}$ (CL = 2) max: 12/15/17 ns to 9.5/12/17 ns $t_{AC}$ (CL = 3) max: 8/10/12 ns to 7.5/9/12 ns $t_{HZ}$ min: 2/2/2 ns to —/—/— ns Change of symbol: $t_{RWL}$ to $t_{DPL}$	T. Takemura	S. Ishikawa
3.0	Jan. 20, 1997	Addition of HM5216805/5216405L-10H/10 Series Change of description for Self-refresh DC Characteristics Addition of $I_{CC6}$ (L-version) max: 250/—/— $\mu$ A	T. Takemura	S. Ishikawa
4.0	Jun. 12, 1997	Deletion of HM5216805/5216405-10/15 Series	T. Takemura	S. Ishikawa
5.0	Nov. 1997	Change of Subtitle		

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