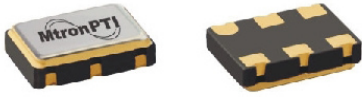


UVCJ Series

5x7 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillators

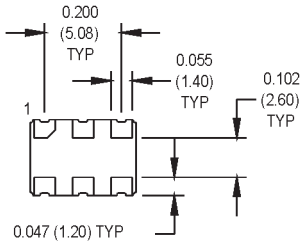
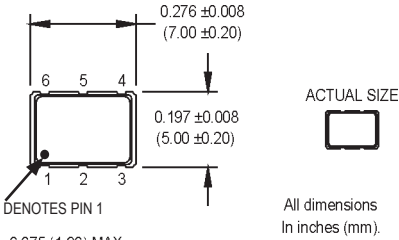


- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for 10 and 40 Gigabit Ethernet and Optical Carrier applications

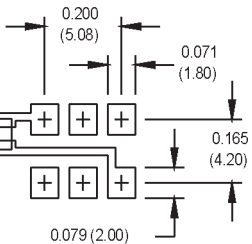


Ordering Information		00.0000 MHz
Product Series	UVCJ	1 8 B L N
Temperature Range	1: 0°C to +70°C 2: -40°C to +85°C 6: -20°C to +70°C 7: -0°C to +85°C 8: 0°C to +50°C	
Stability	3: ±100 ppm 4: ±50 ppm 6: ±25 ppm 8: ±20 ppm	
Enable/Disable	B: Enable High (pin 1) G: Enable High (pin 2) S: Enable Low (pin 1) M: Enable Low (pin 2) U: No Enable/Disable	
Symmetry/Output Logic Type	L: 45/55% LVDS P: 45/55% PECL H: 40/60% LVDS Q: 40/60% PECL	
Package/Lead Configurations	N: Leadless Ceramic (6 pads)	
Frequency (customer specified)		

M2013Sxxx - Contact factory for datasheet.



SUGGESTED SOLDER PAD LAYOUT



PIN 1 ENABLE

- Pad1: Enable/Disable
- Pad2: N/C
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q̄ (LVPECL, LVDS, CML)
- Pad6: Vcc

PIN 2 ENABLE

- Pad1: N/C
- Pad2: Enable/Disable
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q (LVPECL, LVDS, CML)
- Pad6: Vcc

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		700	MHz	
Operating Temperature	T _A	(See ordering information)				
Storage Temperature	T _S	-55		+125	°C	
Frequency Stability	ΔF/F	(See ordering information)				
Aging						See Note 1
1st Year		-3/-5		+3/+5	ppm	<52 MHz/ ≥52 MHz
Thereafter (per year)		-1/-2		+1/-2	ppm	<52 MHz/ ≥52 MHz
Input Voltage	V _{cc}	3.135	3.3	3.465	V	
Input Current	I _{cc}					
0.75 to 24 MHz				70/30	mA	PECL/LVDS
24 to 700 MHz				100/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load		50 Ohms to V _{cc} - 2 VCD 100 Ohm differential load				See Note 2 PECL Waveform LVDS Waveform
Symmetry (Duty Cycle)		(See ordering information)				@ 50% of waveform
Output Skew				200	ps	PECL
Differential Voltage	V _{od}	250	350	450	mV	LVDS
Logic "1" Level	V _{oh}	V _{cc} -1.02			V	LVPECL
Logic "0" Level	V _{ol}			V _{cc} -1.63	V	LVPECL
Rise/Fall Time	T _r /T _f		0.35 0.50	0.55 1.0	ns	@ 20/80% LVPECL @ 20/80% LVDS
Enable Function		80% V _{cc} min or N/C output active 20% V _{cc} max: output disables to high-Z				Output Option B
		PECL low, GND, or N/C – output active PECL high 0 output disables to high-Z				Output Option S
Start up Time				10	ms	
Phase Jitter (Typical)	ϕ _J		2.25 0.35 2.85 1.95 1.30		ps RMS ps RMS ps RMS ps RMS ps RMS	See Note 3 Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz
Mechanical Shock		MIL-STD-202, Method 213, C (100 g's)				
Vibration		MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)				
Thermal Cycle		MIL-STD-883, Method 1010, B (-55°C to +125°C, 15 min dwell, 10 cycles)				
Hermeticity		MIL-STD-202, Method 112				
Solderability		Per EIAJ-STD-002				
Max Soldering Conditions		See solder profile, Figure 1				

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage and aging.
2. PECL load - see Load Circuit Diagram #5. LVDS load – see load circuit diagram #9. Consult factory with nonstandard output load requirements.
3. Consult factory for phase jitter at other specific frequencies.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

MtronPTI Lead Free Solder Profile

