HM62V8512B Series

4 M SRAM (512-kword × 8-bit)

HITACHI

ADE-203-905G (Z)
Rev. 6.0
Mar. 31, 2000

Description

The Hitachi HM62V8512B is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 µm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II is available for high density mounting. The HM62V8512B is suitable for battery backup system.

Features

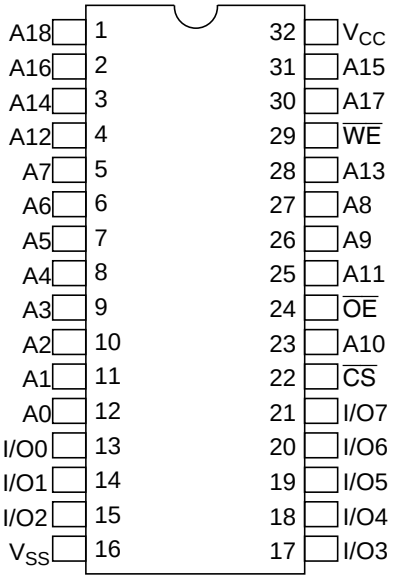
- Single 3.0 V supply: 2.7 V to 3.6 V
- Access time: 70/85 ns (max)
- Power dissipation
  - Active: 15 mW/MHz (typ)
  - Standby: 3 µW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly LV-TTL compatible: All inputs
- Battery backup operation

Ordering Information

Type No.	Access time	Package
HM62V8512BLFP-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8512BLFP-8	85 ns	
HM62V8512BLFP-7SL	70 ns	
HM62V8512BLFP-8SL	85 ns	
HM62V8512BLFP-7UL	70 ns	
HM62V8512BLFP-8UL	85 ns	
HM62V8512BLTT-7	70 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM62V8512BLTT-8	85 ns	
HM62V8512BLTT-7SL	70 ns	
HM62V8512BLTT-8SL	85 ns	
HM62V8512BLTT-7UL	70 ns	
HM62V8512BLTT-8UL	85 ns	
HM62V8512BLRR-7	70 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM62V8512BLRR-8	85 ns	
HM62V8512BLRR-7SL	70 ns	
HM62V8512BLRR-8SL	85 ns	
HM62V8512BLRR-7UL	70 ns	
HM62V8512BLRR-8UL	85 ns	

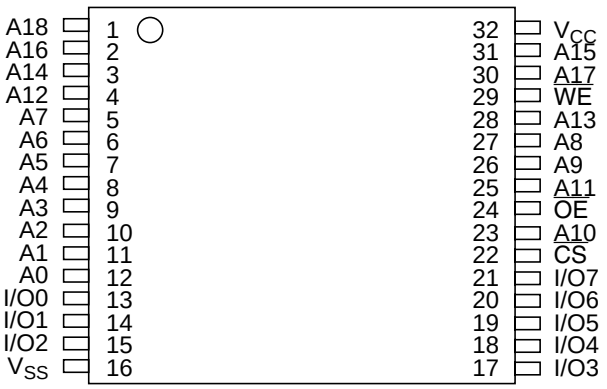
Pin Arrangement

HM62V8512BLFP Series



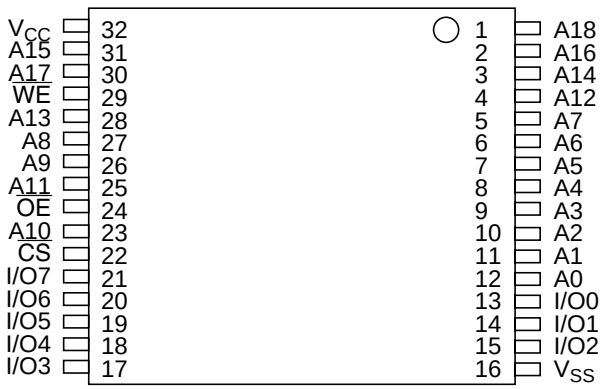
(Top view)

HM62V8512BLTT Series



(Top view)

HM62V8512BLRR Series

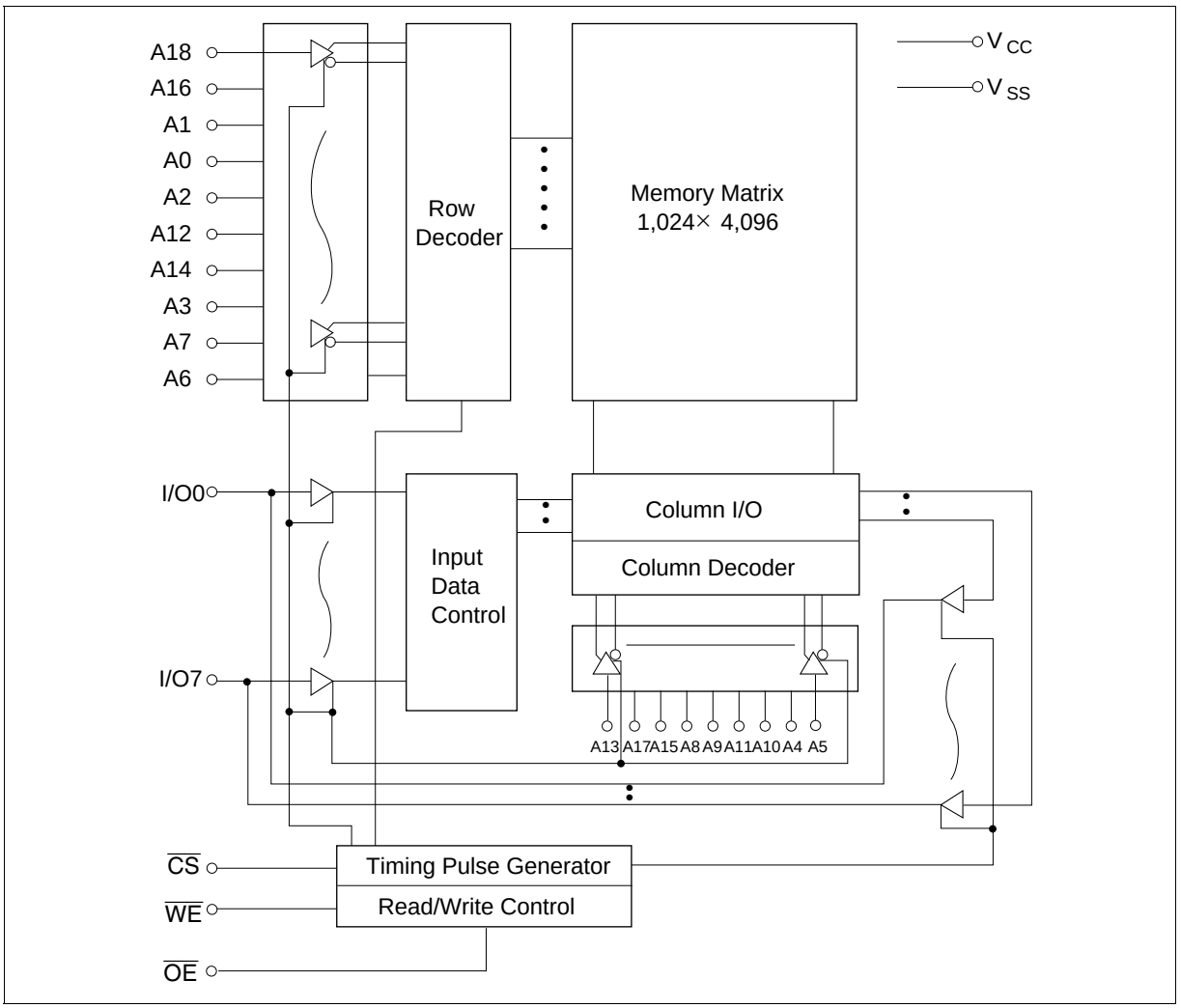


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
×	H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.5*[2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	–20 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–20 to +85	°C

Notes: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 4.6 V

Recommended DC Operating Conditions (Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*[1]	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = –20 to +70°C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	—	10	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	I_{CC1}	—	—	40	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
Operating power supply current	I_{CC2}	—	5	10	mA	Cycle time = 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC	I_{SB}	—	0.1	0.3	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1): DC	I_{SB1}	—	1*[2]	40*[2]	µA	Vin ≥ 0 V, $\overline{CS}$ ≥ V_{CC} – 0.2 V
		—	1*[3]	20*[3]	µA	
		—	1*[4]	5*[4]	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
		—	—	0.2	V	I_{OL} = 100 µA
Output high voltage	V_{OH}	V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
		2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.
4. This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	8	pF	Vin = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –20 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference level: 1.5 V/1.5 V(HM62V8512B-7)
  0.8 V/2.0 V(HM62V8512B-8)

  Output load: 1 TTL Gate + C_L (50 pF)
  (Including scope & jig)

Read Cycle

		HM62V8512B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip select access time	t_{CO}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	35	—	45	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{HZ}	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

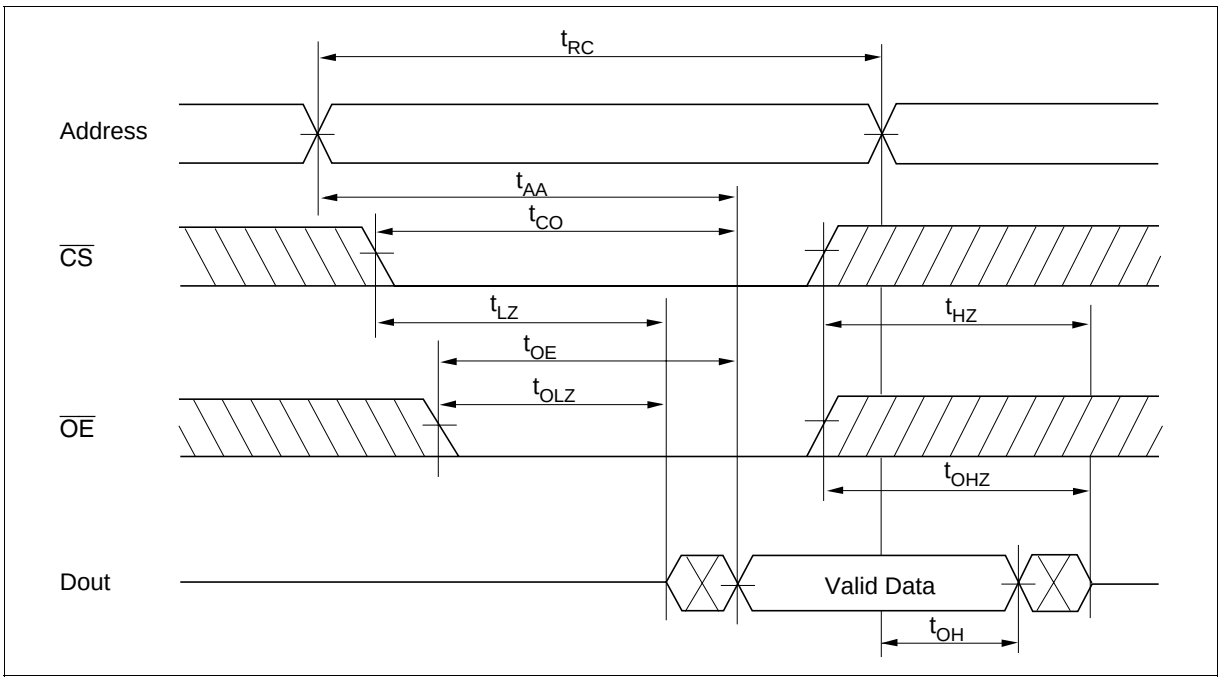
Write Cycle

		HM62V8512B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	60	—	75	—	ns	
Write pulse width	t_{WP}	50	—	55	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2, 7

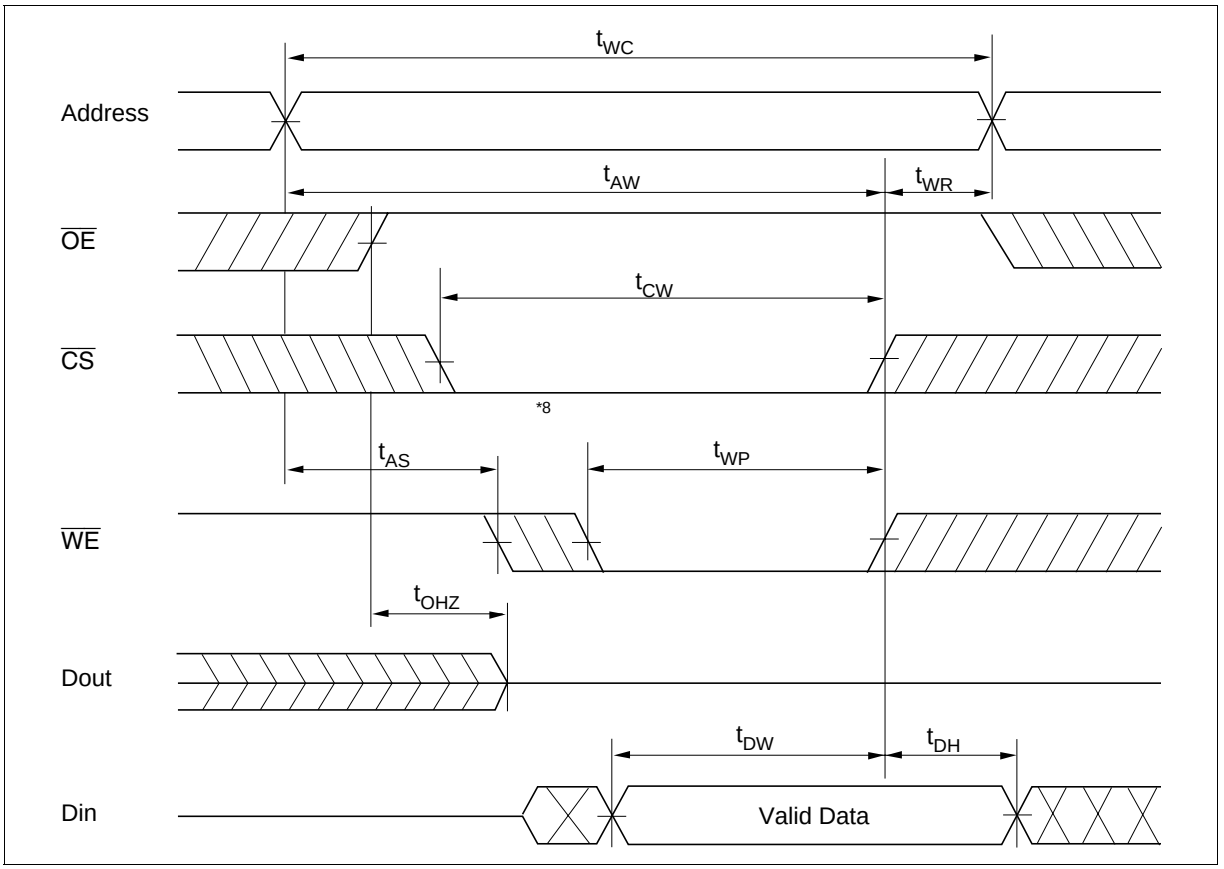
Notes:
1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveforms

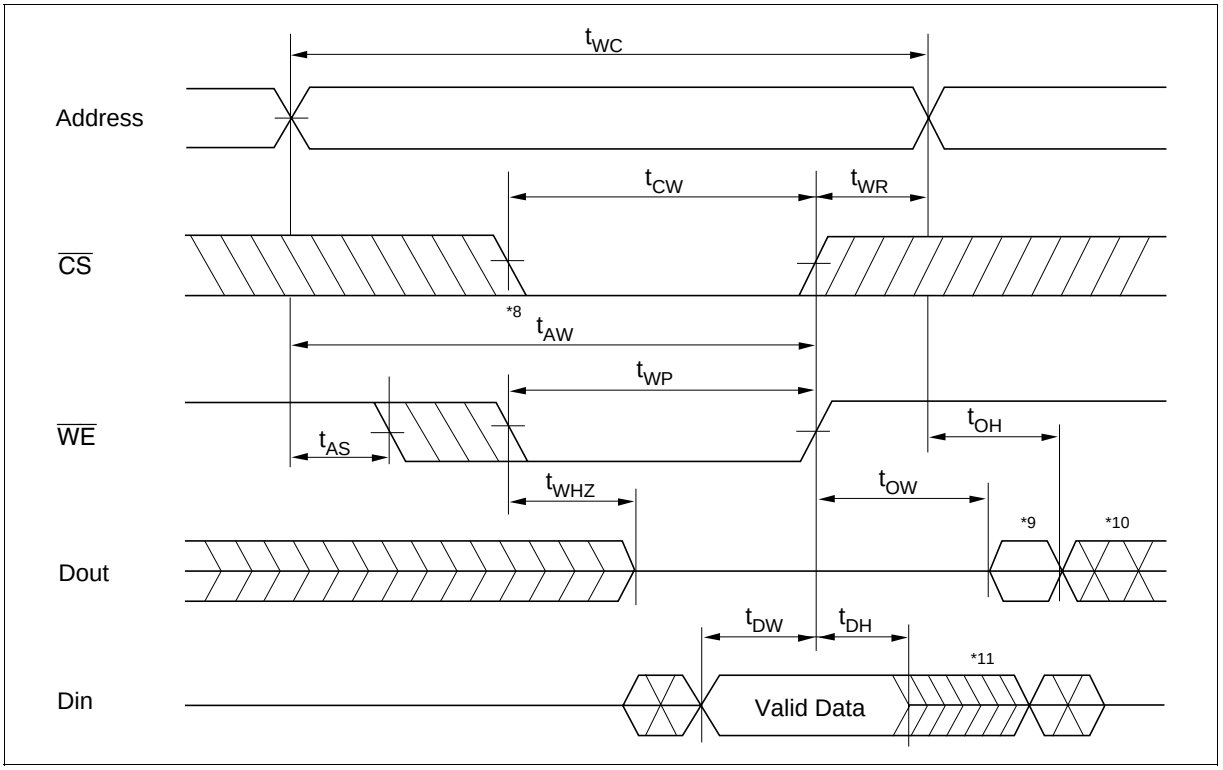
Read Timing Waveform ($\overline{WE}$ = V_{IH})



Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)

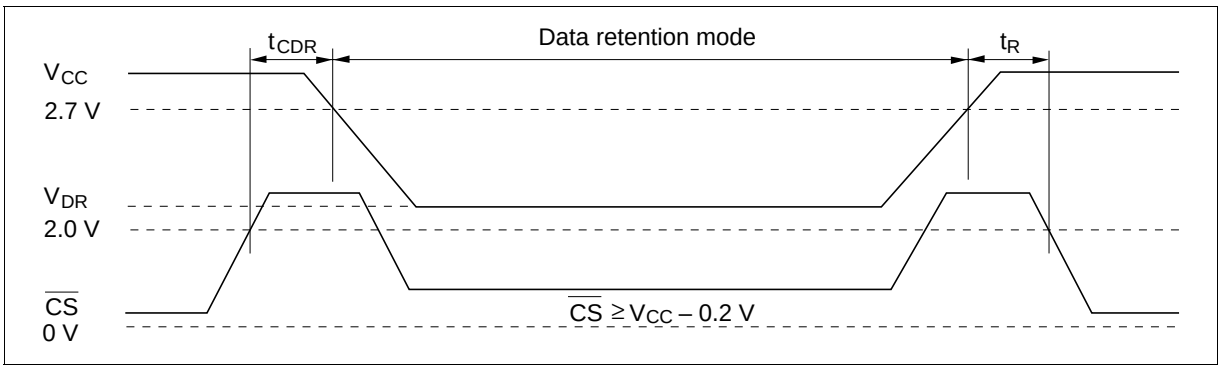


Low V_{CC} Data Retention Characteristics (Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*4
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	0.8*5	20*1	µA	V_{CC} = 3.0 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2$ V
		—	0.8*5	10*2	µA	
		—	0.8*5	2*3	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*6	—	—	ns	

Notes: 1. For L-version and 10 µA (max.) at Ta = –20 to +40°C.
2. For L-SL-version and 3 µA (max.) at Ta = –20 to +40°C.
3. For L-UL-version and 2 µA (max.) at Ta = –20 to +40°C.
4. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
5. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
6. t_{RC} = read cycle time.

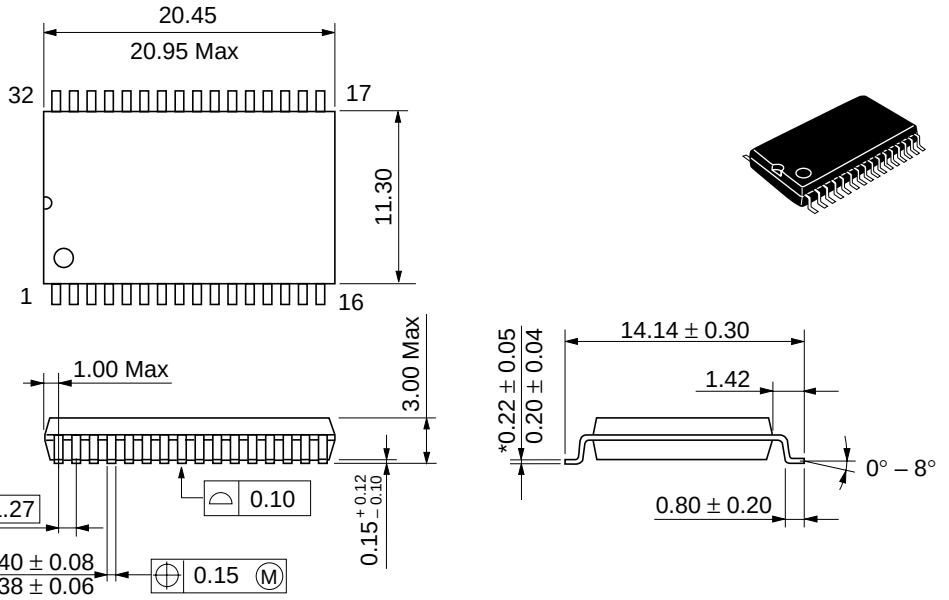
Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



Package Dimensions

HM62V8512BLFP Series (FP-32D)

Unit: mm



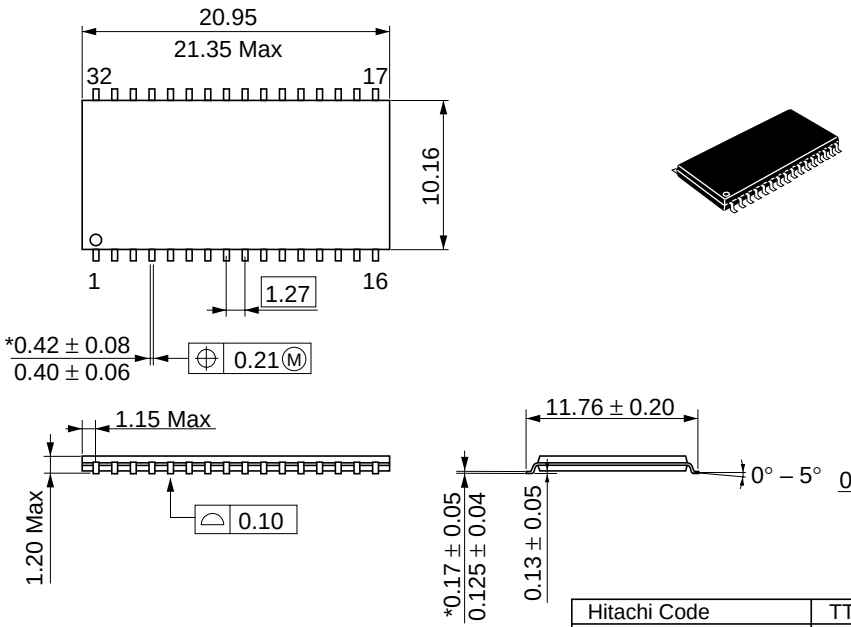
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

Package Dimensions (cont.)

HM62V8512BLTT Series (TTP-32D**)**

Unit: mm



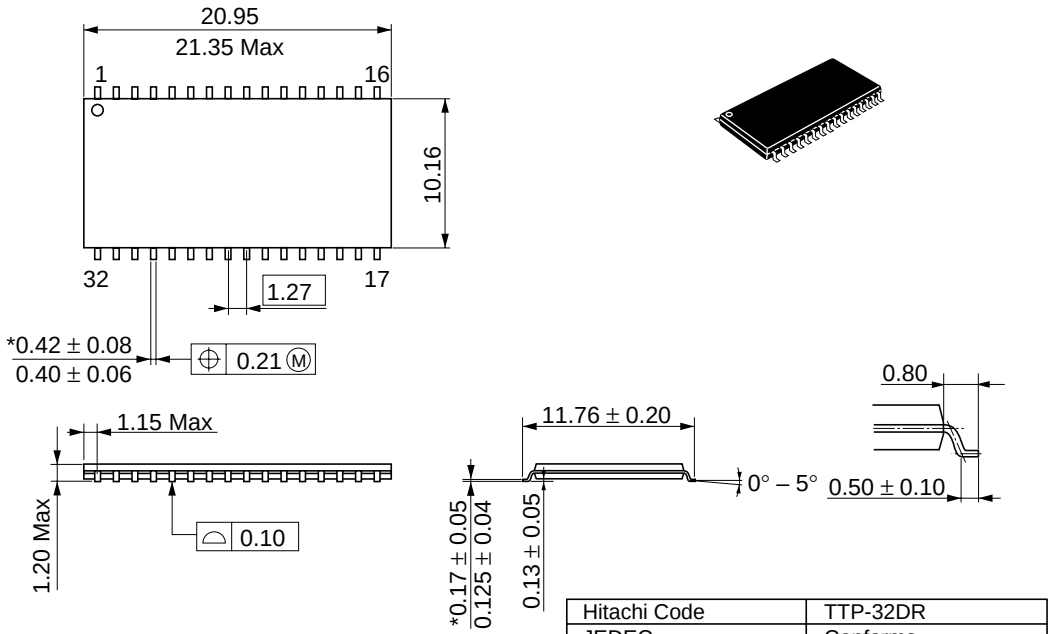
*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Package Dimensions (cont.)

HM62V8512BLRR Series (TTP-32DR)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 24, 1998	Initial issue	M. Higuchi	K. Imato
0.1	Nov. 19, 1998	DC Characteristics I_{CC1} max: 30 mA to 40 mA I_{SB1} max: 20/2 µA to 40/20 µA Low V_{CC} Data Retention Characteristics I_{CCDR} max: 10/1 µA to 20/10 µA Change of note1 and 2	S. Kunito	K. Imato
1.0	Dec. 17, 1998	Deletion of Preliminary Features Change of Power dissipation Active: TBD (typ) to 15 mW/MHz (typ) Standby: TBD (typ) to 3 µW (typ) DC Characteristics I_{CC2} typ: TBD to 5 mA I_{SB1} typ: TBD/TBD to 1/1 µA Low V_{CC} Data Retention Characteristics I_{CCDR} typ: TBD/TBD to 0.8/0.8 µA	S. Kunito	K. Imato
2.0	Jan. 29, 1999	Low V_{CC} Data Retention Characteristics Change of Low V_{CC} Data Retention Timmng Waveform	S. Kunito	K. Imato
3.0	Apr. 8, 1999	Addition of L-UL-version DC Characteristics I_{SB1} typ: 1/1 µA to 1/1/1 µA I_{SB1} max: 40/20 µA to 40/20/5 µA Addition of note4 Low V_{CC} Data Retention Characteristics I_{CCDR} typ: 0.8/0.8 µA to 0.8/0.8/0.8 µA I_{CCDR} max: 20/10 µA to 20/10/2 µA Addition of note3	S. Kunito	K. Imato
4.0	Aug. 24, 1999	Low V_{CC} Data Retention Characteristics Correct error: t_R unit ms to ns	S. Kunito	K. Imato
5.0	Oct. 20, 1999	Low V_{CC} Data Retention Characteristics Change of Low V_{CC} Data Retention Timmng Waveform	I. Ogiwara	K. Imato
6.0	Mar. 31, 2000	AC Characteristics Test Conditions: Output timing reference level 0.8 V/2.0 V to 1.5 V/1.5 V (HM62V8512B-7) 0.8 V/2.0 V (HM62V8512B-8)		