ARA2017

Programmable Gain Amplifier

PRELIMINARY DATA SHEET - Rev 1.0

FEATURES

- High Linearity, High Output Power Integrated Amplifier with Programmable Gain Control
- Attenuation Range: 0-58 dB, Adjustable in 2 dB Increments via a 3-wire Serial Control
- 33 dB Gain (at Minimum Attenuation)
- Low Distortion Products at Output Power Levels up to +64 dBmV
- Low Noise Figure and Output Noise
- Frequency range: 5-85 MHz
- 5 V Operation
- Materials set consistent with RoHS Directors. Surface Mount Package

APPLICATIONS

- DOCSIS 3.0 Data Cable Modems and E-MTAs
- CATV Set Top Boxes

S29 Package
28-Pin QFN
5 mm x 5 mm x 1 mm

PRODUCT DESCRIPTION

The ARA2017 is a highly linear, high output power, programmable gain amplifier optimized for DOCSIS 3.0 cable modem and E-MTA applications. Using a low noise input amplification stage and an ultra linear output driver amplifier, the device generates extremely low distortion products at the high output power levels required by DOCSIS 3.0 signals. Its balanced circuit design provides superior harmonic performance and an integrated digitally-controlled, multiple-stage precision step attenuator enables system solutions to meet DOCSIS power step accuracy requirements.

The ARA2017 supports output power levels of +64 dBmV while minimizing harmonic, distortion, and output noise levels. Its precision attenuator provides up to 58 dB of attenuation in 2 dB increments. The attenuator setting is programmed via a 3-wire serial interface, as is the output stage current, a feature which allows the device to be operated in reduced power modes for extended backup battery life in E-MTA applications. The ARA2017 is offered in a 28-pin 5 mm x 5 mm x 1 mm QFN package.

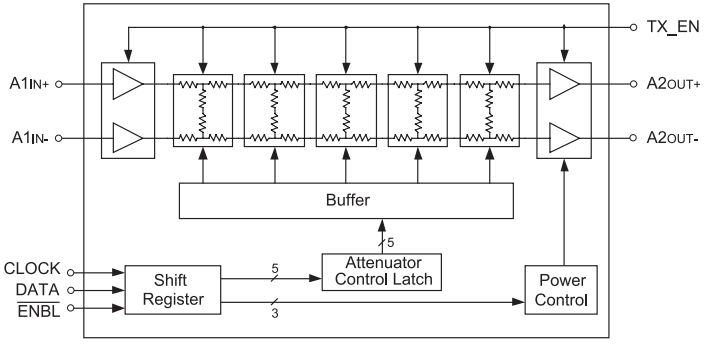


Figure 1: Functional Block Diagram

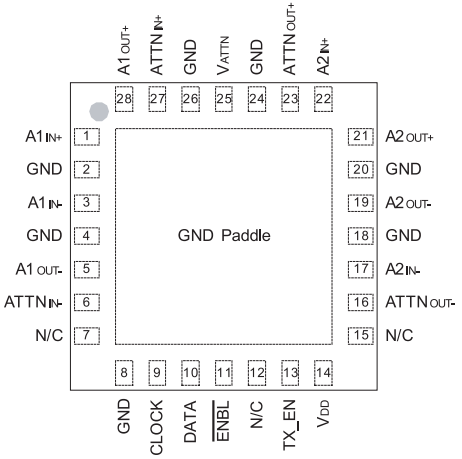


Figure 2: Pinout (X-Ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	$A1_{IN+}$	Amplifier A1 (+) Input	28	$A1_{OUT+}$	Amplifier A1 (+) Output and Supply
2	GND	Ground	27	$ATTN_{IN+}$	Attentuator Input (+)
3	$A1_{IN-}$	Amplifier A1 (-) Input	26	GND	Ground
4	GND	Ground	25	V_{ATTN}	Attenuator Supply
5	$A1_{OUT-}$	Amplifier A1 (-) Output and Supply	24	GND	Ground
6	$ATTN_{IN-}$	Attentuator Input (-)	23	$ATTN_{OUT+}$	Attentuator Output (+)
7	N/C	No Connection	22	$A2_{IN+}$	Amplifier A2 (+) Input
8	GND	Ground	21	$A2_{OUT+}$	Amplifier A2 (+) Output and Supply
9	CLOCK	Clock	20	GND	Ground
10	DATA	Data	19	$A2_{OUT-}$	Amplifier A2 (-) Output and Supply
11	ENBL	Enable	18	GND	Ground
12	N/C	No Connection (Reserved for future use - leave floating)	17	$A2_{IN-}$	Amplifier A2 (-) Input
13	TX_EN	Transmit Enable	16	$ATTN_{OUT-}$	Attentuator Output (-)
14	V_{DD}	Supply	15	N/C	No Connection

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT	COMMENTS
Supply: V_{DD} (pins 5, 14, 19, 21, 28), V_{ATTN} (pin 25)	0	+6	V	
RF Power at Inputs (pins 1, 3)	-	+40	dBmV	differential into 200 Ω
Digital Interface (pins 9, 10, 11, 13)	-0.5	V_{DD}+0.5	V	
Storage Temperature	-55	+150	°C	

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Operating Frequency (f)	5	-	85	MHz
Supply: V_{DD} (pins 5, 14, 19, 21, 28)	+4.5	+5	+5.5	V
Digital Interface (pins 9, 10, 11, 13)	0	-	V_{DD}	V
Case Temperature (T_C)	-20	+25	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Digital Interface Specifications
(V_{DD} = +5.0 V)

PARAMETER	MIN	TYP	MAX	UNIT
Logic High Input Voltage: $V_{IN,HIGH}$	+2.0	-	V_{DD}	V
Logic Low Input Voltage: $V_{IN,LOW}$	0	-	+0.8	V

Note:
1. Logic control levels apply to the 3-wire programming bus (pins 9, 10, 11) and the transmit enable control (pin 13).

Table 5: Electrical Specifications
V_{DD} = +5.0 V, T_X Enabled, (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	34	36	37	dB	0 dB attenuation setting
Gain Flatness	- -	0.5 1.0	- -	dB	5 to 42 MHz 5 to 85 MHz
Gain Variation over Temperature	-	-0.02	-	dB/°C	
Gain Range with Attenuator	58	-	-	dB	
Incremental Attenuator Step Size	1.5	2	2.5	dB	
2nd Harmonic Distortion Level (2)	-	-67	-55	dBc	+64 dBmV into 75 Ω
3rd Harmonic Distortion Level (2)	-	-72	-55	dBc	+64 dBmV into 75 Ω
3rd Order Output Intercept (2)	+88	+93	-	dBmV	2 tone, +61 dBmV/tone
1 dB Gain Compression (2)	-	+73	-	dBmV	
Noise Figure	-	2.5	-	dB	Full gain @ 0 dB attenuator setting; Includes input balun loss
Output Noise Power Active / No Signal / Min. Atten. Set. Active / No Signal / Max. Atten. Set.	 - -	 -38.5 -53.8	 - -	dBmV	 Any 160 kHz bandwidth from 5 to 85 MHz
Isolation (85 MHz) in Tx disable mode	-	60	-	dB	
Differential Input Impedance	-	200	-	Ω	between pins 1 and 3 (Tx enabled)
Differential Output Impedance	-	75	-	Ω	between pins 19 and 21
Output Impedance	-	75	-	Ω	with transformer
Output Return Loss (75 Ohm characteristic impedance)	- -	-15 -12	- -	dB	Tx enabled Tx disabled
Output Voltage Transient Tx enable / Tx disable	- -	50 7	- -	mVp-p	0 dB attenuator setting 24 dB attenuator setting
Total Supply Current (2) (pins 5, 14, 19, 21, 25, 28)	- -	340 10.5	400 -	mA	Tx enabled (TX_EN high) Tx disabled (TX_EN low)
Total Power Consumption	- -	1.7 52.5	- -	W mW	Tx enabled (TX_EN high) Tx disabled (TX_EN low)

Notes:
1. As measured in ANADIGICS test fixture.
(2) Measured using the maximum current setting-see Application Information section.

DATA PLOTS

Figure 3: Gain vs Frequency over Voltage
(T_C = 25 °C)

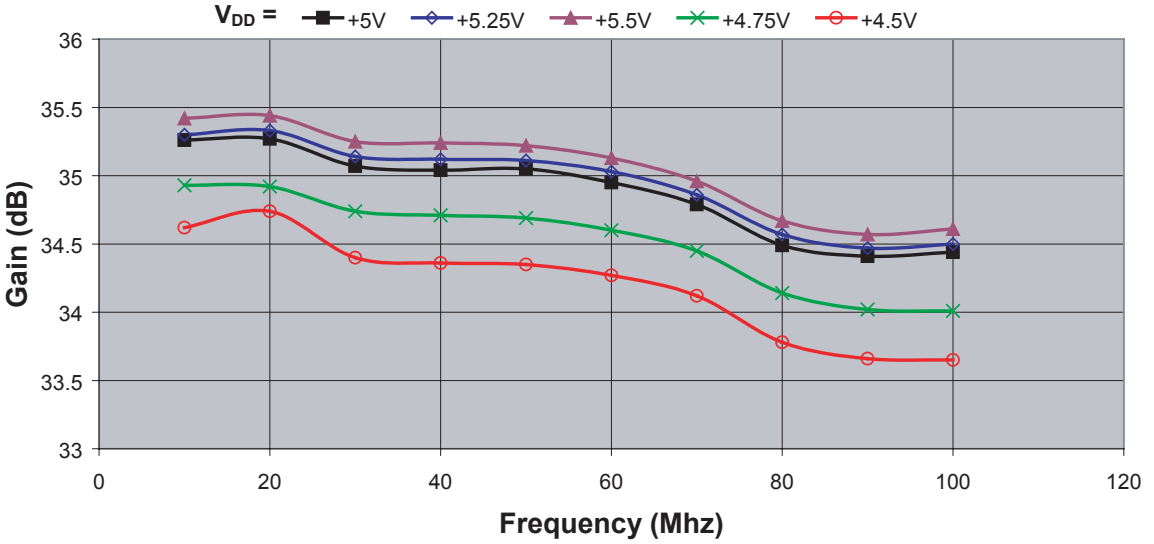


Figure 4: Gain vs Temperature
(V_{DC} = +5V, F1 = 10 MHz)

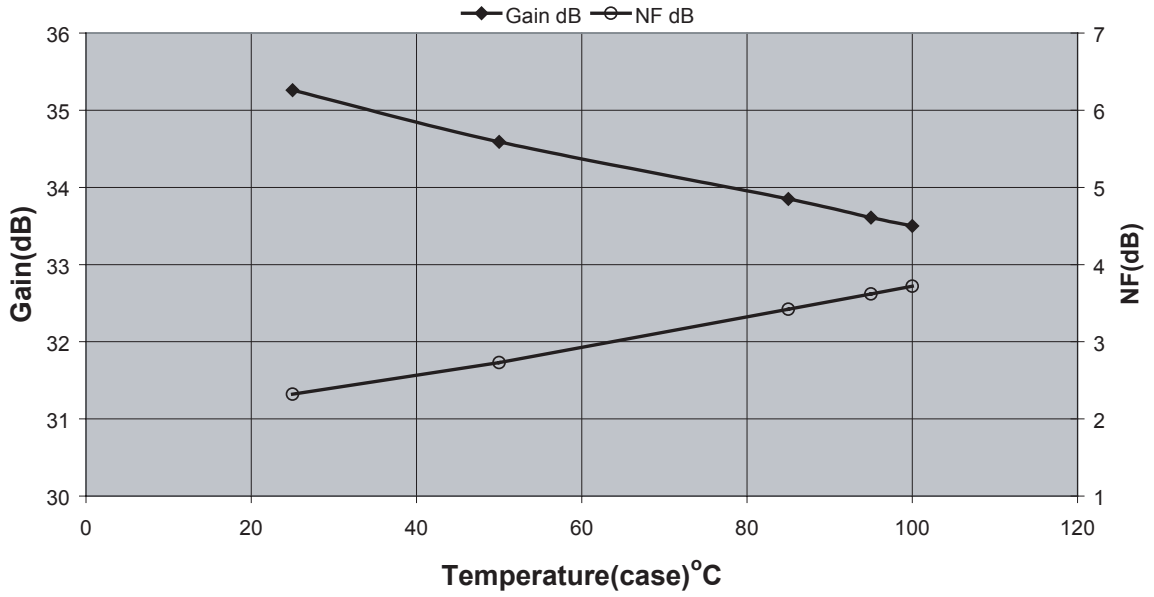


Figure 5: NF vs Frequency over Voltage

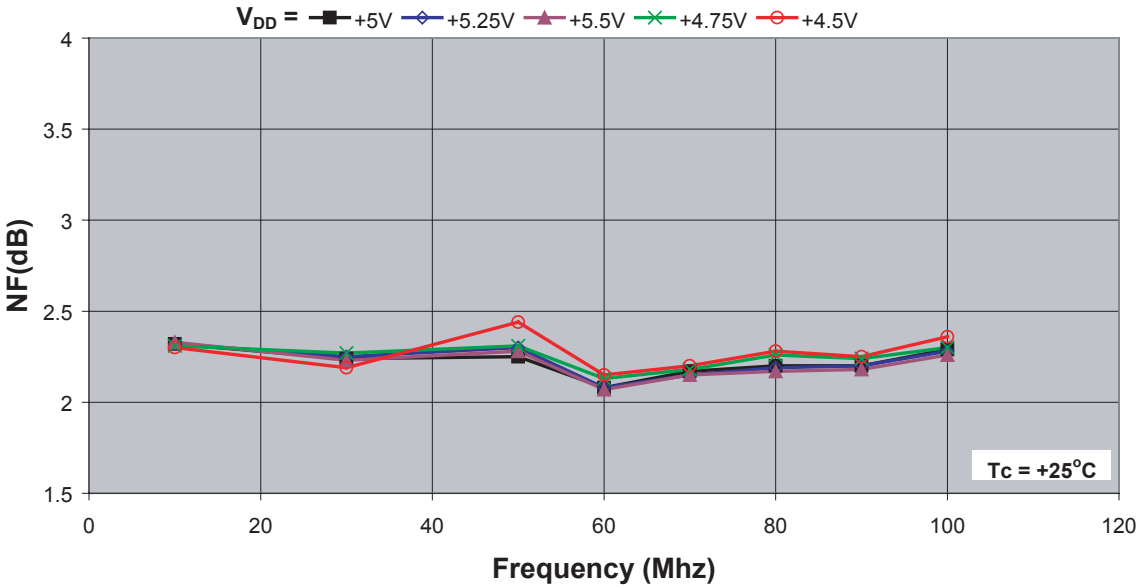


Figure 6: Output Power at 1dB Gain Compression (P1dB) vs. Case Temperature (V_{DD} = +5V, F1 = 10MHz)

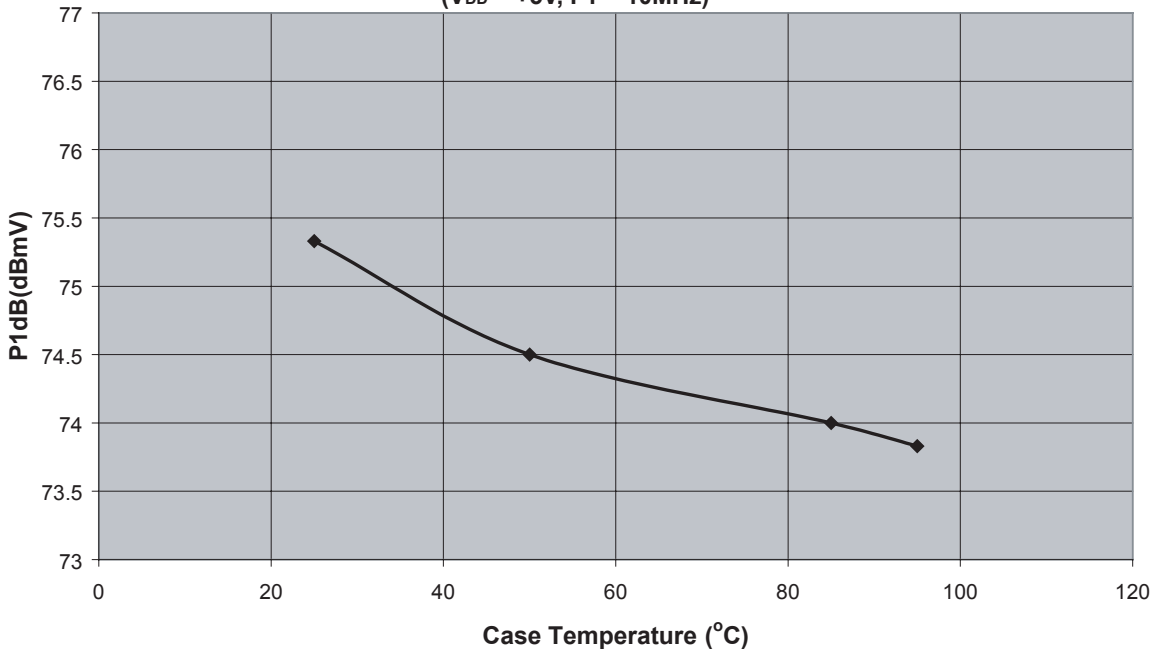


Figure 7: Output Power at 1dB Gain Compression (P1dB) vs Voltage (Tc = 25 °C, F1 = 10MHz)

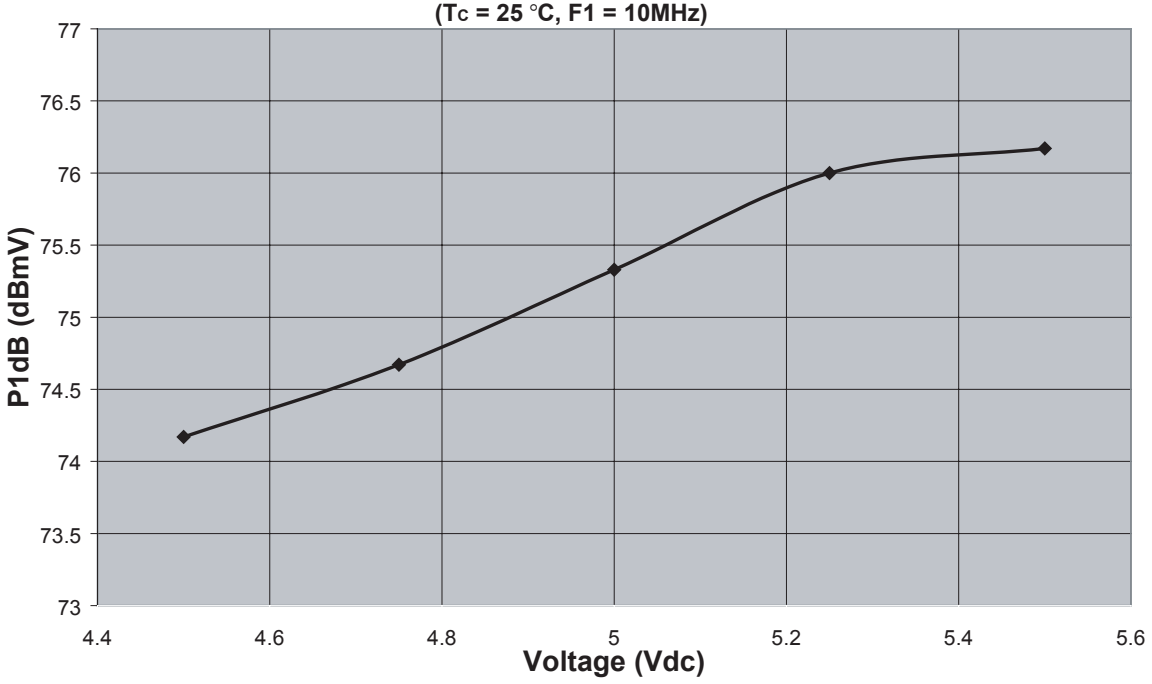


Figure 8: Output Third Order Intercept Point (OIP3) vs. Case Temperature

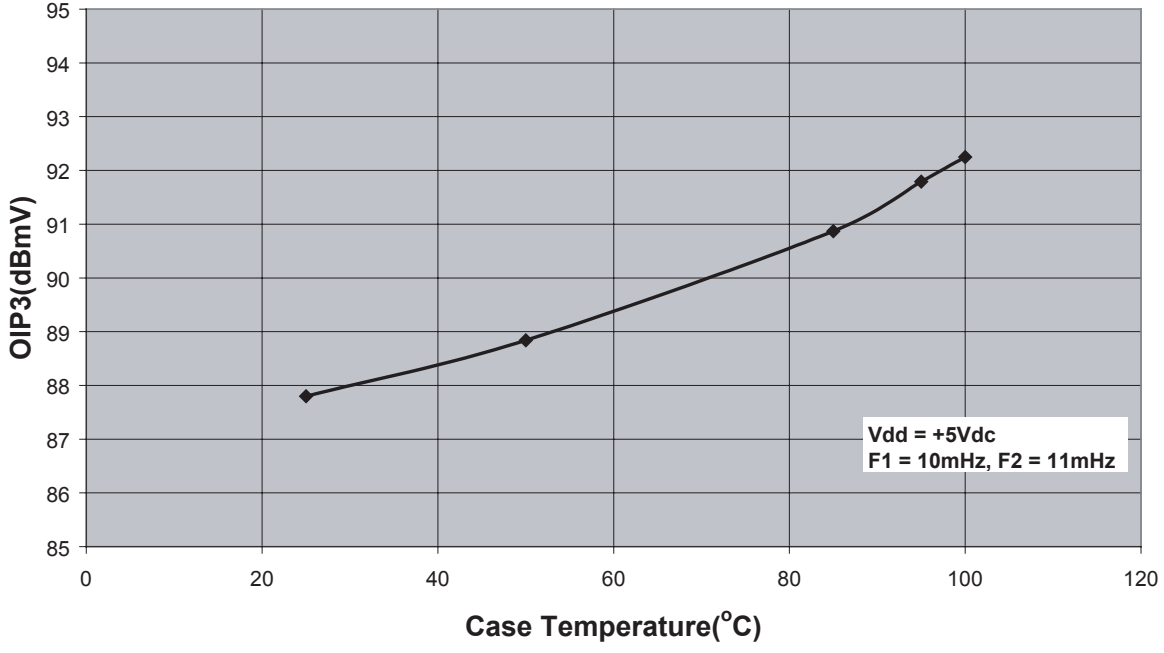


Figure 9: Output Third Order Intercept Point (OIP3) vs Voltage

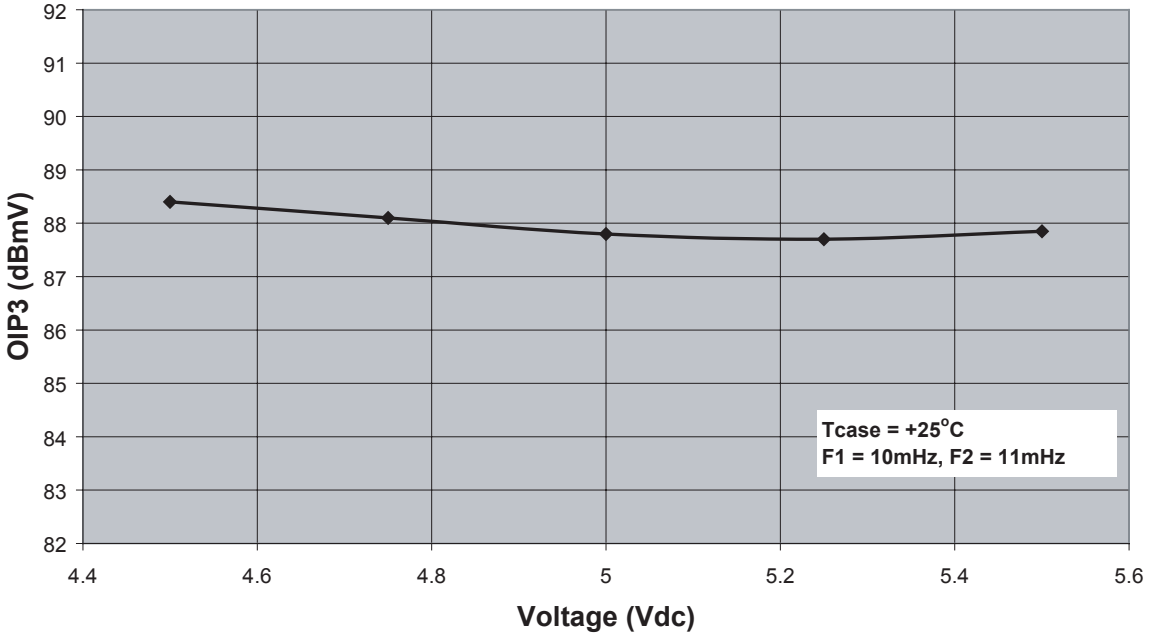


Figure 10: Attenuator Accuracy over Frequency (T_C = 25 °C, V_{DC} = +5V)

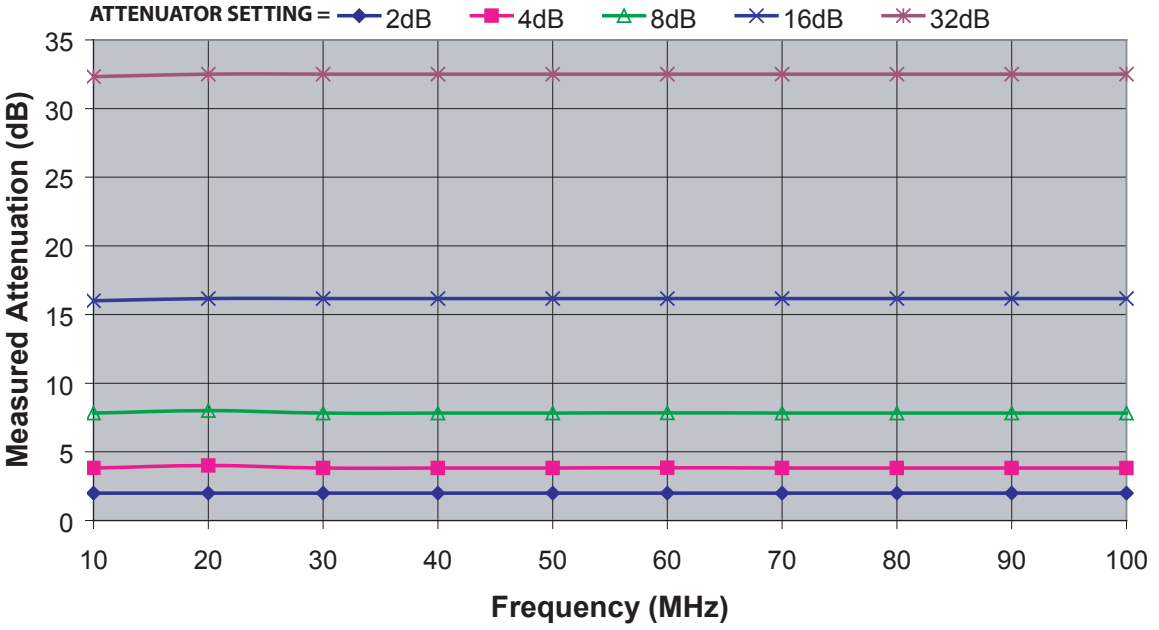


Figure 11:Attenuator Accuracy over Voltage
(T_C = +25 °C, F1 = 10MHz)

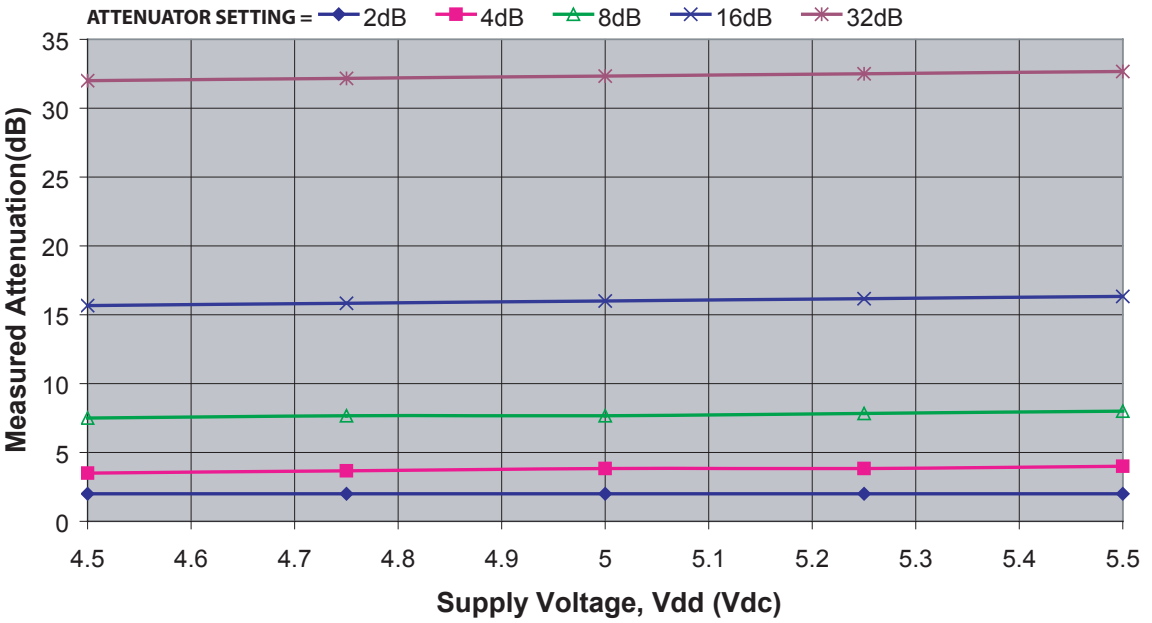
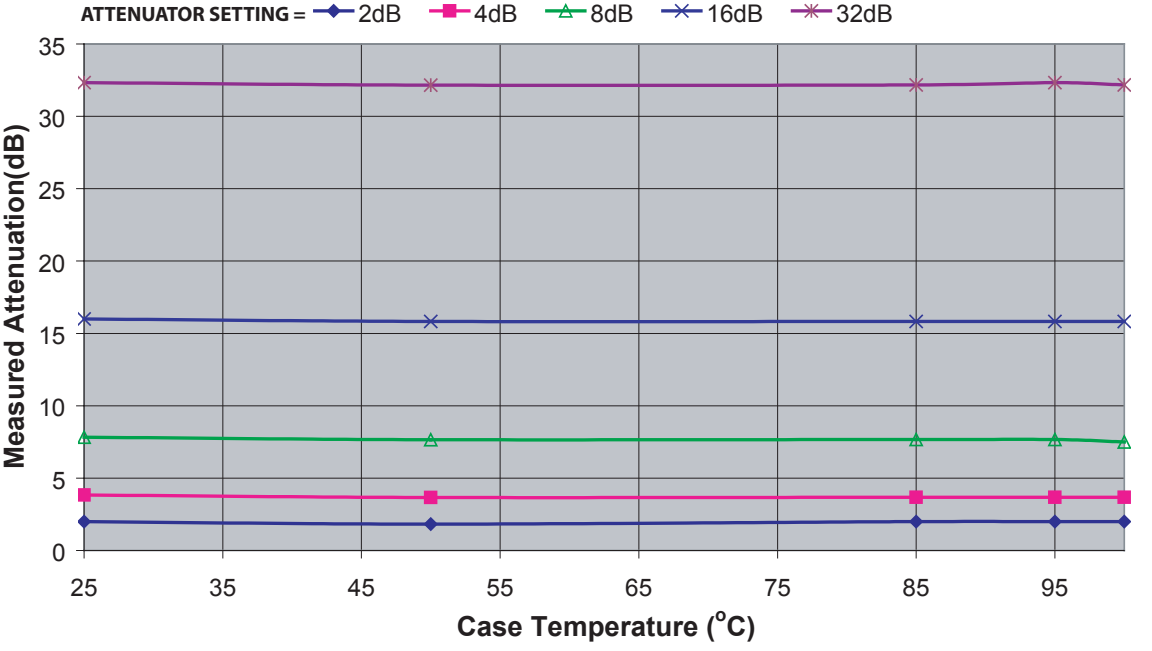


Figure 12: Attenuator Accuracy over Temperature
(V_{DC} = +5V, F1 = 10MHz)



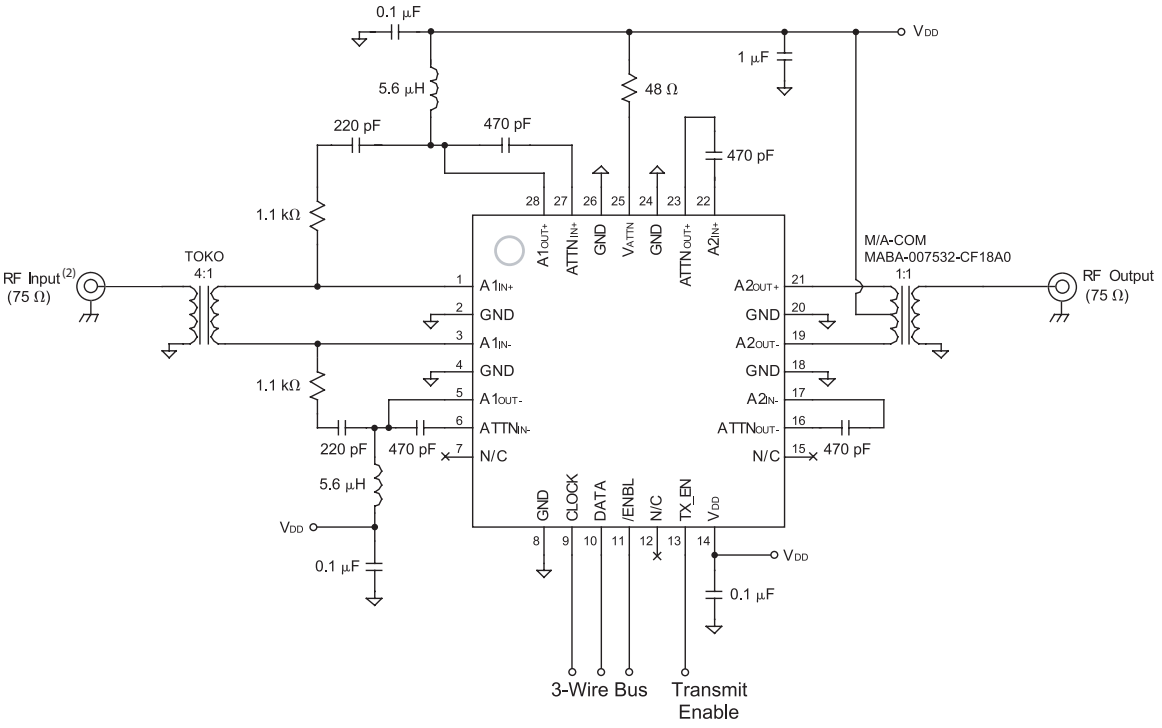


Figure 13: Test Circuit

NOTES:
1. Pin 12 is reserved for future use. Do not connect (leave floating).
(2) Input balun is used for evaluation test purposes only in 75 Ω system. Actual application does not require a 4:1 balun on the input.

LOGIC PROGRAMMING

Programming Instructions

The programming word is set through a 10 bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last. The enable line must be low for the duration of the data entry, then set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

Table 6: Programming Register

DATA BIT	9	8	7	6	5	4	3	2	1	0
FUNCTION	Current			Gain					0	1

Notes:
1. Refer to Application Information section for Current and Gain bit settings.
2. Data bit 0 should always be set to "1".
3. Data bit 1 is reserved for future use, and should be set to "0".

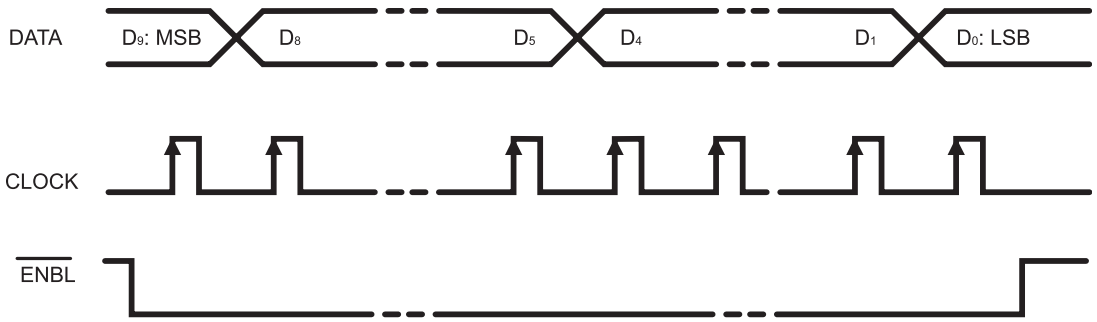


Figure 14: Serial Data Input Timing

APPLICATION INFORMATION

Transmit Enable / Disable

The ARA2017 can be switched on (Tx enable) and off (Tx disable) via an asynchronous input TX_EN (pin 13). A logic high will turn the amplifier on. The gain and current settings are retained during Tx disable and do not need to be reloaded.

Gain/Attenuator Setting

The gain of the ARA2017 can be controlled via the 3-wire bus. Data bits D2 through D6 set the gain/ attenuator level, with 00000 being the min gain setting, and 11111 being the max gain setting. A new gain/ attenuator setting can be loaded while the PGA is on (Tx enable), but will not take effect until TX_EN has been cycled off /on.

Output Stage Current Setting

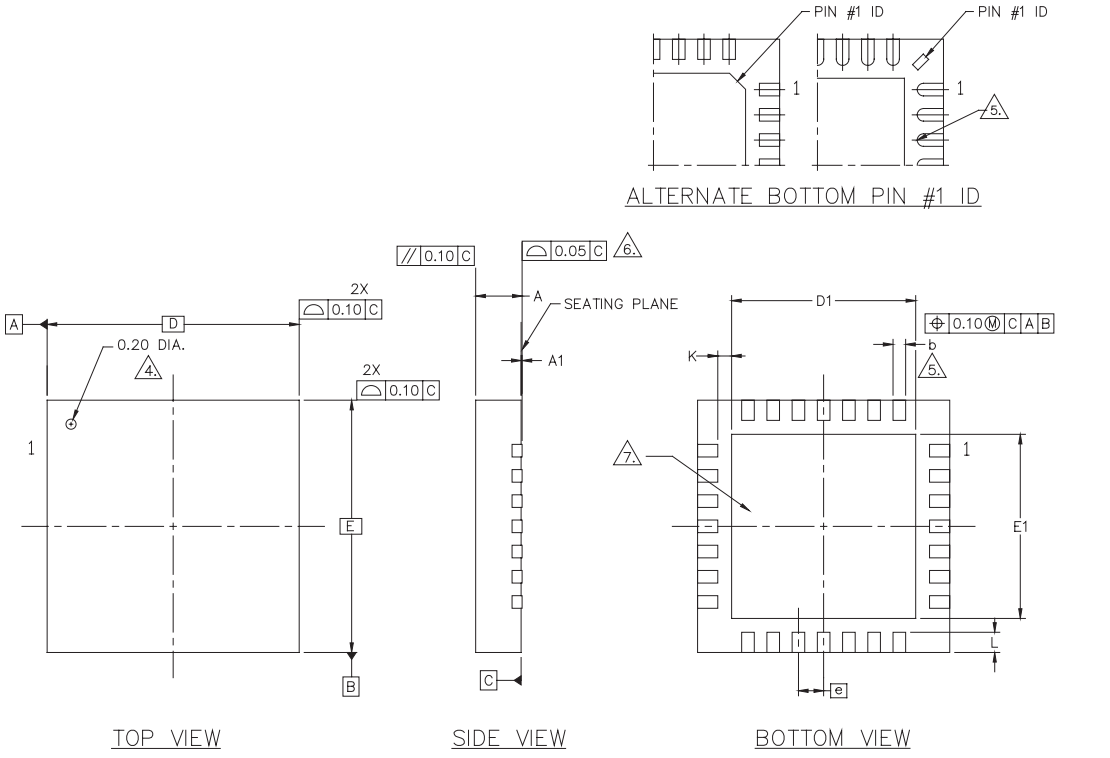
The ARA2017 consists of 2 gain stages. The input stage operates at a constant fixed current when Tx is enabled. The current in the output stage can be controlled via the 3-wire bus. Data bits D7 – D9 set the current. 111 will set the output stage to maximum current for maximum linearity. The current can be lowered for improved efficiency at lower output power levels, or lower linearity requirements. 000 will turn both stages off, the same as Tx disable. A new current setting can be loaded while the PGA is on (Tx Enable), but will not take effect until TX_EN has been cycled off /on.

Output Transformer

Matching the balanced output of the ARA2017 to a single-ended 75 Ω load is accomplished using a 1:1 turns ratio transformer. In addition to the balanced to single-ended conversion, this transformer provides the bias to the output amplifier stage via the center tap.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. As a result, care must be taken when selecting the transformer to be used at the output. It must be capable of handling the RF and DC power requirements without saturating the core, and it must have adequate isolation and good phase and amplitude balance. It also must operate over the desired frequency and temperature range for the intended application.

PACKAGE OUTLINE



SYMBOL	DIMENSIONS–MM MIN.	MAX.	NOTE	SYMBOL	DIMENSIONS–INCHES MIN.	MAX.	NOTE
A	0.80	1.00		A	0.031	0.039	
A1	0.00	0.05		A1	0.000	0.002	
b	0.18	0.30		b	0.007	0.012	
D	5.00 BSC			D	0.197 BSC		
D1	3.40	3.80		D1	0.134	0.149	
E	5.00 BSC			E	0.197 BSC		
E1	3.40	3.80		E1	0.134	0.149	
e	0.50 BSC			e	0.020 BSC		
K	0.20 MIN.			K	0.007 MIN.		
L	0.35	0.57		L	0.014	0.022	

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER MARKED.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL TIP. RADIUS OPTIONAL. DIMENSION b SHOULD NOT BE MEASURED IN RADIUS AREA.
6. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. REFERENCE JEDEC OUTLINE MO–220.

Figure 15: S29 Package Outline - 28 Pin 5 mm x 5 mm x 1 mm QFN

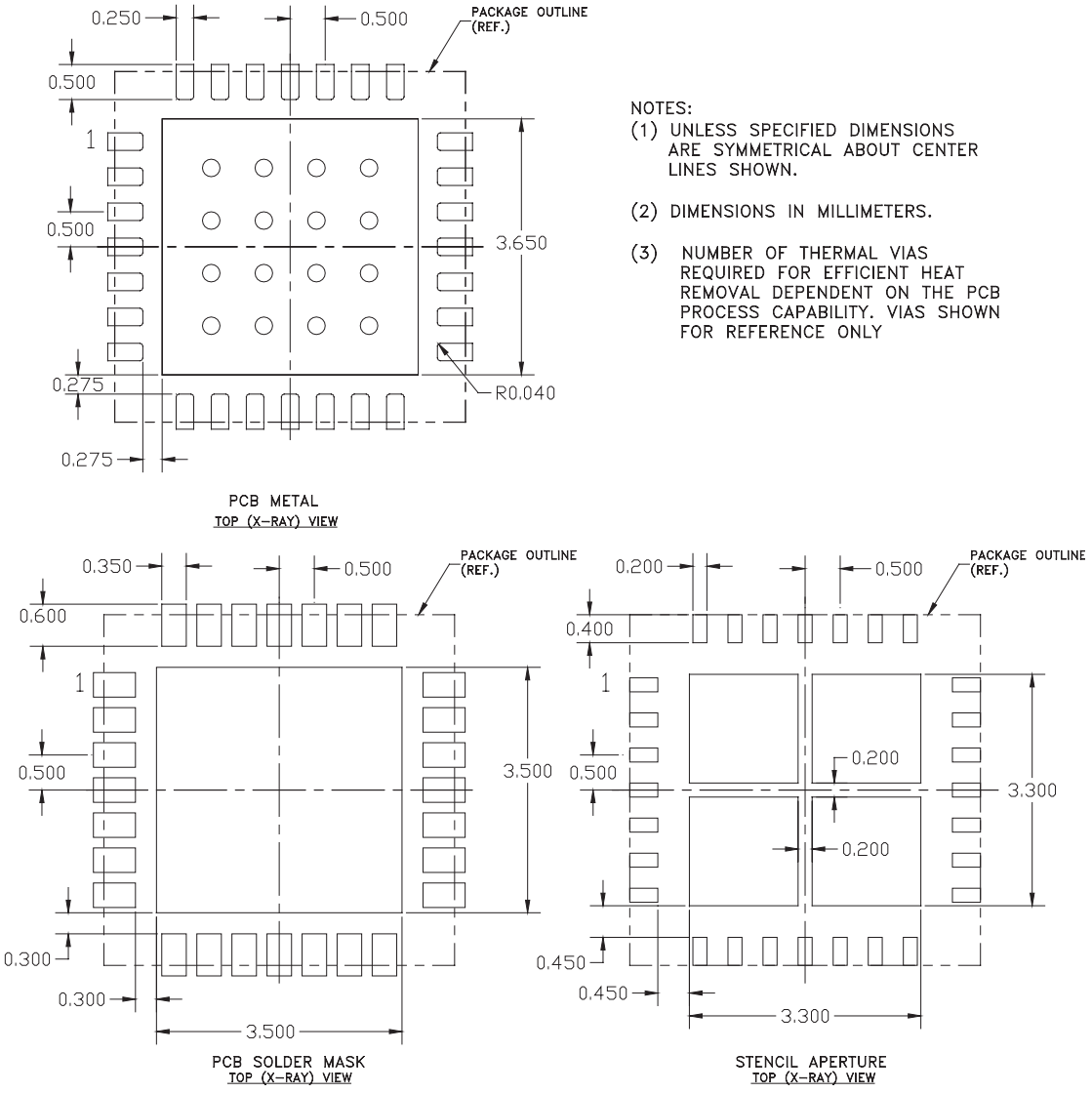


Figure 16: Land Pattern

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ARA2017RS29P8	-20 °C to +85 °C	28 Pin QFN Package 5 mm x 5 mm x 1 mm	Tape and Reel, 2500 pieces per Reel

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