HT1608L
2×20 Channel LCD Driver

Features

- Operating voltage: 2.7V~5.2V
- LCD driving voltage: 3.0V~5.0V
- 40 internal LCD drivers available
- Bias voltage: static to 1/5 bias
- LCD driver with serial/parallel conversion function
- Common or segment driver output by selection

Applications

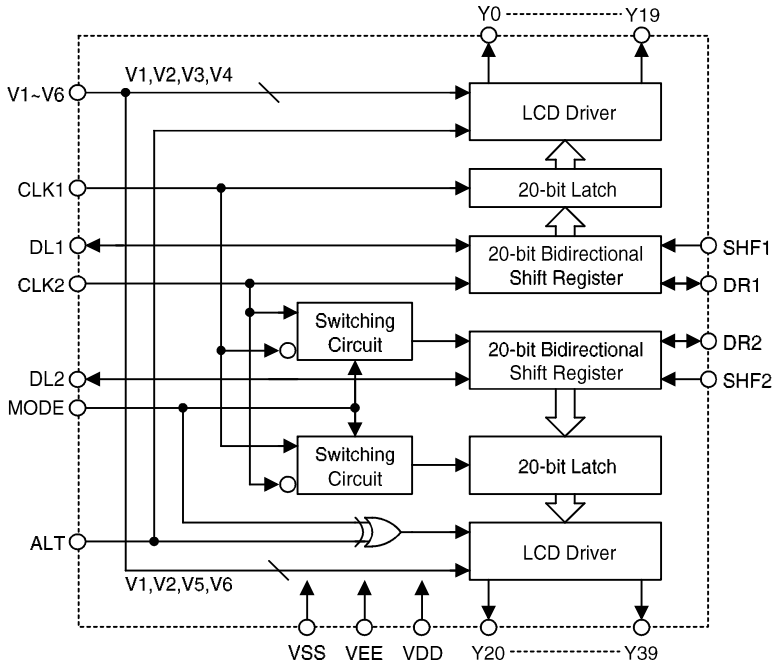
- Electronic dictionaries
- Portable computers
- Remote controllers
- Calculators

General Description

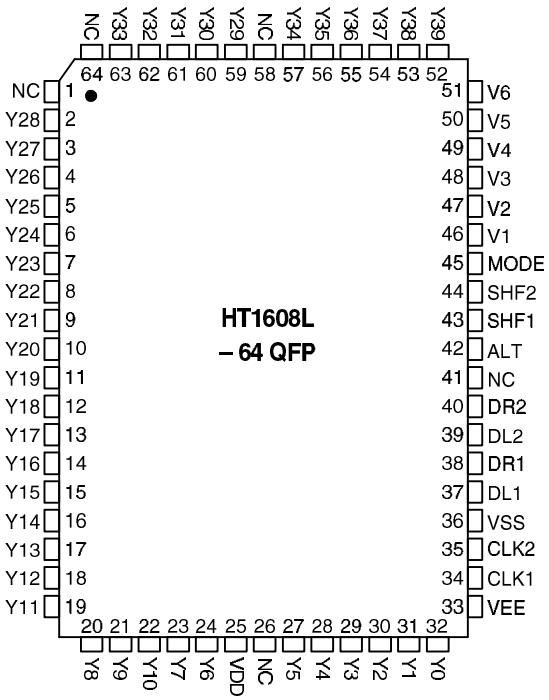
The HT1608L is an LCD driver LSI with 40 output channels using CMOS technology. It is equipped with two sets of 20-bit bidirectional shift registers, 20-bit data latches, 20-bit LCD drivers, and logic control circuits.

The HT1608 can convert serial data received from an LCD controller into parallel data and send out LCD driving waveforms to the LCD panel. The HT1608L is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCDs. The chip can be applied to a common driver or a segment driver.

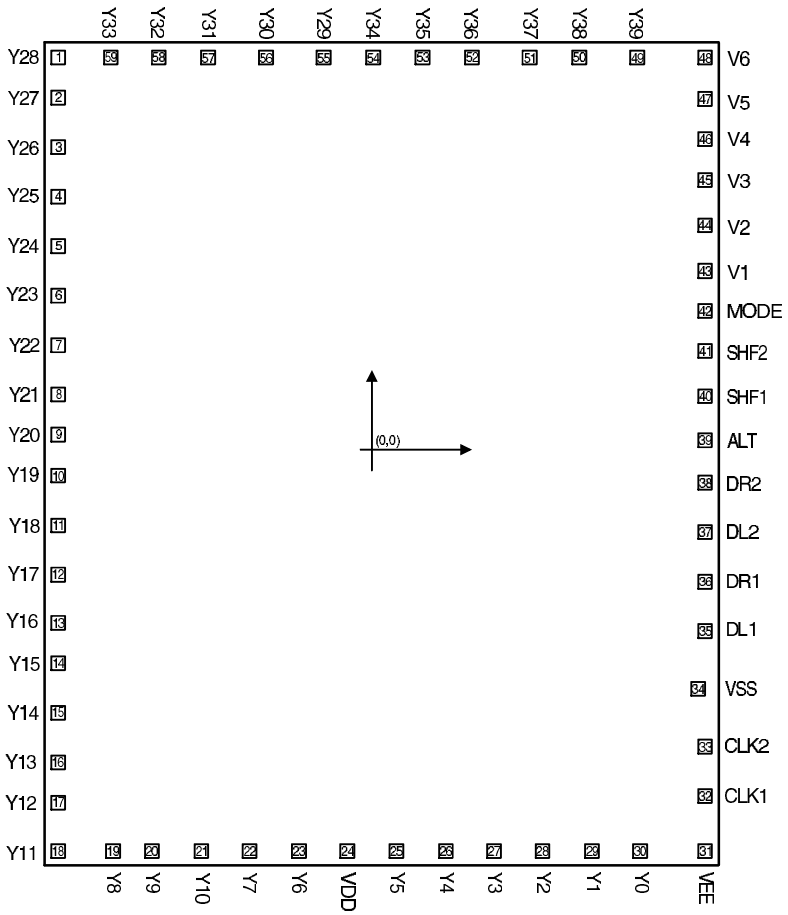
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 101×115 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	–44.54	51.94	31	44.12	–51.38
2	–44.54	45.86	32	44.12	–42.97
3	–44.54	39.78	33	44.12	–36.93
4	–44.54	33.70	34	42.33	–29.62
5	–44.54	27.63	35	44.12	–22.31
6	–44.54	21.55	36	44.12	–16.28
7	–44.54	15.47	37	44.12	–10.67
8	–44.54	9.39	38	44.12	–4.63
9	–44.54	3.32	39	44.12	0.98
10	–44.54	–2.76	40	44.12	7.01
11	–44.54	–8.84	41	44.12	12.62
12	–44.54	–14.92	42	44.12	18.66
13	–44.54	–21.00	43	44.12	24.31
14	–44.54	–27.07	44	44.12	29.83
15	–44.54	–33.15	45	44.12	35.36
16	–44.54	–39.23	46	44.12	40.88
17	–44.54	–45.31	47	44.12	46.41
18	–44.54	–51.38	48	44.12	51.94
19	–36.55	–51.38	49	31.28	51.94
20	–29.92	–51.38	50	24.74	51.94
21	–23.29	–51.38	51	18.19	51.94
22	–16.66	–51.38	52	11.65	51.94
23	–10.03	–51.38	53	5.10	51.94
24	–3.40	–51.38	54	–1.45	51.94
25	3.23	–51.38	55	–7.99	51.94
26	9.86	–51.38	56	–14.53	51.94
27	16.49	–51.38	57	–21.08	51.94
28	23.12	–51.38	58	–27.63	51.94
29	29.75	–51.38	59	–34.17	51.94
30	36.38	–51.38			

Pad Description

Pad No.	Pad Name	I/O	Description
1~9	Y28~Y20	O	LCD driver outputs for channel 2
10~23	Y19~Y6	O	LCD driver outputs for channel 1
24	VDD	—	Power supply (positive)
25~30	Y5~Y0	O	LCD driver outputs for channel 1
31	VEE	I	LCD power supply
32	CLK1	I	Latch signal for channel 1 on the falling edge CLK1 is used for channel 2 when MODE is set to V_{SS} (Note 1)

Pad No.	Pad Name	I/O	Description
33	CLK2	I	Shift signal for channel 1 on the falling edge and used for channel 2 when MODE is set to V_{SS} (Note 1)
34	VSS	—	Power supply (ground)
35	DL1	I/O	Data input/output of channel 1 shift register
36	DR1	I/O	Data input/output of channel 1 shift register
37	DL2	I/O	Data input/output of channel 2 shift register
38	DR2	I/O	Data input/output of channel 2 shift register
39	ALT	I	Alternate signal input for LCD driving waveform
40	SHF1	I	Shift direction selection of channel 1 shift register (Note 2)
41	SHF2	I	Shift direction selection of channel 2 shift register (Note 2)
42	MODE	I	Mode select signal of channel 2 (Note 3)
43, 44	V1, V2	I	LCD bias supply voltage for channels 1 and 2
45, 46	V3, V4	I	LCD bias supply voltage for channel 1
47, 48	V5, V6	I	LCD bias supply voltage for channel 2
49~59	Y39~Y29	O	LCD driver outputs for channel 2

		Channel 1	Channel 2
CLK1	↑	—	—
	↓	Latch data	Latch data
CLK2	↑	—	—
	↓	Shift data	Shift data

Note 1: Data is processed on the clock falling or rising edge as shown in the following table.

		Channel 1	Channel 2
CLK1	↑	—	Shift data
	↓	Latch data	—
CLK2	↑	—	Latch data
	↓	Shift data	—

MODE= L (V_{SS})
MODE= H (V_{DD})

Note 2 : Shift direction of channel 1 and 2

Shift Direction of Channel 1 (Channel 2)		
SHF1 (SHF2)	**DL1 (DL2)**	**DR1 (DR2)**
H	OUT	IN
L	IN	OUT

Note 3 :

MODE	Channel 2		ALT Polarity	Purpose
	Latch Data	Shift Data		
H	CLK2 ↑	CLK1 ↑	$\overline{ALT}$	for Common drive
L	CLK1 ↓	CLK2 ↓	ALT	for Segment drive

The output levels of channel 1 and 2 are decided by the combination of MODE, ALT and latched data. Refer to the following table:

MODE	Latched Data	ALT	Channel 1 (Y0~Y19)	Channel 2 (Y20~Y39)
H (V_{DD})	H	H	V1	V2
		L	V2	V1
	L	H	V3	V6
		L	V4	V5
L (V_{SS})	H	H	V1	V1
		L	V2	V2
	L	H	V3	V5
		L	V4	V6

Absolute Maximum Ratings*

Supply Voltage .....–0.3V to 5.5V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature.....–50°C to 125°C
Operating Temperature.....–20°C to 70°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

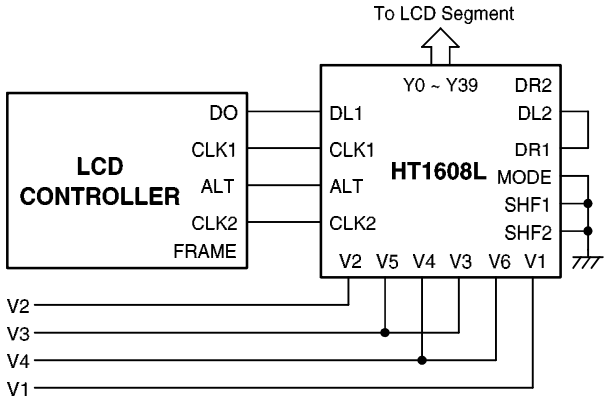
Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD}	Operating Current	5V	No load	—	100	300	μA
I_{STB}	Standby Current	5V	—	—	1	5	μA
f_{CLK2}	Data Shift Frequency	5V	—	—	—	400	kHz
tw_{CLK}	Clock Pulse Width	5V	—	800	—	—	ns
V_{IL}	"L" Input Voltage	5V	—	—	—	1	V
V_{IH}	"H" Input Voltage	5V	—	4	—	—	V
V_{OL}	"L" Output Voltage	5V	I_{OL}=+0.4mA	—	—	0.4	V
V_{OH}	"H" Output Voltage	5V	I_{OH}=–0.4mA	4.6	—	—	V
V_{LCD}	LCD Driving Voltage	—	V_{DD}–V_{EE}	3	—	5.0	V

Functional Description

Both channel 1 and 2 used as segment drivers (MODE=L)

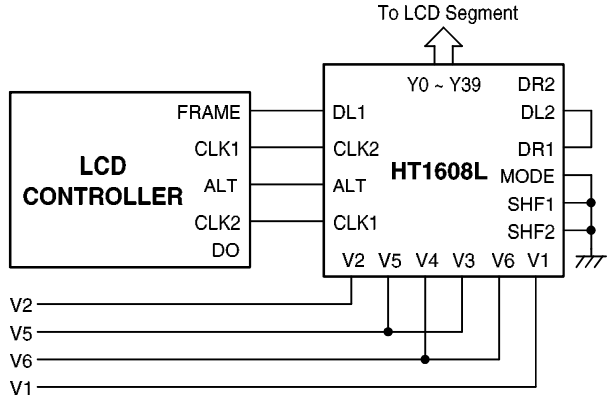
When both channel 1 and 2 of the HT1608L are used as segment drivers, they will shift data on the falling edge of CLK2 and shift latch data on the falling edge of CLK1. V3 and V5 or V4 and V6 are shortened in the application circuit as shown in the following figure.



Note: V1, V2: Selection levels for both segment and common application
V3, V4: Non-selection levels for segment application

Both channel 1 and 2 used as common drivers (MODE=L)

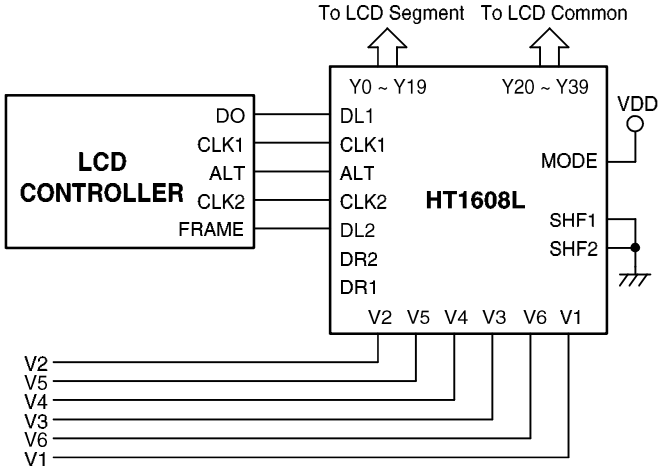
When both channel 1 and 2 of the HT1608L are used as common drivers, the MODE is set low and the signals (CLK1, CLK2, FRAME) from the controller are connected as shown in the following figure.



Note: V1, V2: Selection levels for both segment and common application
V5, V6: Non-selection levels for segment application

Channel 1 used as a segment driver and channel 2 as a common driver (MODE=H)

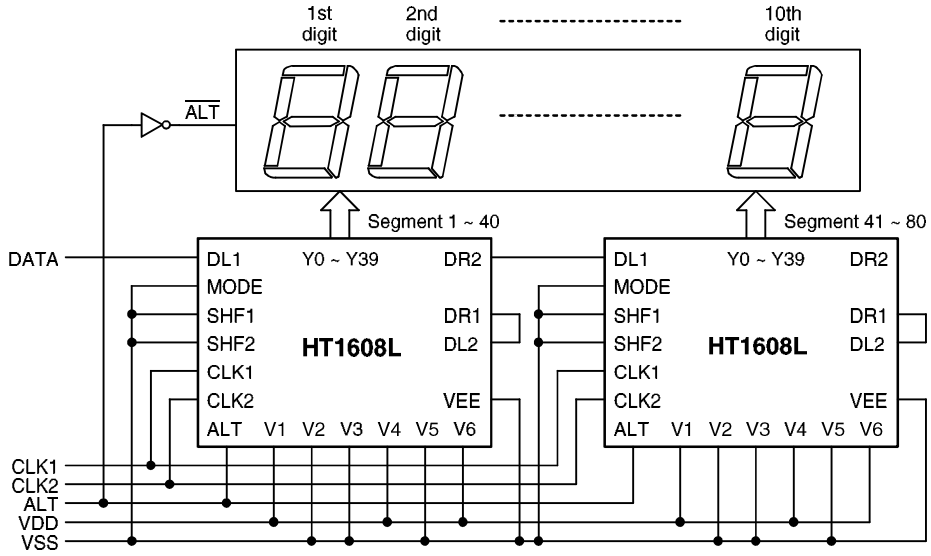
When channel 2 is used as a common driver, MODE is connected to VDD. Channel 2 will shift data on the rising edge of CLK1 and shift latch data on the rising edge of CLK2.



Static driver

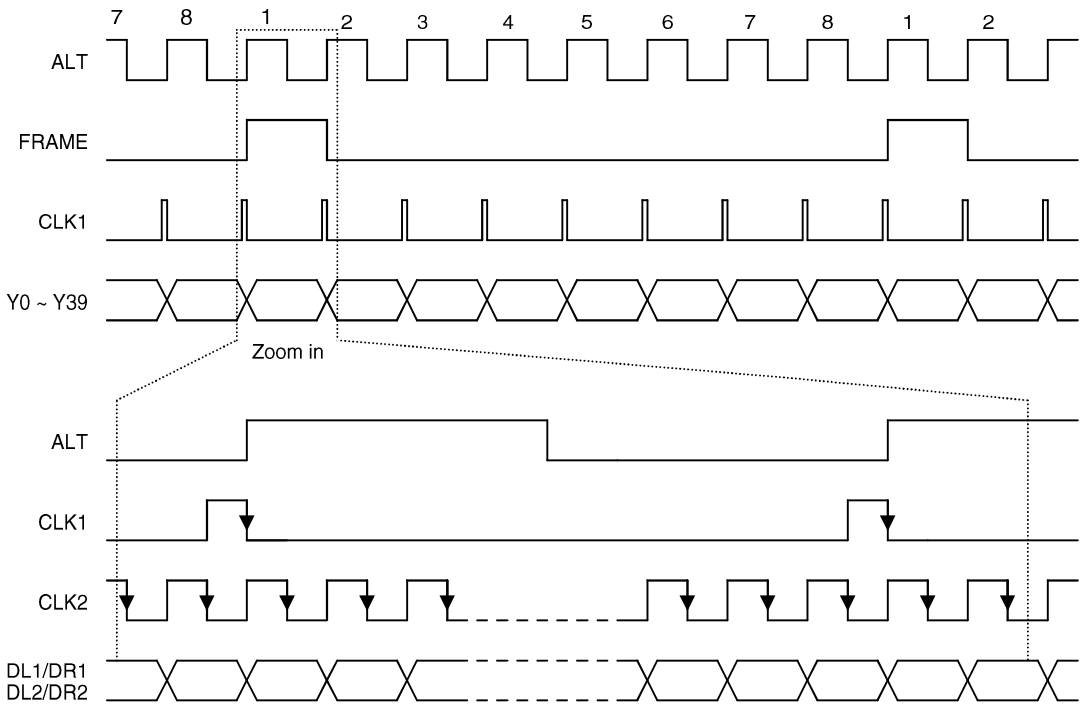
When the HT1608L is used as a static driver, data is transferred on the falling edge of CLK2 and latched on the falling edge of CLK1. The frequency of CLK1 becomes the frame frequency of the LCD driver. The frequency of ALT has to be twice the frequency of CLK1. ALT has to be synchronized on the falling edge of CLK1.

The power supply for the LCD driver is used by shortening V1, V4 and V6 or V2, V3 and V5. One of the LCD output terminals can be used as a common output. The application circuit connections are shown below:

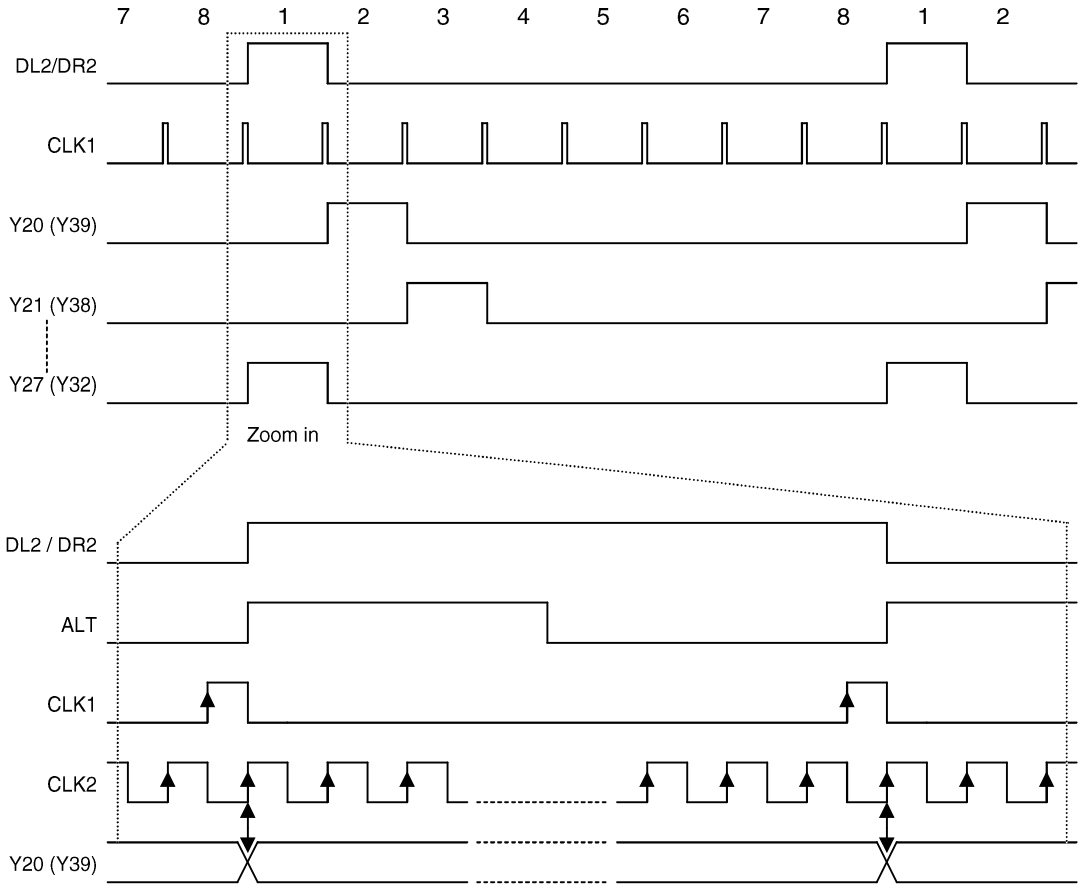


Timing Diagrams

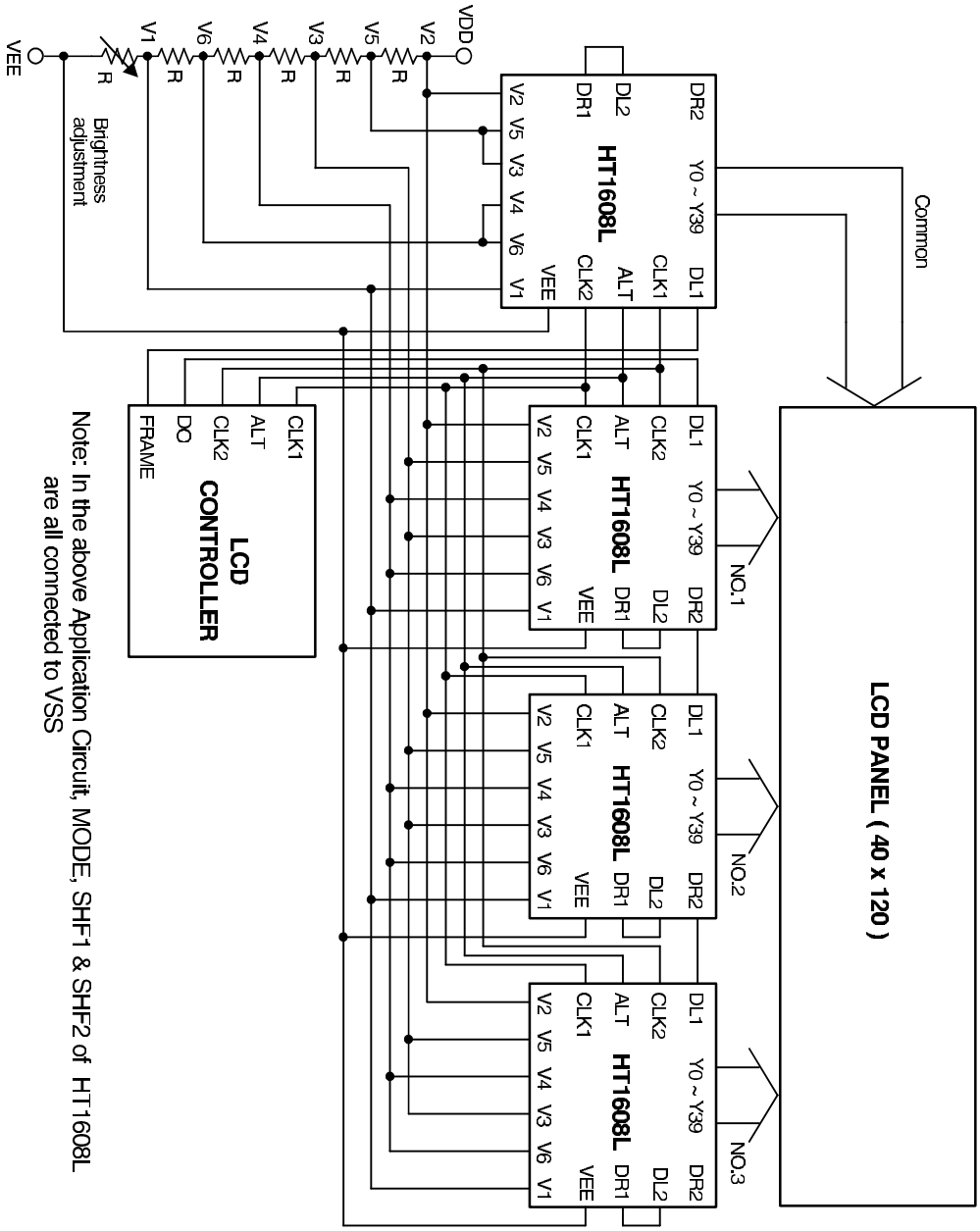
Segment data waveform (1/8 duty)



Common data waveform (a typical waveform of channel 2 as a COMMON driver, 1/8 duty)



Application Circuits



Note: In the above Application Circuit, MODE, SHF1 & SHF2 of HT1608L are all connected to VSS