

P-Channel 20-V (D-S) MOSFET

■ Features

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability

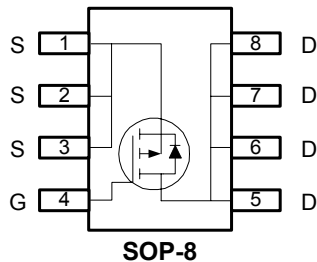
■ General Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWM DC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

■ Product Summary

V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
-20	8.4@ $V_{GS}=-4.5V$	-13.5
	10.4@ $V_{GS}=-2.5V$	-12

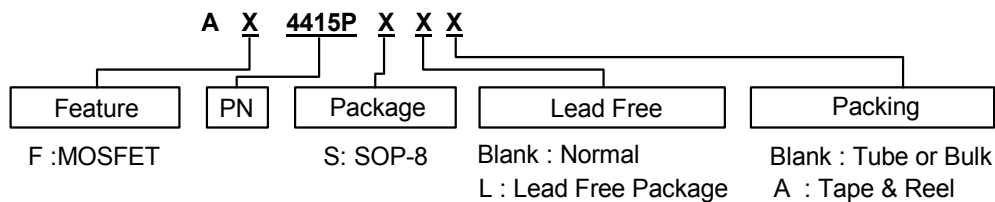
■ Pin Assignments



■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

■ Ordering information





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■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	-13.5
		$T_A=70^\circ\text{C}$	-11.6
I_{DM}	Pulsed Drain Current (Note 2)	± 50	A
I_S	Continuous Source Current (Diode Conduction) (Note 1)	-2.1	A
P_D	Power Dissipation (Note 1)	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2.3
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

■ Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JC}$	Maximum Junction-to-Case (Note 1)	25	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Junction-to-Ambient (Note 1)	50	$^\circ\text{C}/\text{W}$

Note 1: surface Mounted on 1"x 1" FR4 Board.

Note 2: Pulse width limited by maximum junction temperature

■ Specifications ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
$V_{(BR)DSS}$	Drain-Source breakdown Voltage	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-20	-	-	V
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-	-1.5	V
I_{GSS}	Gate-Body Leakage	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$	-	-	± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-16\text{V}, V_{GS}=0\text{V}$	-	-	-1	μA
		$V_{DS}=-16\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$	-	-	-5	
$I_{D(on)}$	On-State Drain Current (Note 3)	$V_{DS}=-4.5\text{V}, V_{GS}=-10\text{V}$	-50	-	-	A
$r_{DS(on)}$	Drain-Source On-Resistance (Note 3)	$V_{GS}=-4.5\text{V}, I_D=-13.5\text{A}$	-	6.7	8.4	m Ω
		$V_{GS}=-2.5\text{V}, I_D=-12\text{A}$	-	8.0	10.4	
		$V_{GS}=-4.5\text{V}, I_D=-13.5\text{A}, T_J=55^\circ\text{C}$	-	7.2	8.7	
g_{fs}	Forward Transconductance (Note 3)	$V_{GS}=-15\text{V}, I_D=-11.5\text{A}$	-	70	-	S
V_{SD}	Diode Forward Voltage	$I_S=2.5\text{A}, V_{GS}=0\text{V}$	-	-0.6	-1.2	V
Dynamic (Note 4)						
Q_g	Total Gate Charge	$V_{DS}=-10\text{V}, V_{GS}=-4.5\text{V}, I_D=-13.5\text{A}$	-	86	118	nC
Q_{gs}	Gate-Source Charge		-	20	-	
Q_{gd}	Gate-Drain Charge		-	11	-	
Switching						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10, R_L=6\Omega, I_D=-1\text{A}, V_{GEN}=-4.5\text{V}$	-	20	35	nS
t_r	Rise Time		-	23	36	
$t_{d(off)}$	Turn-Off Delay Time		-	289	456	
t_f	Fall-Time		-	134	218	

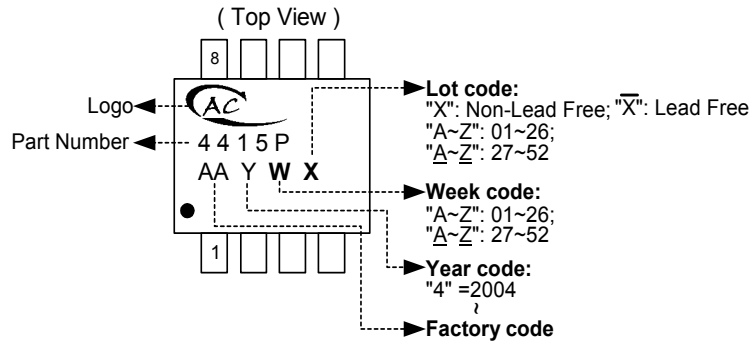
Note 3: Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.

Note 4: Guaranteed by design, not subject to production testing.

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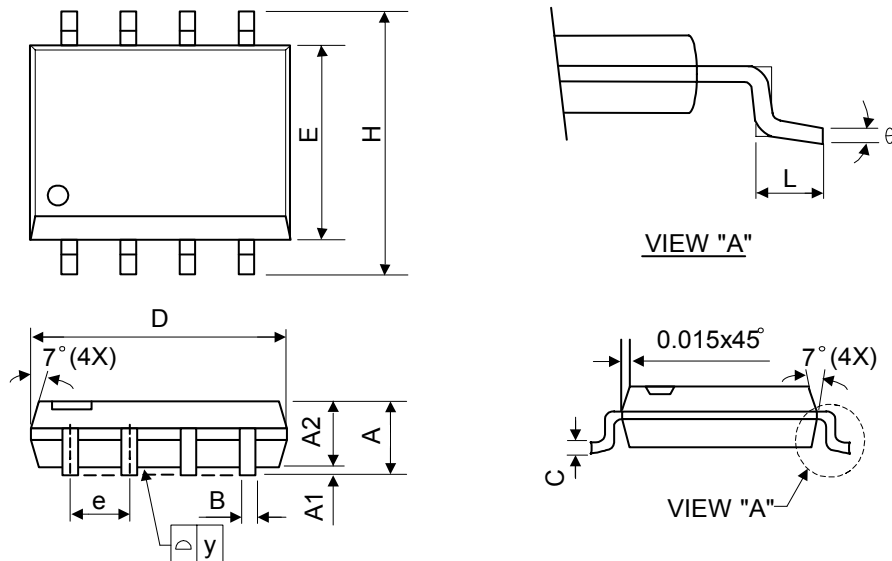
■ Marking Information

SOP-8L



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°