



# Preliminary

# 1M X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

# **Document Title**

1M X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

# **Revision History**

| Rev. No. | <u>History</u> | Issue Date      | <u>Remark</u> |
|----------|----------------|-----------------|---------------|
| 0.0      | Initial issue  | August 25, 2005 | Preliminary   |



# **Preliminary**

# 1M X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

#### **Features**

- Fast access times: 6.5/7.5/8.0 ns(153/133/117 MHz)
- Single 2.5V±5% power supply
- Synchronous burst function
- Individual Byte Write control and Global Write
- Three separate chip enables allow wide range of options for CE control, address pipelining

## **General Description**

The A63P06361 is a high-speed SRAM containing 36M bits of bit synchronous memory, organized as 1024K words by 36 bits.

The A63P06361 combines advanced synchronous peripheral circuitry, 2-bit burst control, input registers, output buffer and a 1M X 36 SRAM core to provide a wide range of data RAM applications.

The positive edge triggered single clock input (CLK) controls all synchronous inputs passing through the registers. Synchronous inputs include all addresses (A0 - A19), all data inputs (I/O<sub>1</sub> - I/O<sub>36</sub>), active LOW chip enable ( $\overline{\text{CE}}$ ), two additional chip enables (CE2,  $\overline{\text{CE2}}$ ), burst control inputs ( $\overline{\text{ADSC}}$ ,  $\overline{\text{ADSP}}$ ,  $\overline{\text{ADV}}$ ), byte write enables ( $\overline{\text{BWE}}$ ,  $\overline{\text{BW1}}$ ,  $\overline{\text{BW2}}$ ,  $\overline{\text{BW3}}$ ,  $\overline{\text{BW4}}$ ) and Global Write ( $\overline{\text{GW}}$ ). Asynchronous inputs include output enable ( $\overline{\text{OE}}$ ), clock (CLK), BURST mode (MODE) and SLEEP mode (ZZ).

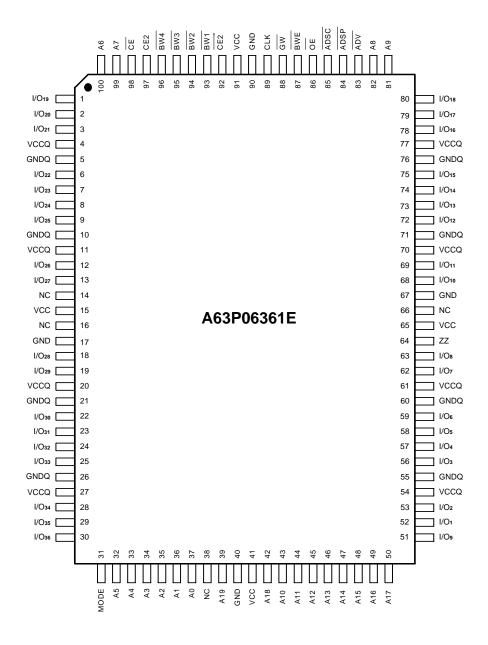
- Selectable BURST mode
- SLEEP mode (ZZ pin) provided
- Available in 100-pin LQFP package
- Industrial operating temperature range: -45°C to +125°C for -I series

Burst operations can be initiated with either the address status processor ( $\overline{\text{ADSP}}$ ) or address status controller ( $\overline{\text{ADSC}}$ ) input pin. Subsequent burst sequence burst addresses can be internally generated by the A63P06361 and controlled by the burst advance ( $\overline{\text{ADV}}$ ) pin. Write cycles are internally self-timed and synchronous with the rising edge of the clock (CLK).

This feature simplifies the write interface. Individual Byte enables allow individual bytes to be written.  $\overline{BW1}$  controls I/O1 - I/O9,  $\overline{BW2}$  controls I/O10 - I/O18,  $\overline{BW3}$  controls I/O19 - I/O27, and  $\overline{BW4}$  controls I/O28 - I/O36, all on the condition that  $\overline{BWE}$  is LOW.  $\overline{GW}$  LOW causes all bytes to be written.

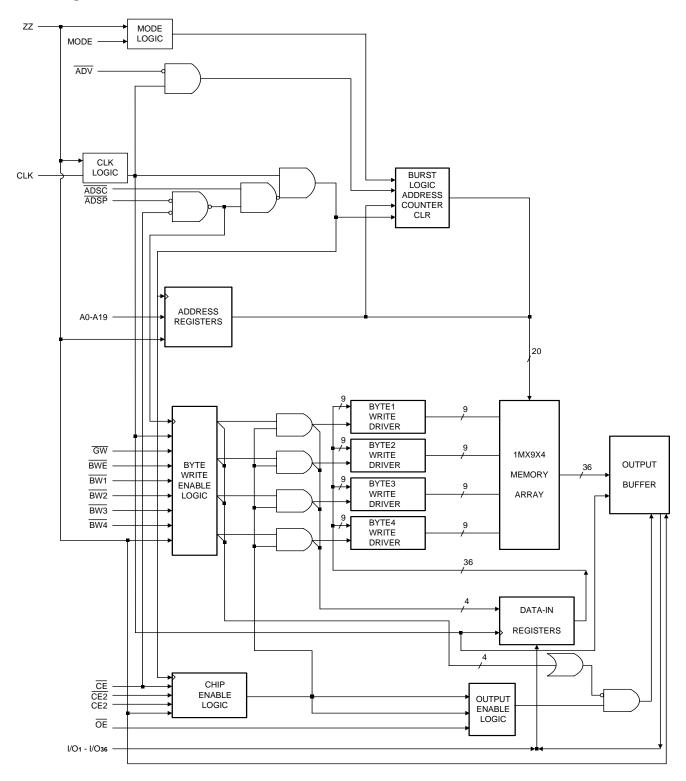


## **Pin Configuration**





## **Block Diagram**





# **Pin Description**

| Pin No.   | Symbol         | Description  |
|---|----------------|--|
| 32 – 37,39, 42 - 50, 81,<br>82, 99, 100   | A0 - A19       | Address Inputs   |
| 89  | CLK            | Clock  |
| 87, 93 - 96   | BWE, BW1 - BW4 | Byte Write Enables   |
| 88  | GW             | Global Write   |
| 86  | ŌĒ             | Output Enable  |
| 92, 97, 98  | CE2,CE2, CE    | Chip Enables   |
| 83  | ĀDV            | Burst Address Advance  |
| 84  | ADSP           | Processor Address Status   |
| 85  | ADSC           | Controller Address Status  |
| 31  | MODE           | Burst Mode: HIGH or NC (Interleaved burst) LOW (Linear burst)      |
| 64  | ZZ             | Asynchronous Power-Down (Snooze): HIGH (Sleep) LOW or NC (Wake up) |
| 1,2, 3, 6 - 9, 12, 13, 18,<br>19, 22 - 25, 28, 29,30,51,<br>52, 53,<br>56 - 59, 62, 63, 68, 69, 72<br>- 75, 78, 79,80 | I/O1- I/O36    | Data Inputs/Outputs  |
| 1, 14, 16, 30, 38, 39, 42,<br>43, 51, 66, 80  | NC             | No Connection  |
| 15, 41, 65, 91  | VCC            | Power Supply   |
| 17, 40, 67, 90  | GND            | Ground   |
| 4, 11, 20, 27,<br>54, 61, 70, 77  | VCCQ           | Isolated Output Buffer Supply                                      |
| 5, 10, 21, 26,<br>55, 60, 71, 76  | GNDQ           | Isolated Output Buffer Ground                                      |



# **Synchronous Truth Table (See Notes 1 Through 5)**

| Operation                                | Address  | <u></u> | CE2 | CE2 |      | ADSC | ADV | WRITE | <u></u> | CLK | I/O       |
|--|----------|---------|-----|-----|------|------|-----|-------|---------|-----|-----------|
| Operation                                | Used     | CE      |     |     | ADSP |      | ADV |       | OE      |     | Operation |
| Deselected Cycle,<br>Power-down          | NONE     | Η       | Х   | X   | X    | L    | Х   | Х     | Х       | L-H | High-Z    |
| Deselected Cycle,<br>Power-down          | NONE     | L       | Х   | L   | L    | Х    | X   | Х     | Х       | L-H | High-Z    |
| Deselected Cycle, Power-down             | NONE     | L       | Н   | Х   | L    | Х    | Х   | Х     | Х       | L-H | High-Z    |
| Deselected Cycle, Power-down             | NONE     | L       | Х   | L   | Н    | L    | Х   | Х     | Х       | L-H | High-Z    |
| Deselected Cycle,                        | NONE     | L       | Н   | Х   | Н    | L    | Х   | Х     | Х       | L-H | High-Z    |
| Power-down<br>READ Cycle,                | External | L       | L   | Н   | L    | Х    | X   | X     | L       | L-H | Dout      |
| Begin Burst<br>READ Cycle,               | External | L       | L   | Н   | L    | Х    | Х   | X     | Н       | L-H | High-Z    |
| Begin Burst<br>WRITE Cycle,              | External | L       | L   | Н   | Н    | L    | X   | L     | X       | L-H | Din       |
| Begin Burst READ Cycle,                  | External | L       | L   | Н   | Н    | L    | Х   | Н     | L       | L-H | Dout      |
| Begin Burst                              |          |         |     |     |      |      |     |       |         |     |           |
| READ Cycle,<br>Begin Burst               | External | L       | L   | Н   | Н    | L    | Х   | Н     | Н       | L-H | High-Z    |
| READ Cycle,<br>Continue Burst            | Next     | Х       | Х   | Х   | Н    | Н    | L   | Н     | L       | L-H | Dout      |
| READ Cycle,<br>Continue Burst            | Next     | Х       | Х   | Х   | Н    | Н    | L   | Н     | Н       | L-H | High-Z    |
| READ Cycle,<br>Continue Burst            | Next     | Н       | Х   | Х   | Х    | Н    | L   | Н     | L       | L-H | Dout      |
| READ Cycle,<br>Continue Burst            | Next     | Н       | Х   | Х   | Х    | Н    | L   | Н     | Н       | L-H | High-Z    |
| WRITE Cycle, Continue Burst              | Next     | Х       | Х   | Х   | Н    | Н    | L   | L     | Х       | L-H | Din       |
| WRITE Cycle, Continue Burst              | Next     | Н       | Х   | Х   | Х    | Н    | L   | L     | Х       | L-H | Din       |
| READ Cycle,                              | Current  | Х       | Х   | Х   | Н    | Н    | Н   | Н     | L       | L-H | Dout      |
| Suspend Burst READ Cycle,                | Current  | Х       | Х   | Х   | Н    | Н    | Н   | Н     | Н       | L-H | High-Z    |
| Suspend Burst READ Cycle,                | Current  | Н       | Х   | Х   | Х    | Н    | Н   | Н     | L       | L-H | Dout      |
| Suspend Burst READ Cycle,                | Current  | Н       | Х   | Х   | Х    | Н    | Н   | Н     | Н       | L-H | High-Z    |
| Suspend Burst WRITE Cycle,               | Current  | Х       | Х   | Х   | Н    | Н    | Н   | L     | Х       | L-H | Din       |
| Suspend Burst WRITE Cycle, Suspend Burst | Current  | Н       | Х   | Х   | X    | Н    | Н   | L     | Х       | L-H | Din       |



Notes: 1. X = "Disregard", H = Logic High, L = Logic Low.

- 2. WRITE = L means:
  - 1) Any  $\overline{BWx}$  ( $\overline{BW1}$ ,  $\overline{BW2}$ ,  $\overline{BW3}$ , or  $\overline{BW4}$ ) and  $\overline{BWE}$  are low or
  - 2) GW is low.
- 3. All inputs except  $\overline{\mathsf{OE}}$  must be synchronized with setup and hold times around the rising edge (L-H) of CLK.
- 4. For write cycles that follow read cycles,  $\overline{\text{OE}}$  must be HIGH before the input data request setup time and held HIGH throughout the input data hold time.
- 5. ADSP LOW always initiates an internal Read at the L-H edge of CLK. A Write is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. Refer to the Write timing diagram for clarification.

#### **Write Truth Table**

| Operation       | GW | BWE | BW1 | BW2 | BW3 | BW4 |
|-----------------|----|-----|-----|-----|-----|-----|
| READ            | Н  | Н   | Х   | Х   | Х   | Х   |
| READ            | Н  | L   | Н   | Н   | Н   | Н   |
| WRITE Byte 1    | Н  | L   | L   | Н   | Н   | Н   |
| WRITE all bytes | Н  | L   | L   | L   | L   | L   |
| WRITE all bytes | L  | Х   | Х   | Х   | Х   | Х   |



#### **Linear Burst Address Table (MODE = LOW)**

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X X00                    | X X01                     | X X10                    | X X11                     |
| X X01                    | X X10                     | X X11                    | X X00                     |
| X X10                    | X X11                     | X X00                    | X X01                     |
| X X11                    | X X00                     | X X01                    | X X10                     |

## Interleaved Burst Address Table (MODE = HIGH or NC)

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X X00                    | X X01                     | X X10                    | X X11                     |
| X X01                    | X X00                     | X X11                    | X X10                     |
| X X10                    | X X11                     | X X00                    | X X01                     |
| X X11                    | X X10                     | X X01                    | X X00                     |

## **Absolute Maximum Ratings\***

| Power Supply Voltage (VCC)          | 0.5V to +3.6V    |
|-------------------------------------|------------------|
| Voltage Relative to GND for any Pir | Except VCC (Vin, |
| Vout)0                              | .5V to VCC +0.5V |
| Power Dissipation (PD)              | 2W               |
| Storage Temperature (Tbias)         | 65°C to 150 °C   |
| Storage Temperature (Tstg)          | 55°C to 125°C    |

#### **Operating Ranges**

#### **Ambient Temperature**

| Commercial (C) Devices | 0°C to +70°C    |
|------------------------|-----------------|
| Industrial (I) Devices | -45°C to +125°C |

#### Vcc & Vccq Supply Voltages

| Vcc for all devices                          | . +2.5V   |
|--|-----------|
| Vccq for all devices                         | . +2.5V   |
| Operating ranges define those limits between | which the |
| functionally of the device is guaranteed.    |           |

#### \*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

## **Recommended DC Operating Conditions**

 $(0^{\circ}C \le T_A \le 70^{\circ}C, \ VCC, \ VCCQ = 2.5V+5\% \ or \ 2.5V-5\%, \ unless \ otherwise \ noted)$ 

| Symbol | Parameter                                | Min.  | Тур. | Max.    | Unit | Note |
|--------|--|-------|------|---------|------|------|
| VCC    | Supply Voltage (Operating Voltage Range) | 2.375 | 2.5  | 2.625   | V    |      |
| VCCQ   | Isolated Input Buffer Supply             | 2.375 | 2.5  | 2.625   | V    |      |
| GND    | Supply Voltage to GND                    | 0.0   | -    | 0.0     | V    |      |
| Vih    | Input High Voltage                       | 1.7   | -    | VCC+0.3 | V    | 1, 2 |
| Vінq   | Input High Voltage (I/O Pins)            | 1.7   | -    | VCC+0.3 | V    |      |
| VIL    | Input Low Voltage                        | -0.3  | -    | 0.7     | V    | 1, 2 |



## **DC Electrical Characteristics**

(0°C  $\leq$  Ta  $\leq$  70°C, VCC, VCCQ = 2.5V+5% or 2.5V-5%, unless otherwise noted)

| Symbol | Parameter              | Min. | Max. | Unit | Test Conditions   | Note  |
|--------|------------------------|------|------|------|---|-------|
| [[]    | Input Leakage Current  | -    | ±2.0 | μΑ   | All inputs Vin = GND to VCC   |       |
| ILO    | Output Leakage Current | -    | ±2.0 | μΑ   | OE = ViH, Vout = GND to VCC   |       |
| lcc1   | Supply Current         | -    | 300  | mA   | Device selected; VCC = max.<br>lout = 0mA, all inputs = VIH or VIL<br>Cycle time = tкс min.                       | 3, 11 |
| ISB1   | Standby Current        | -    | 180  | mA   | Device deselected; VCC = max. All inputs are fixed. All inputs ≥ VCC - 0.2V or ≤ GND + 0.2V Cycle time = tκc min. | 11    |
| ISB2   |                        | -    | 150  | mA   | ZZ ≥ VCC - 0.2V   |       |
| Vol    | Output Low Voltage     | -    | 1.0  | V    | loL = 8 mA  |       |
| Voн    | Output High Voltage    | 1.6  | -    | V    | Іон = -4 mA   |       |

## Capacitance

| Symbol | Parameter                | Тур. | Max. | Unit | Conditions          |
|--------|--------------------------|------|------|------|---------------------|
| Cin    | Input Capacitance        | 3    | 4    | pF   | Ta = 25 C; f = 1MHz |
| Ci/o   | Input/Output Capacitance | 4    | 5    | pF   | VCC = 2.5V          |

<sup>\*</sup> These parameters are sampled and not 100% tested.



# AC Characteristics $(0^{\circ}C \le T_A \le 70^{\circ}C, \ VCC = 2.5V+5\% \ or \ 2.5V-5\%)$

| Symbol    | Parameter   | -6.5 |      | -7.5 |      | -8.5 |      | Unit | Note |
|-----------|---|------|------|------|------|------|------|------|------|
|           |   | Min. | Max. | Min. | Max. | Min. | Max. |      |      |
| Ткс       | Clock Cycle Time  | 7.5  | -    | 8.5  | -    | 10   | -    | ns   |      |
| Ткн       | Clock High Time   | 2.5  | -    | 2.8  | -    | 3.0  | -    | ns   |      |
| TĸL       | Clock Low Time  | 2.5  | -    | 2.8  | -    | 3.0  | -    | ns   |      |
| Тко       | Clock to Output Valid   | -    | 6.5  | -    | 7.5  | -    | 8.5  | ns   |      |
| tĸqx      | Clock to Output Invalid   | 3.0  | -    | 3.0  | -    | 3.0  | -    | ns   |      |
| tkqlz     | Clock to Output in Low-Z  | 2.5  | -    | 2.5  | -    | 2.5  | -    | ns   | 5, 6 |
| tконz     | Clock to Output in High-Z   | -    | 3.5  | -    | 3.5  | -    | 5.0  | ns   | 5, 6 |
| toeq      | OE to Output Valid  | -    | 3.5  | -    | 3.5  | -    | 5.0  | ns   | 8    |
| toelz     | OE to Output in Low-Z   | 0    | -    | 0    | -    | 0    | -    | ns   | 5, 6 |
| toehz     | OE to Output in High-Z  | -    | 3.5  | -    | 3.5  | -    | 5.0  | ns   | 5, 6 |
| Setup Tim | Setup Times   |      |      |      |      |      |      |      |      |
| Tas       | Address   | 1.5  | -    | 2.0  | -    | 2.0  | -    | ns   | 7, 9 |
| tadss     | Address Status ( ADSC , ADSP )  | 1.5  | -    | 2.0  | -    | 2.0  | -    | ns   | 7, 9 |
| tadvs     | Address Advance ( ADV )   | 1.5  | -    | 2.0  | -    | 2.0  | -    | ns   | 7, 9 |
| tws       | Write Signals (BW1, BW2, BW3, BW4, BWE, GW)                           | 1.5  | -    | 2.0  | -    | 2.0  | -    | ns   | 7, 9 |
| Tos       | Data-in   | 1.5  | -    | 1.5  | -    | 2.0  | -    | ns   | 7, 9 |
| tces      | Chip Enable ( $\overline{\text{CE}}$ , CE2, $\overline{\text{CE2}}$ ) | 1.5  | -    | 2.0  | -    | 2.0  | -    | ns   | 7, 9 |
| Hold Time | es  |      |      |      |      | •    |      |      |      |
| Тан       | Address   | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |
| tadsh     | Address Status ( ADSC , ADSP )  | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |
| tаан      | Address Advance ( ADV )   | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |
| twн       | Write Signal (BW1, BW2, BW3, BW4, BWE, GW)                            | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |
| Тон       | Data-in   | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |
| tсен      | Chip Enable ( $\overline{\text{CE}}$ , CE2, $\overline{\text{CE2}}$ ) | 0.5  |      | 0.5  |      | 0.5  |      | ns   | 7, 9 |



#### Notes:

1. All voltages refer to GND.

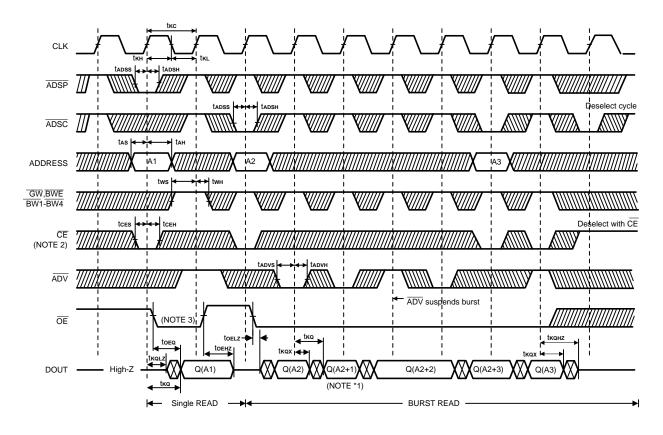
2. Overshoot:  $VIH \le +2V$  for  $t \le t\kappa c/2$ . Undershoot:  $VIL \ge -0.7V$  for  $t \le t\kappa c/2$ . Power-up:  $VIH \le +2$  and  $VCC \le 1.7V$ 

for  $t \le 200 \text{ms}$ 

- 3. Icc1 is given with no output current. Icc1 increases with greater output loading and faster cycle times.
- 4. Test conditions assume the output loading shown in Figure 1, unless otherwise specified.
- 5. For output loading, C<sub>L</sub> = 5pF, as shown in Figure 2. Transition is measured ±150mV from steady state voltage.
- 6. At any given temperature and voltage condition, tконz is less than tкоLz and toeнz is less than tqeLz.
- 7. A WRITE cycle is defined by at least one Byte Write enable LOW and ADSP HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and (ADSC or ADV LOW) or ADSP LOW for the required setup and hold times.
- 8. OE has no effect when a Byte Write enable is sampled LOW.
- 9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP or ADSC is LOW and the chip is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP or ADSC is LOW to remain enabled.
- 10. The load used for Voн, VoL testing is shown in Figure 2. AC load current is higher than the given DC values. AC I/O curves are available upon request.
- 11. "Device Deselected" means device is in POWER-DOWN mode, as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
- 12. MODE pin has an internal pulled-up, and ZZ pin has an internal pulled-down. All of then exhibit an input leakage current of  $10\mu$ A.
- 13. Snooze (ZZ) input is recommended that users plan for four clock cycles to go into SLEEP mode and four clocks to emerge from SLEEP mode to ensure no data is lost.



#### **Timing Waveforms**





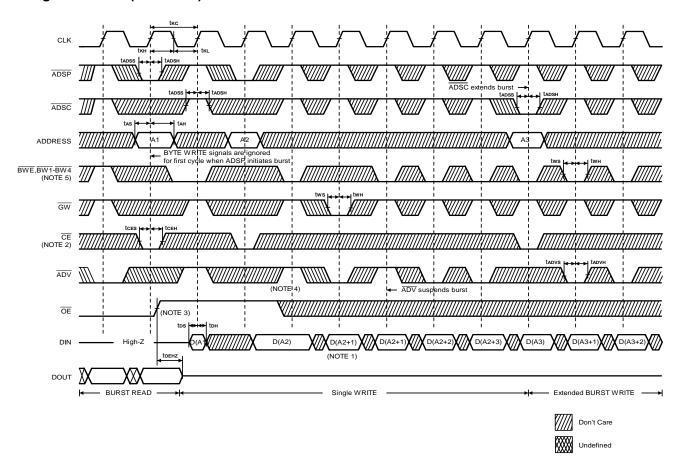
#### **Read Timing**

Notes: 1. QA(2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

- 2.  $\overline{\text{CE}}$  and CE2 have timing identical to  $\overline{\text{CE}}$ . On this diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE2}}$  is LOW and CE2 is HIGH. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE2}}$  is HIGH and CE2 is LOW.
- 3. Timing is shown assuming that the device was not enabled before entering into this sequence.  $\overline{\text{OE}}$  does not cause Q to be driven until after the following clock rising edge.



#### **Timing Waveforms (continued)**



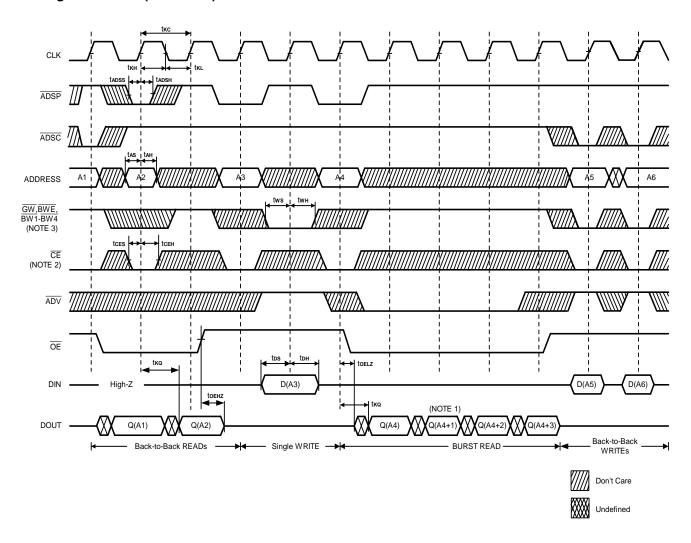
## **Write Timing**

Notes: 1. D(A2) refers to output from address A2. D(A2+1) refers to output from the internal burst address immediately following A2.

- 2. Timing for  $\overline{\text{CE2}}$  and  $\overline{\text{CE2}}$  is identical to that for  $\overline{\text{CE}}$ . As shown in the above diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE2}}$  is LOW and CE2 is HIGH. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE2}}$  is HIGH and CE2 is LOW.
- 3.  $\overline{\text{OE}}$  must be HIGH before the input data setup, and held HIGH throughout the data hold period. This prevents input/output data contention for the period prior to the time Byte Write enable inputs are sampled.
- 4. ADV must be HIGH to permit a Write to the loaded address.
- 5. Byte Write enables are decided by means of a Write truth table.



#### **Timing Waveforms (continued)**



#### **Read/Write Timing**

Notes: 1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.

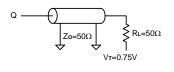
- 2.  $\overline{\text{CE2}}$  and  $\overline{\text{CE2}}$  have timing identical to  $\overline{\text{CE}}$ . On this diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE}}$  is LOW and CE2 is HIGH, When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE2}}$  is HIGH and CE2 is LOW.
- 3. The data bus (Q) remains in High-Z following a WRITE cycle unless an  $\overline{ADSP}$ ,  $\overline{ADSC}$ , or  $\overline{ADV}$  cycle is performed.
- 4. Byte Write enables are decided by means of a Write truth table.
- 5. Back-to-back READs may be controlled by either ADSP or ADSC



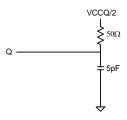
## **AC Test Conditions**

| Input Pulse Levels            | GND to 3V           |  |  |  |
|-------------------------------|---------------------|--|--|--|
| Input Rise and Fall Times     | 1 ns                |  |  |  |
| Input Timing Reference Levels | 1.5V                |  |  |  |
| Output Reference Levels       | VccQ/2              |  |  |  |
| Output Load                   | See Figures 1 and 2 |  |  |  |

Figure 1. Output Load Equivalent Figure



## 2. Output Load Equivalent



# **Ordering Information**

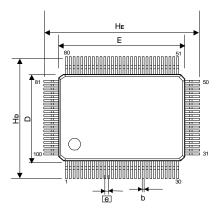
| Part No.        | Access Times (ns) | Frequency (MHz) | Package           |  |
|-----------------|-------------------|-----------------|-------------------|--|
| A63P06361E-6.5  | 6.5               | 153             | 100L LQFP         |  |
| A63P06361E-6.5F | 6.5               | 153             | 100L Pb-Free LQFP |  |
| A63P06361E-7.5  | 7.5               | 133             | 100L LQFP         |  |
| A63P06361E-7.5F | 7.5               | 133             | 100L Pb-Free LQFP |  |
| A63P06361E-8    | 8                 | 117             | 100L LQFP         |  |
| A63P06361E-8F   | 8                 | 117             | 100L Pb-Free LQFP |  |

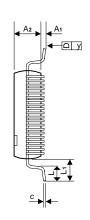


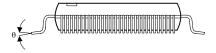
## **Package Information**

## **LQFP 100L Outline Dimensions**

unit: inches/mm







| Symbol | Dimensions in inches |       |       | Dimensions in mm |       |       |  |
|--------|----------------------|-------|-------|------------------|-------|-------|--|
|        | Min.                 | Nom.  | Max.  | Min.             | Nom.  | Max.  |  |
| A1     | 0.002                | -     | -     | 0.05             | -     | -     |  |
| A2     | 0.053                | 0.055 | 0.057 | 1.35             | 1.40  | 1.45  |  |
| b      | 0.011                | 0.013 | 0.015 | 0.27             | 0.32  | 0.37  |  |
| С      | 0.005                | -     | 0.008 | 0.12             | -     | 0.20  |  |
| HE     | 0.860                | 0.866 | 0.872 | 23.35            | 22.00 | 22.15 |  |
| E      | 0.783                | 0.787 | 0.791 | 19.90            | 20.00 | 20.10 |  |
| Hp     | 0.624                | 0.630 | 0.636 | 15.85            | 16.00 | 16.15 |  |
| D      | 0.547                | 0.551 | 0.555 | 13.90 14.00      |       | 14.10 |  |
| е      | 0.026 BSC            |       |       | 0.65 BSC         |       |       |  |
| L      | 0.018                | 0.024 | 0.030 | 0.45             | 0.60  | 0.75  |  |
| L1     | 0.039 REF            |       |       | 1.00 REF         |       |       |  |
| у      | -                    | -     | 0.004 | -                | -     | 0.1   |  |
| θ      | 0°                   | 3.5°  | 7°    | 0°               | 3.5°  | 7°    |  |

#### Notes:

- 1. Dimensions D and E do not include mold protrusion.
- Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.