ANADIGICS

AIT1042

Integrated Digital Tuner
with RF and IF Gain Control

PRELIMINARY DATA SHEET - Rev 1.0

FEATURES

- Complete Integrated RF Tuner: Includes Upconverter with RF Gain Control, Downconverter, Digital IF Amplifier with Gain Control, Dual PLL, and VCOs with integrated tanks
- IF Output - 35 to 50 MHz
- 54 to 1002 MHz Operation
- Operates from a Single +5 V Supply
- Integrated Oscillator Tank Circuits
- 78 dB Gain (including external filter losses) through Digital Output
- 35 dB RF Gain Control Range
- 45 dB IF Gain Control Range
- 2-Wire Serial Programming with 4 Addresses for Multiple Tuner Applications
- Programmable Power-Down Mode
- Programmable Charge Pump Currents
- Materials set consistent with RoHS directives

APPLICATIONS

- CATV Tuners
- HDTV Tuners
- Set-Top Boxes
- PC TV Tuner Cards or Tuner-on-Board

S38 Package
48 Pin QFN
7 mm x 7 mm x 1 mm

PRODUCT DESCRIPTION

The AIT1042 Integrated Digital Tuner with RF and IF Gain Control is a complete 1 GHz bandwidth tuner IC specifically designed to support digital video and data applications. It combines GaAs and Silicon technology to integrate the upconverter, downconverter, VCO, synthesizer, IF amplifier, RF gain control and IF gain control functions of a double-conversion tuner into one small package.

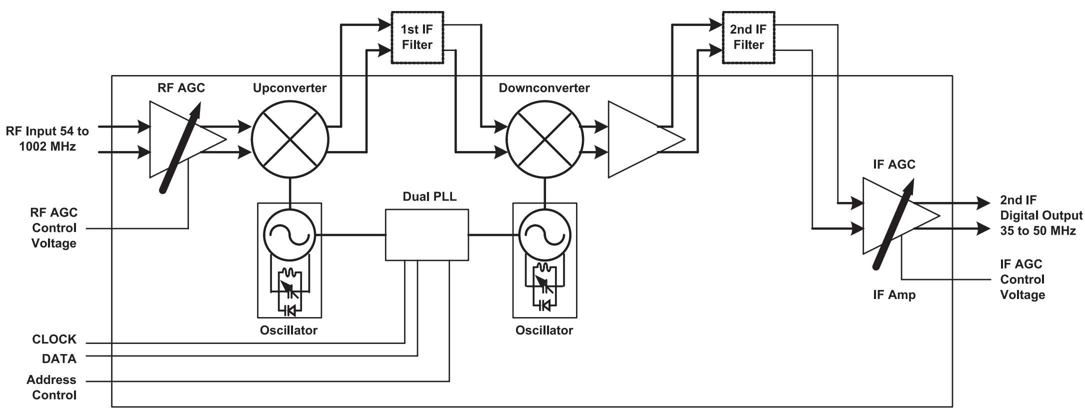


Figure 1: Functional Block Diagram

The exceptional linearity and low noise figure of the AIT1042 are ideal for use with today's CATV systems with densely loaded spectrum. With integrated oscillator tank circuits, the AIT1042's high level of integration minimizes board layout sensitivities and the amount of external circuitry required for a complete receiver solution. The integrated IF output further enables system solutions that minimize board layout space.

The device operates from a single +5 V supply, and incorporates a programmable power-down mode.

The AIT1042 is offered in a small 7 mm x 7 mm x1 mm, 48 pin, RoHS compliant, surface mount package ideal for space-sensitive applications such as PC cards and multiple-tuner set-top boxes.

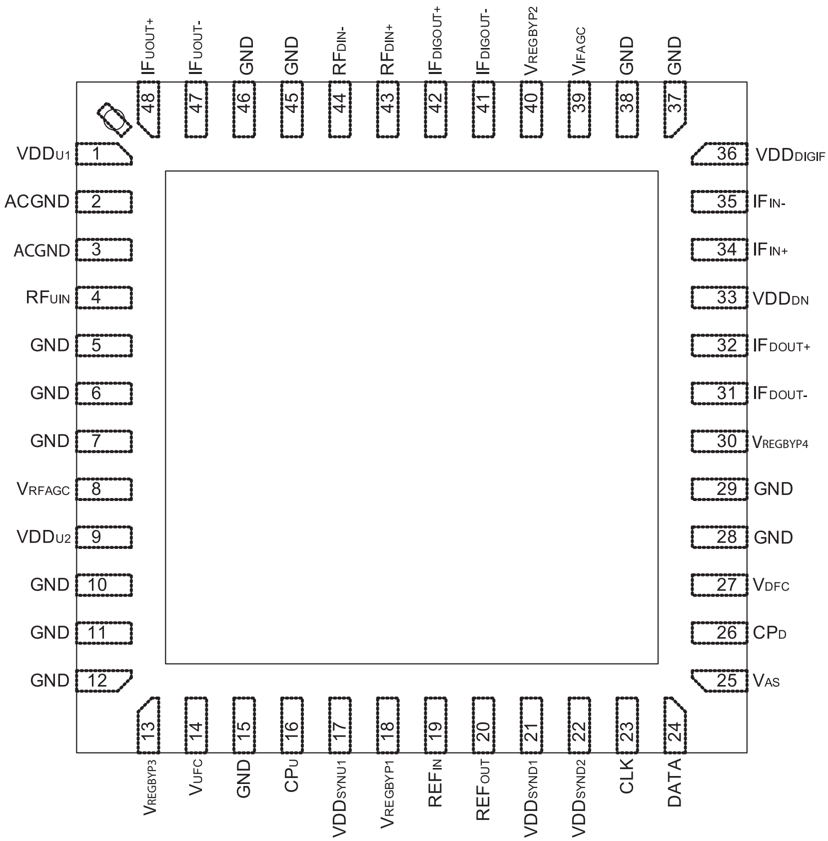


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	VDD_{U1}	Upconverter Supply	48	IF_{OUT+}	Upconverter Differential IF Output (Input to 1st IF Filter)
2	ACGND	AC Ground	47	IF_{OUT-}	Upconverter Differential IFOutput (Input to 1st IF Filter)
3	ACGND	AC Ground	46	GND	Ground
4	RF_{UIN}	Upconverter RF Input	45	GND	Ground
5	GND	Ground	44	RF_{DN-}	Downconverter Diff. RF Input
6	GND	Ground	43	RF_{DN+}	Downconverter Diff. RF Input
7	GND	Ground	42	$IF_{DIGOUT+}$	Digital IF Differential Output
8	V_{RFAGC}	RF Gain Control Voltage	41	$IF_{DIGOUT-}$	Digital IF Differential Output
9	VDD_{U2}	Upconverter Supply	40	$V_{REGBYP2}$	Regulator Bypass
10	GND	Ground	39	V_{IFAGC}	IF Gain Control Voltage
11	GND	Ground	38	GND	Ground
12	GND	Ground	37	GND	Ground
13	$V_{REGBYP3}$	Regulator Bypass	36	VDD_{DIGIF}	Digital IFAMP Supply
14	V_{UFC}	Upconverter Oscillator Frequency Control Voltage	35	IF_{IN-}	IF Amplifier Differential Input
15	GND	Ground	34	IF_{IN+}	IF Amplifier Differential Input
16	CP_{U}	Upconverter Synthesizer Charge Pump Output	33	VDD_{DN}	Downconverter Supply
17	VDD_{SYNU1}	Upconverter Synthesizer Supply	32	IF_{DOUT+}	Downconverter Differential IF Output (Input to 2nd IF Filter) Inductively Coupled to VDD
18	$V_{REGBYP1}$	Regulator Bypass	31	IF_{DOUT-}	Downconverter Differential IF Output (Input to 2nd IF Filter) Inductively Coupled to VDD
19	REF_{IN}	Crystal Reference Input	30	$V_{REGBYP4}$	Regulator Bypass
20	REF_{OUT}	Crystal Reference Output	29	GND	Ground
21	VDD_{SYND1}	Downconverter Synthesizer Supply	28	GND	Ground
22	VDD_{SYND2}	Downconverter Synthesizer Supply	27	V_{DFC}	Downconv. Oscillator Frequency Control Voltage
23	CLK	2-Wire Interface CLK	26	CP_{D}	Downconverter Synthesizer Charge Pump Output
24	DATA	2-Wire Interface Data	25	V_{AS}	2-Wire Interface Address Select Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT	COMMENTS
Supply Voltage (VCC)	0	+6	V	
RF Gain Control Voltage (V_{RFAGC})	0	+6	V	
IF Gain Control Voltage (V_{IFAGC})	0	+6	V	
RF Input Power	-	+60	dBmV	at RF_{UIN} and RF_{DIN}
Electrostatic Discharge (Human Body Model)	-	250	V	Class 1A
Storage Temperature	-55	+150	°C	

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Supply Voltage (VCC)	4.75	5.00	5.25	V
RF Gain Control Voltage (V_{RFAGC})	0	-	+3	V
IF Gain Control Voltage (V_{IFAGC})	0	-	+3	V
Upconverter RF Input Center Frequency (f_{RF})	54	-	1002	MHz
First IF Center Frequency (f_{IF1})	1680	1690	1700	MHz
IF Output Center Frequency (f_{IF2})	35	45	50	MHz
Case Temperature	0	-	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: DC Electrical Specifications
(T_C = +55 °C, VDD = +5.0 V)

PARAMETER	MIN	TYP	MAX	UNIT
RF Gain Control Current	-	100	-	μA
IF Gain Control Current	-	100	-	μA
Total Supply Current	-	320	-	mA
Total Power Consumption	-	1600	-	mW
Standby Current	-	125	-	mA

Table 5: AC Electrical Specifications
(T_C = +55 °C, VDD = +5.0 V, f_{IF1} = 1690 MHz, f_{IF2} = 45.75 MHz)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Conversion Gain (2), (3), (4)	-	78	-	dB	IF Output (pins 41 & 42)
Channel Flatness	-	±0.5	-	dB	6 MHz Bandwidth
SSB Noise Figure	-	8	-	dB	Measured at max gain
Input Return Loss	3	-	-	dB	75 Ω Impedance without match
Composite LO Phase Noise	-	-85	-	dBc/Hz	10 kHz Offset
RF Gain Control Range	-	40	-	dB	max gain at V_{RFAGC} = +3 V min gain at V_{RFAGC} = +0.5 V
Digital IF Gain Control Range	-	45	-	dB	max gain at V_{IFAGC} = +3 V min gain at V_{IFAGC} = +0.5 V
Final IF Output Voltage (4)	-	1000	-	mV_{P-P}	IF Output (pins 41 & 42)
CSO	-	-55	-	dBc	129 Channels, +3 dBmV each
CTB	-	-63	-	dBc	129 Channels, +3 dBmV each
XMOD	-	-57	-	dBc	129 Channels, +3 dBmV each 15.75 kHz AM-modulated
Power Supply Rejection to 1 MHz	20	-	-	dB	

Notes:
1. All specifications as measured in ANADIGICS test fixture with a 1st IF filter loss of 4 dB and a 2nd IF filter loss of 15 dB.
(2) At maximum RF and IF AGC gain settings, where applicable.
(3) Including nominal 1st and 2nd IF filter losses of 4 dB and 15 dB, respectively.
(4) IF output measured with a 1 kΩ differential load across pins 41 and 42.

Table 6: Digital 2-Wire Interface Specifications
(T_C = +55 °C, VDD = +5.0 V, ref. Figure 3)

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLK Frequency	f_{CLK}	1	400	kHz
Logic High Input (pins 23, 24)	V_H	2.0	-	V
Logic Low Input (pins 23, 24)	V_L	-	0.8	V
Logic Input Current Consumption (pins 23, 24)	I_{LOG}	-	10	μA
Address Select Input Current Consumtion (pin 25)	I_{AS}	-	10	μA
Data Sink Current (2)	I_{AK}	-	4.0	mA
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	μs
Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	-	μs
LOW period of CLK	t_{LOW}	1.3	-	μs
HIGH period of CLK	t_{HIGH}	0.6	-	μs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	μs
Data Hold Time (for 2-wire bus devices)	$t_{HD;DAT}$	0.0	0.9	μs
Data Set-up Time	$t_{SU;DAT}$	100	-	ns
Rise Time of DATA and CLK signals	t_R	$20 + 0.1C_b$ (1)	300	ns
Fall Time of Data and CLK signals	t_F	$20 + 0.1C_b$ (1)	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	-	μs
Capacitive Load for Each Bus Line	C_b	-	400	pF

Notes:
(1) Cb is the total capacitance of one bus line in pF.
(2) For maximum 0.8 V level during Acknowledge Pulse.
3. All timing values are referred to minimum V_H and maximum V_L levels.

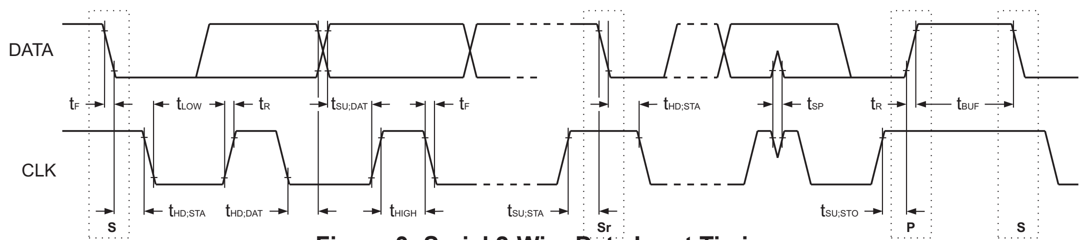


Figure 3: Serial 2-Wire Data Input Timing

Figure 4: CSO vs. Frequency
(+3dBmV input power, 129 channels - flat, Tc = +55°C)

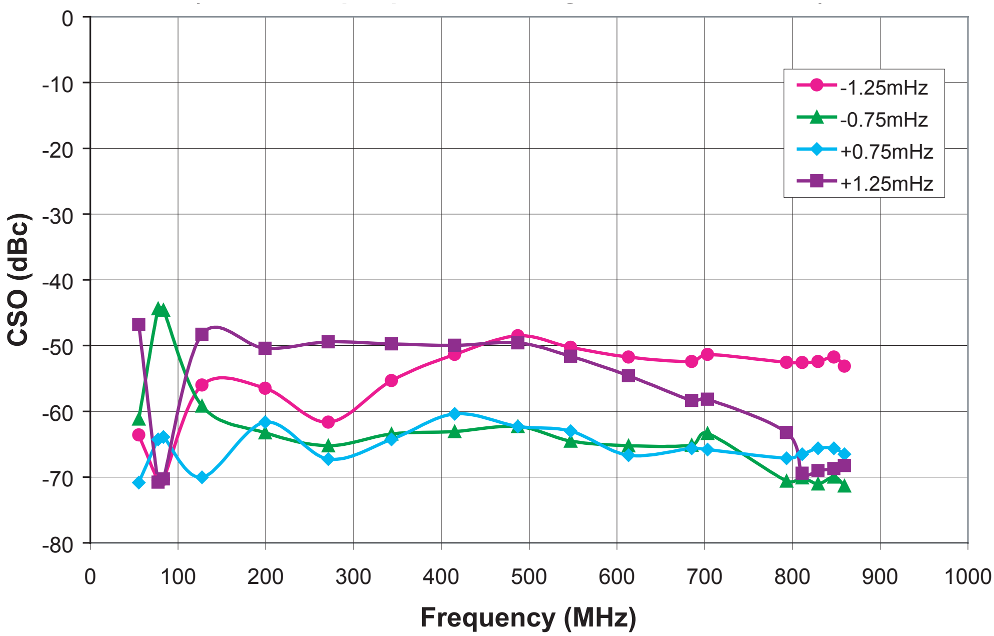


Figure 5: CSO vs. Frequency
(+15 dBmV input power, +3dBmV Attack, 129 channels - flat, Tc = +55°C)

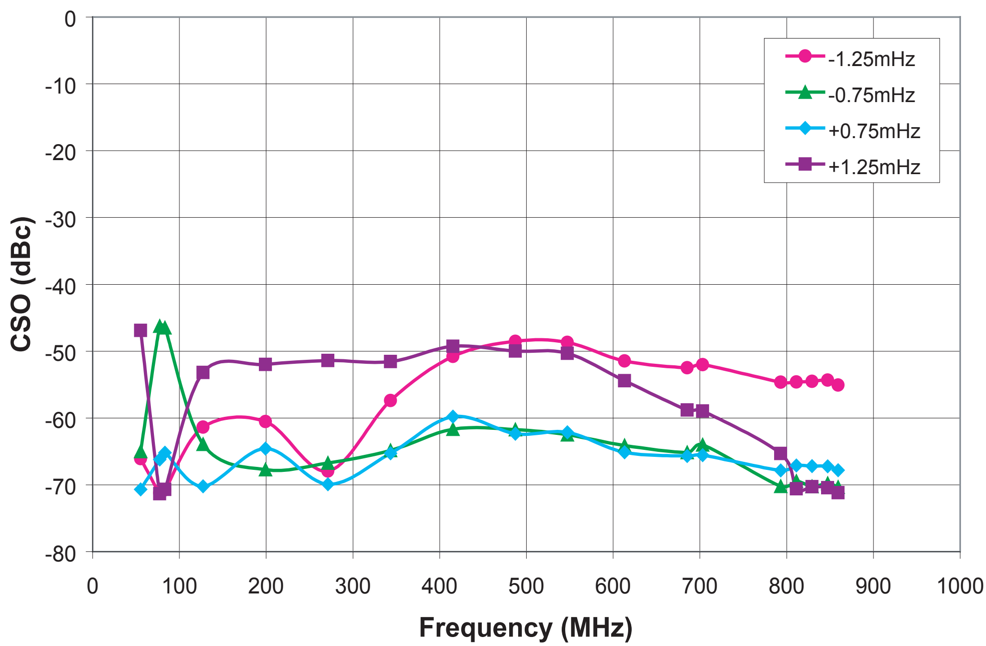


Figure 6: CSO vs. Frequency
(+20 dBmV input power, +3 dBmV Attack / 129 channels - flat, Tc = +55°C)

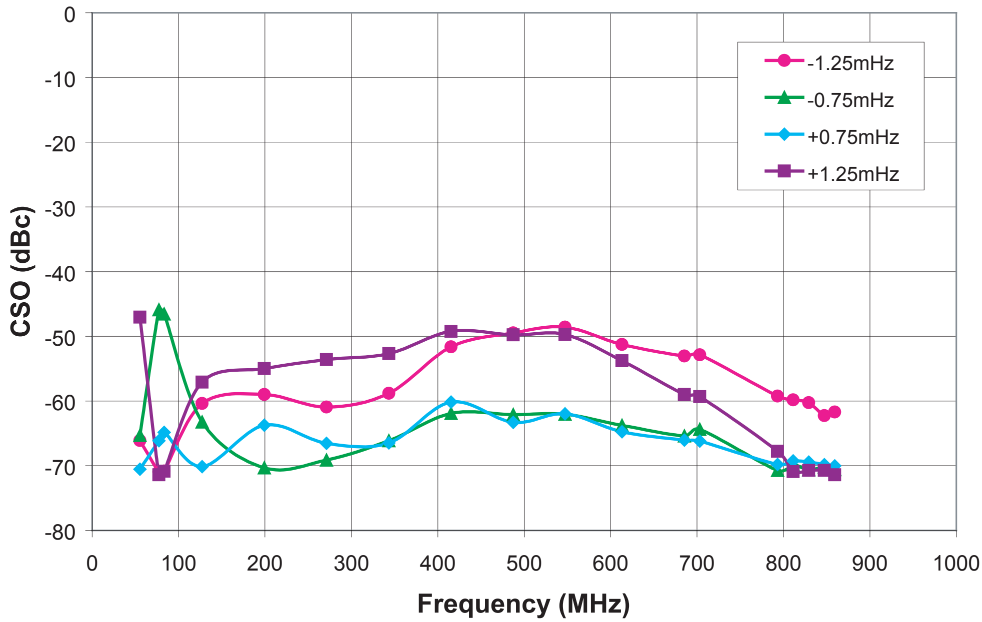


Figure 7: CTB vs. Frequency
(129 channels - flat, Tc = +55°C)

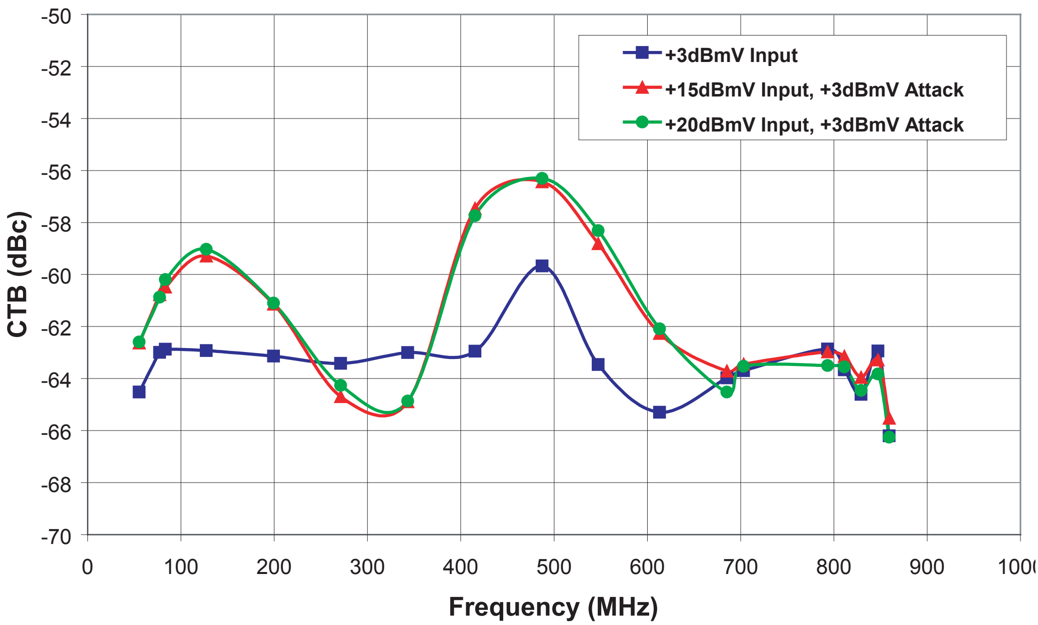


Figure 8: XMOD vs. Frequency
(129 channels - flat, Tc = +55°C)

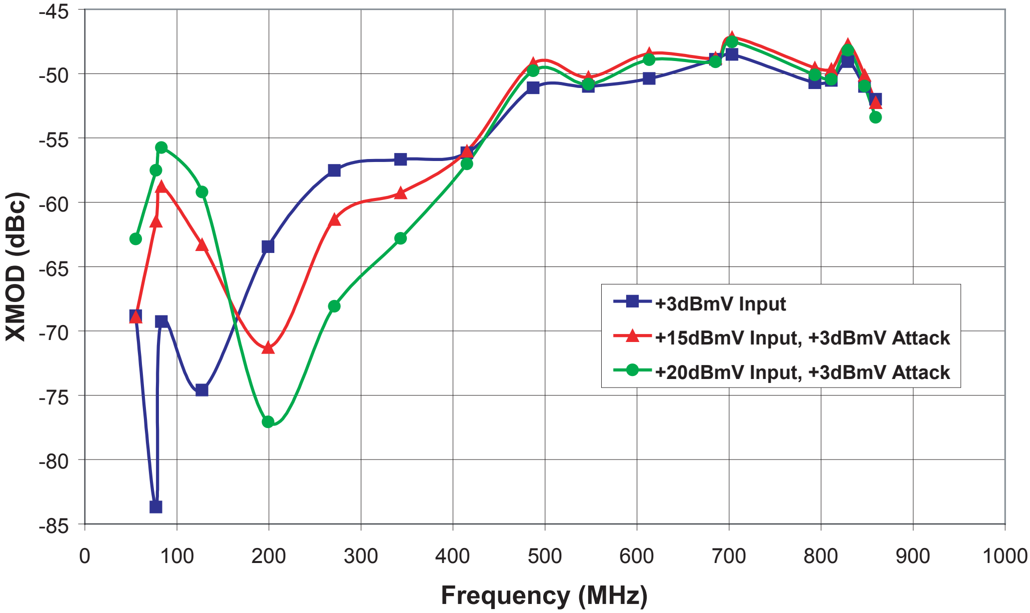


Figure 9: Gain & NF vs. Frequency
(Tc = +55°C)

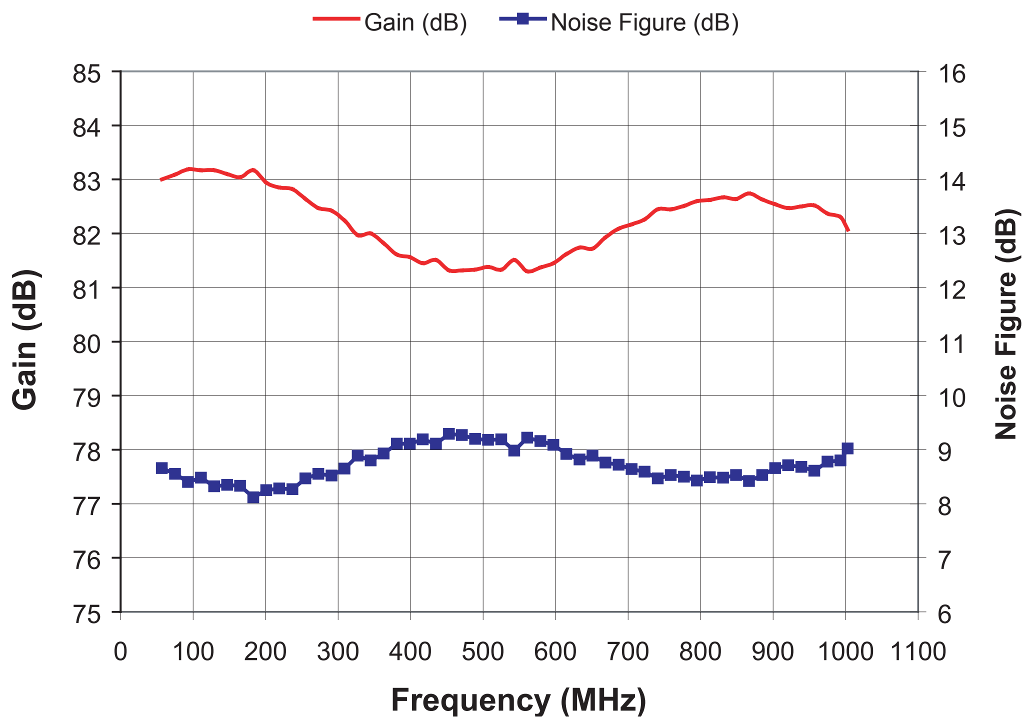
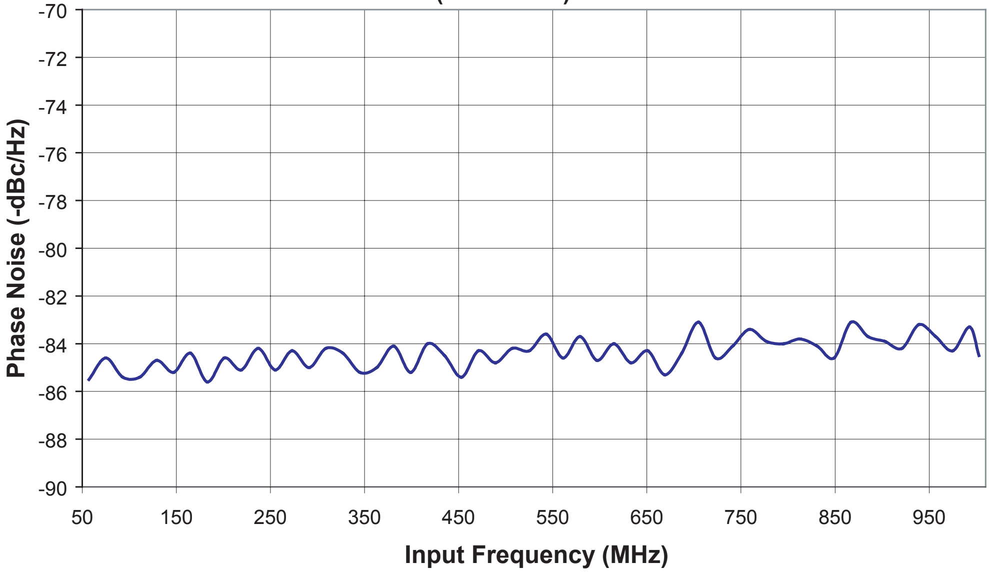


Figure 10: Composite Oscillator Phase Noise @ 10 KHz Offset
(T_C = +55°C)



LOGIC PROGRAMMING

This section describes the programming interface for the ANADIGICS AIT1042 integrated tuner.

PHYSICAL INTERFACE

Hosts that conform to the I^2C-Bus Specification standard can be used to program the AIT1042. The physical layer interface is a two-wire serial bus using CLOCK and DATA digital lines. The nominal bit rate of the interface is 400 kbits/sec. For data transmission, the signal on the DATA line must be stable when the CLOCK signal is high, and the state of the data must change only while the CLOCK signal is low. A logic level transition on the DATA line during a high CLOCK signal indicates the beginning or end of a data transmission, as specified in the following sections and shown in **Figure 4**.

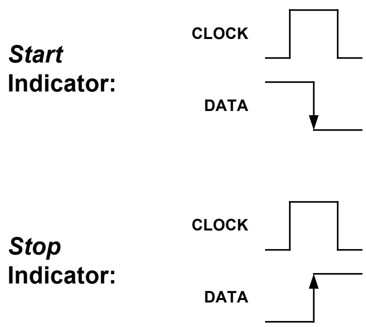


Figure 4: Transmission Indicators

ADDRESSING THE AIT1042

The AIT1042 monitors the CLOCK and DATA signals for a *Start* indication from the host. A *Start* is indicated by a high-to-low transition of the DATA signal while the CLOCK signal is high. Immediately following the *Start* indicator, the host sends an 8-bit address word to the AIT1042. Address words depend on the voltage on Pin 25 (V_{AS}), as shown in **Table 7** (the MSB is sent first, LSB last). Once the AIT1042 has recognized the *Start* indicator and a valid address word, it sends an address acknowledgement to the host by pulling the DATA line low for one clock pulse. The host can then begin to send data to program the AIT1042.

Table 7: Address Select Decoding
(V_{DD} = +5 V)

Pin 25 V_{AS} Voltage	Address (Hex)
1.1 to 1.7 V	C0
0 to 0.8 V	C2
2.1 to 2.7 V	C4
4.2 V to V_{DD}	C6

Sending Data

If the received address byte matches the address set by the V_{AS} voltage, the AIT1042 will acknowledge by pulling the data low before the 9th positive clock edge. The host can then begin sending programming data in 8-bit words. The MSB is sent first and the LSB last. The AIT1042 acknowledges receipt by pulling the DATA line low for one clock pulse after each received byte. The data acknowledgement tells the host it may send the next data word. Each group of three data words (24 bits total) is used to program one of seven registers described below.

Completing Data Transmission

After sending the final data word, the host sends a *Stop* indicator to mark the end of data transmission. A *Stop* is indicated by a low-to-high transition of the DATA signal while the CLOCK signal is held high. After receiving the *Stop* indicator, the AIT1042 ceases to send further acknowledgements and begins to monitor the CLOCK and DATA signals for the next *Start* indicator.

Note: The Stop *indicator does not directly control when the programming data is latched or takes effect; the data takes effect immediately following the receipt of each three-word block of data, which represents a complete 24-bit divider register.*

Re-sending Data

If, for some reason, the data transmission fails or is interrupted, the host can resend the data. To resend data, a new *Start* indicator and address word must be sent prior to any data words.

PROGRAMMING THE AIT1042

This section describes how to program the registers of the AIT1042 to control its operation. The 24-bit registers that control the dividers and other functions are each segmented into three 8-bit data words. Some bits have required fixed values (reserved bits and addressing), while others are used for control and synthesizer operation. The grayed areas of the addresses and control registers are fixed values and must be set as indicated in **Table 8**.

Control Register I

Control register I has two user programmable functions:

- Wake-up (Bit 19)
- Charge pump current settings (Bits 8-10 and bits 12-14) in the synthesizers

Table 9 shows how the Wake-up bit is used to control power up of the AIT1042. When the device is initially powered up the wake up bit (19) is set to 0 and the device will draw minimum current. Setting bit 19 to 1 will turn the device on for normal operation.

The charge pump current settings for the upconverter (CPI1) and downconverter (CPI2) synthesizers are set by Bits 8-10 and Bits 12-14, respectively. Refer to **Table 10**.

MSB — **Table 8: Control Register I** — **LSB**

PLL_CtrlI (Control Register I)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	W	0	0	0	0	CPI2			0	CPI1			1	0	0	0	0	0	0	1

Table 9: Wake-up Mode Bit

Bit 19	Wake-up mode
0	Power down (default)
1	Normal operation

Table 10: Charge Pump Current Bits

CPIx Bits	Charge Pump Current
0000	(reserved)
0001	0.7 mA
0010	1.3 mA
0011	1.9 mA
0100	2.5 mA
0101	3.1 mA
0110	3.6 mA
0111	4.1 mA

Note: 1000 thru 1111 are Reserved.

Control Register II

Control register II contains only fixed values of address and reserve bits that must be programmed as indicated in **Table 11**.

Table 11: Control Register II

MSB | LSB

PLL_CtrlII (Control Register II)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Control Register III

Control register III contains only fixed values of address and reserved bits that must be programmed as indicated in **Table 12**. There are no user programmable bits and this control register must be transmitted last.

Table 12: Control Register III

MSB | LSB

PLL_CtrlIII (Control Register III)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1

Upconverter Main and Reference Divider Registers

The upconverter main and reference divider registers are used to set the A, B and R counters in the upconverter synthesizer. The output frequency for the synthesizer is computed using the following equation:
where:

$$f_{osc} = \frac{[(16)(B) + A]\, f_{xtal}}{R}$$

f_{OSC} is the upconverter local oscillator (LO1) frequency
B is the divide ratio of the B counter (2 to 2047 inclusive)
A is the divide ratio of the A counter ($0 \leq A \leq P-1$, $A < B$)
f_{XTAL} is the frequency of the reference crystal oscillator
R is the divide ratio of the R counter (2 to 1023 inclusive)
The preset modulus of the prescalar is 16 and is not programmable.

In the main divider register, the A counter is set via Bits 2-8 and the B counter is set with Bits 9-19. In the reference divider register, the R counter is set with Bits 2-11. The remaining bits must use the fixed values indicated in Tables 13 and 14.

MSB **Table 13: Upconverter Main Divider Register** **LSB**

PLL1_Main (Upconverter Main Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	B counter											A counter							1	1

MSB **Table 14: Upconverter Reference Divider Register** **LSB**

PLL1_Ref (Upconverter Reference Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0	0	0	0	0	R counter										1	0

Downconverter Main and Reference Divider Registers

The downconverter main and reference divider registers are used to set the A, B and R counters in the downconverter synthesizer. The output frequency for the synthesizer is computed using the following equation:

$$f_{osc} = \frac{[(64)(B) + A]\, f_{xtal}}{R}$$

where:

- f_{OSC} is the downconverter local oscillator (LO2) frequency
- B is the divide ratio of the B counter (2 to 2047 inclusive)
- A is the divide ratio of the A counter ($0 \leq A \leq P-1$, $A < B$)
- f_{XTAL} is the frequency of the reference crystal oscillator
- R is the divide ratio of the R counter (2 to 4095 inclusive)
- The preset modulus of the prescalar is 64 and is not programmable.

In the main divider register, the A counter is set via Bits 2-8 and the B counter is set with Bits 9-19. In the reference divider register, the R counter is set with Bits 2-13. The remaining bits must use the fixed values indicated in **Tables 15 and 16**.

Table 15: Downconverter Main Divider Register

MSB **LSB**

PLL2_Main (Downconverter Main Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	B counter											A counter							0	1

Table 16: Downconverter Reference Divider Register

MSB **LSB**

PLL2_Ref (Downconverter Reference Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0	0	0	R counter												0	0

Synthesizer Programming Example

The following is an example for programming the two synthesizers in the AIT1042 device. The calculations will determine the values required to input into the four main registers:

- Main divider and reference divider for the upconverter
- Main divider and reference divider for the downconverter.

Conditions

The desired CATV frequency to receive is 55.25MHz (picture carrier).
The 1st IF (HIF) is 1690.75MHz and the 2nd IF is 45.75MHz.
Phase detector comparison frequency for the upconverter is 2000KHz (2MHz).
Phase detector comparison frequency for the downconverter is 62.5KHz.
The crystal (xtal) reference oscillator frequency is 16MHz
The preset modulus of the prescalar for: Upconverter - P = 16 and for Downconveter – P = 64.

Calculation of the Reference Divider Values

The value for each reference divider can be calculated by dividing the reference oscillator frequency by the desired phase detector comparison frequency:

R = Fref.osc./FPD

For the upconverter, the 16MHz crystal oscillator frequency and the 2000KHz phase detector comparison frequency are used to get:
RPLL1 = 16MHz/2000KHz(2MHz) = 8. Therefore, the bit values for the upconverter reference divider register would be: 0000001000

For the downconverter, the 16MHz crystal oscillator frequency and the 62.5KHz phase detector comparison frequency are used to get: RPLL2 = 16MHz/62.5KHz (0.625MHz) = 256. Therefore, the bit values for the downconverter reference divider register would be:
0100000000

Main Divider Register Calculations

The values of the A and B counters are determined by the desired VCO output frequency of the on-chip local oscillators and the phase detector comparison frequency:

N = FVCO/FPD B = trunc(N/P) A = N – (B x P)

The upconverter local oscillator frequency will be 1690.75MHz + 55.25MHz = 1746MHz for this example. Therefore, the N value for PLL1 will be = 1746MHz/2MHz = 873, the B value for PLL1 will be = (873/16) = 54, and the A value for PLL1 will be = 873 – (54 x 16) = 9. The upconverter main divider register value will be: B = 00000110110, A = 0001001

The downconverter local oscillator frequency will be 1690.75 – 45.75MHz = 1645MHz.
Therefore, the N values for PLL2 will be 1645MHz/62.5KHz = 26320, the B value for PLL2 will be = (26320/64) = 411, and the A value for PLL2 will be = 26320 – (411 x 64) = 16. The downconverter main register value will be: B = 00110011011, A = 0010000

Table 17: Complete Register Map

MSB | LSB

PLL2_Ref (Downconverter Reference Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0	0	0	R counter												0	0

PLL2_Main (Downconverter Main Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	B counter											A counter							0	1

PLL1_Ref (Upconverter Reference Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0	0	0	0	0	R counter										1	0

PLL1_Main (Upconverter Main Divider Register)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	B counter											A counter							1	1

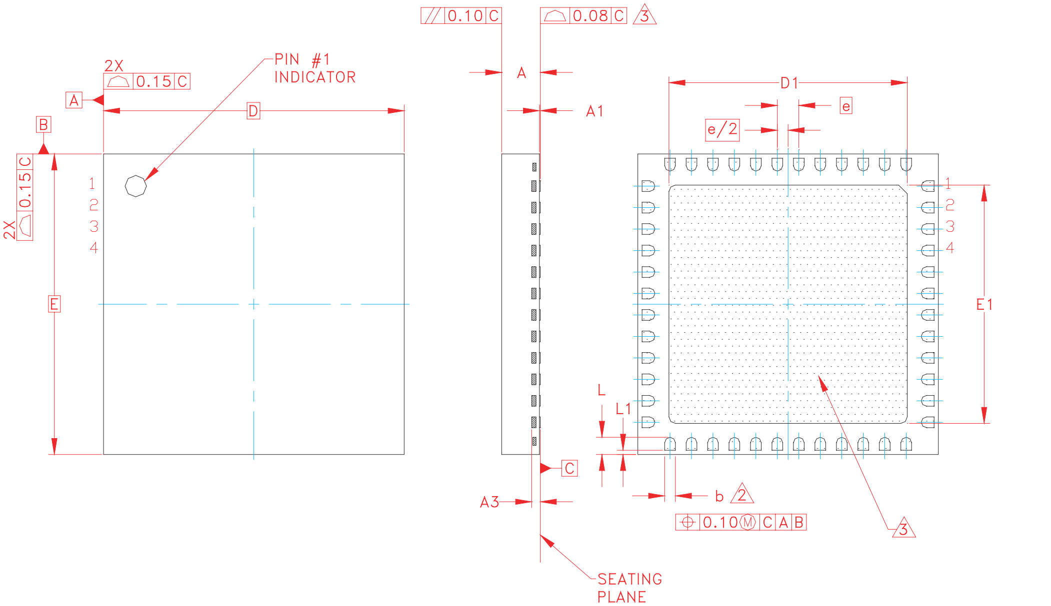
PLL_CtrlI (Control Register I)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	W	0	0	0	0	CPI2			0	CPI1			1	0	0	0	0	0	0	1

PLL_CtrlII (Control Register II)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

PLL_CtrlIII (Control Register III)																							
First data byte								Second data byte								Third data byte							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1

Reminder: Program Control Register III last.

PACKAGE OUTLINE



SYMBOL	DIMENSIONS–MM		DIMENSIONS–INCHES		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.80	1.00	0.031	0.039	–
A1	0.00	0.05	0.000	0.002	–
A3	0.20 REF.		0.008 REF.		–
b	0.18	0.30	0.007	0.012	48X
D	7.00 BSC		0.275 BSC		–
D1	5.40	5.65	0.212	0.222	–
E	7.00 BSC		0.275 BSC		–
E1	5.40	5.65	0.212	0.222	–
e	0.50 BSC		0.020 BSC		–
L	0.30	0.50	0.012	0.020	48X
L1	0.00	0.10	0.000	0.003	48X

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TERMINAL TIP–NOT IN RADIUS AREA. RADIUS OPTIONAL.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. RADIUS ON TERMINAL IS OPTIONAL.

Figure 12: S38 Package Outline - 48 Pin 7 mm x 7 mm x 1 mm QFN

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AIT1042RS38P8	O°C to +85°C	RoHS-Compliant 48 pin QFN Package 7mm x 7mm x 1mm	Tape & Reel, 2500 pieces per Reel
AIT1042RS38P9	O°C to +85°C	RoHS-Compliant 48 pin QFN Package 7mm x 7mm x 1mm	Special Handling

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