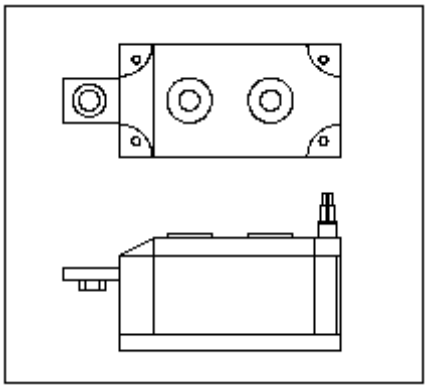
IRK.170, .230, .250 SERIES
High Voltage Thyristor/Diode and Thyristor/Thyristor

FEATURES



- *Electrically isolated base plate.*
- *3000 V_{RMS} isolating voltage.*
- *Industrial standard package.*
- *Simplified mechanical designs, rapid assembly.*
- *High surge capability.*
- *Large creepage distances.*
- *Beryllium oxide substrate.*

DESCRIPTION

These IRK series of Power Modules use power thyristors/ diodes in four basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel.

These modules are intended for general purpose applications such as battery chargers, welders and plating equipment.

MAJOR RATINGS & CHARACTERISTICS

Parameters		IRK.170	IRK.230	IRK.250	Units
$I_{T(AV)}$	@ 85°C	170	230	250	A
$I_{T(RMS)}$		377	510	555	A
I_{TSM}	@ 50 Hz	5100	7500	8500	A
I^2t	@ 50 Hz	131	280	361	kA^2s
$I^2\sqrt{t}$		1310	2800	3610	$kA^2\sqrt{s}$
V_{DRM} -V_{RRM}		Up to 1800	Up to 1800	Up to 1800	V
T_J		-40 to 130			°C

ELECTRICAL SPECIFICATION

VOLTAGE RATINGS

Type Number	Voltage Code	V_{RRM} / V_{DRM}, max. repetitive peak reverse and off-state voltage blocking voltage V	V_{RSM}, max. non-repetitive peak reverse voltage V	I_{DRM} / I_{RRM} max. @ 130°C mA
	04	400	500	50
IRK.170	06	600	700	50
IRK.230	08	800	900	50
IRK.250	10	1000	1100	50
	12	1200	1300	50
	14	1400	1500	50
	16	1600	1700	50
	18	1800	1900	50

ON-STATE CONDUCTION

	Parameters	IRK.170	IRK.230	IRK.250	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	170	230	250	A	180° conduction, half sine wave		
	@ Case temperature	85	85	85	°C			
$I_{T(RMS)}$	Max. RMS on-state current	377	510	555	A	as AC switch		
I_{TSM}	Max. peak, one cycle on-state, non-repetitive surge current	5100	7500	8500	A	t = 10ms	No voltage reapplied	Sinusoidall half wave, Initial $T_J = T_J$ max.
		4300	6300	7150	A	t = 10ms	100% V_{RRM} reapplied	
I^2t	Maximum I^2t for fusing	131	280	361	kA^2s	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max.
		92.5	198	255	kA^2s	t = 10ms	100% V_{RRM} reapplied	
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	1310	2800	3610	$kA^2\sqrt{s}$	t = 0.1 to 10ms. No voltage reapplied.		
$V_{T(TO)1}$	Low level value of threshold voltage	0.89	1.03	0.97	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.12	1.07	1.00	V	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
r_{t1}	Low level on-state slope resistance	1.34	0.77	0.60	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
r_{t2}	High level on-state slope resistance	0.96	0.73	0.57	mΩ	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
V_{TM}	Max. on-state voltage drop	1.60	1.59	1.44	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = T_J$ max., 180° conduction AV. power = $V_{T(TO)} \times I_{T(AV)} + r_1 \times (I_{T(RMS)})^2$		
I_H	Maximum holding current	500			mA	Anode supply = 12V, initial I_T = 30A, T_J = 25°C		
I_L	Max. latching current	1000			mA	Anode supply = 12V, resistive load = 1Ω, gate pulse : 10V, 100µs, T_J = 25°C		

SWITCHING

t_d	Typical delay time	1.0	1.0	1.0	µs	T_J = 25°C	Gate current = 1A $dIg/_{dt}$ = 1A/µs
t_r	Typical rise time	2.0	2.0	2.0	µs	T_J = 25°C	Vd = 0.67% V_{DRM}
t_q	Typical turn-off time	50-150			µs	I_{TM} = 300A; dI/dt = 15A/µs; $T_J = T_J$ max.: Vr = 50V; dV/dt = 20V/µs; Gate 0V, 100ohm	

BLOCKING

	Parameter	170	230	250		Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	1000			V/µs		T_J = 125°C, exponential to 67% rated V_{DRM}
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	50			mA		T_J = 125°C, rated V_{DRM} /V_{RRM} applied
V_{INS}	RMS isolation voltage	3500			V		50Hz,Circuit to base, all terminal shorted,25°C,1sec

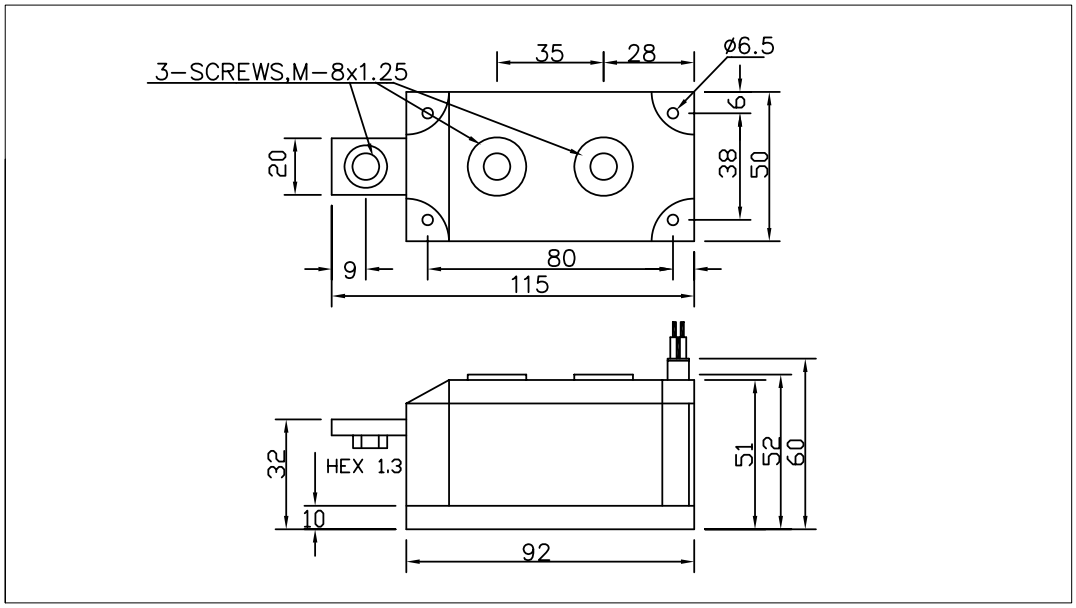
TRIGGERING

	Parameter	170	230	250	Units	Conditions
P_{GM}	Maximum peak gate power	10.0			W	T_J = 125°C, $t_p \leq$ 5ms
$P_{G(AV)}$	Maximum average gate power	2.0				T_J = 125°C, f= 50Hz, d% = 50
I_{GM}	Max. peak positive gate current	3.0			A	T_J = 125°C, $t_p \leq$ 5ms
$+V_{GM}$	Max. peak positive gate voltage	20			V	T_J = 125°C, $t_p \leq$ 5ms
$-V_{GM}$	Max. peak negative gate voltage	5.0				
I_{GT}	DC gate current required to trigger	TYP.		MAX.	mA	Max. required gate trigger/current / voltage are the lowest value which will trigger all units 12V anode-to-cathode applied.
		350		--		T_J = -40°C
		200		150		T_J = 25°C
		100		--		T_J = 125°C
V_{GT}	DC gate voltage required to trigger	4.0		--	V	T_J = -40°C
		3.0		3.0		T_J = 25°C
		2.0		--		T_J = 125°C
V_{GD}	DC gate voltage not to trigger	0.25			V	T_J = 125°C Max. gate current / voltage not to trigger the max. value which will not trigger any unit with rated V_{DRM}anode-to-cathode applied
I_{GD}	DC gate current not to trigger	10.0			mA	T_J = 125°C
di/dt	Maximum critical rate of rise of turned-on current	500			A/µs	T_J = 125°C, I_{TM}=400A ,rated V_{DRM} applied

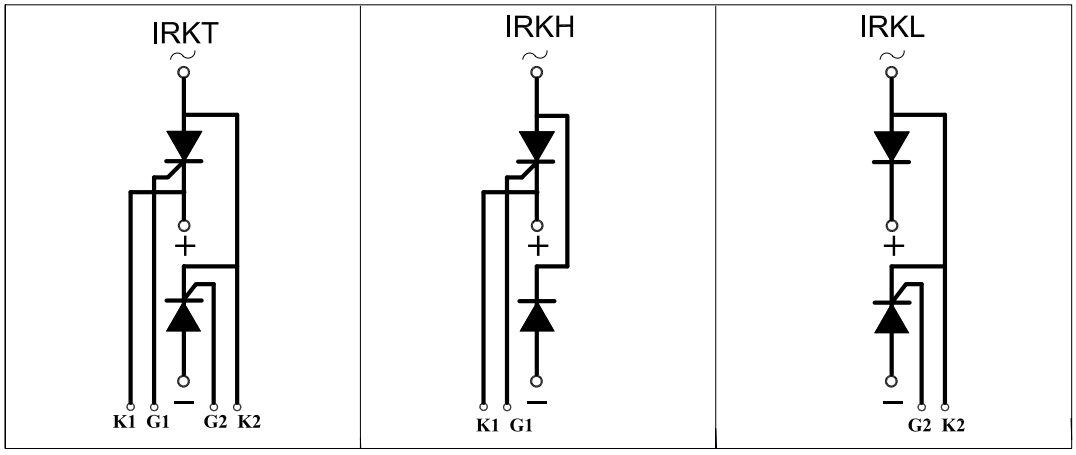
THERMAL AND MECHANICAL SPECIFICATION

	Parameter	170	230	250	Units	Conditions
T_J	Max. operating temperature range	-40 to 130			°C	
T_{stg}	Max. storage temperature range	-40 to 150				
R_{thJ-C}	Max. thermal resistance, junction to case	0.17	0.125	0.125	K/W	Perjunction, DC operation
R_{thJ-C}	Max. thermal resistance, junction to heatsink	0.02	0.02	0.02	K/W	Mountingsufaceflat,smooth and greased
T	Mounting tourque, ±10%	4 to 6			Nm	For Module to heatsink and busbar to Module
w t	Approximate weight	500			g	
	Case style	MAGN-A-PAK				

OUTLINE DIAGRAM



Circuit Configuration Table



Ordering Information Table

IRK	T	170	/	16
①	②	③		④

① – Module type
② – Circuit configuration (See Circuit Configuration table)
③ – Current Code
④ – Voltage Code (See Voltage Ratings table)

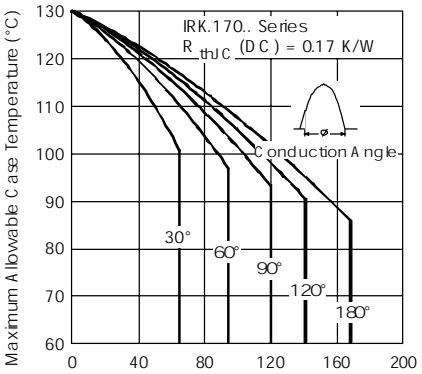


Fig. 1 - Current Ratings Characteristics

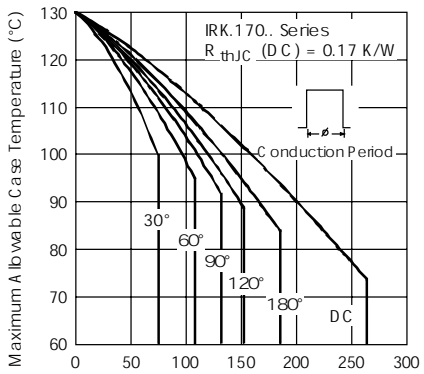


Fig. 2 - Current Ratings Characteristics

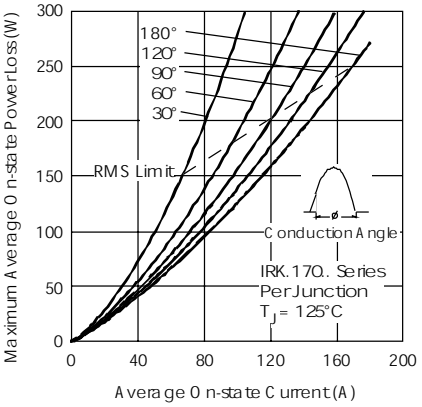


Fig. 3 - On-state Power Loss Characteristics

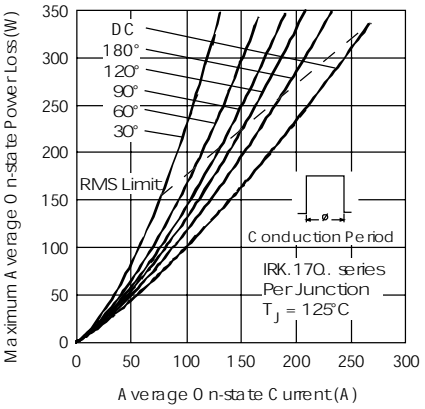


Fig. 4 - On-state Power Loss Characteristics

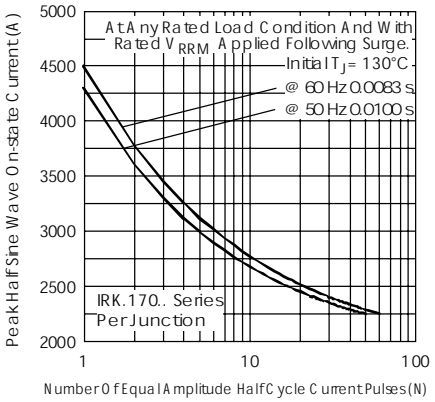


Fig. 5 - Maximum Non-Repetitive Surge Current

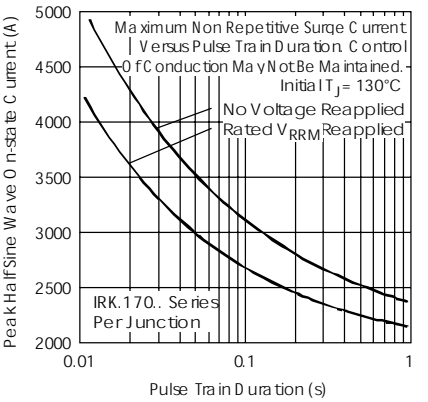


Fig. 6 - Maximum Non-Repetitive Surge Current

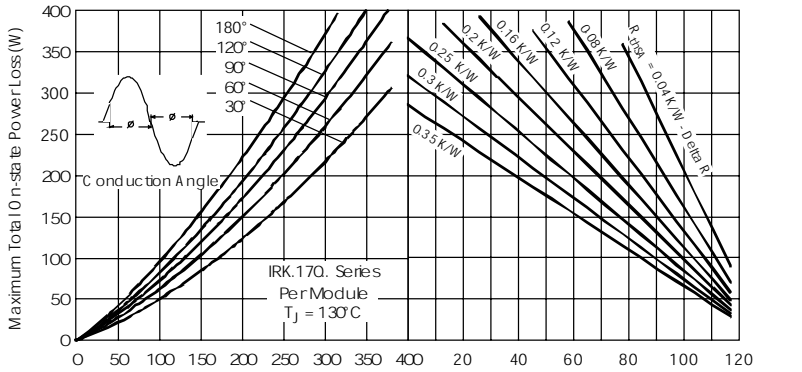


Fig. 7 - On-state Power Loss Characteristics

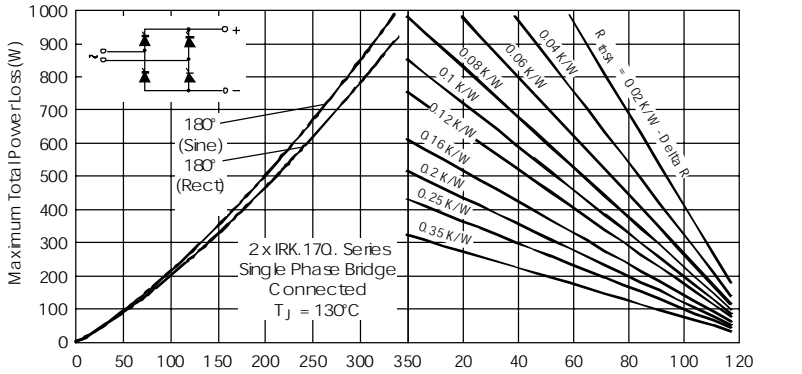


Fig. 8 - On-state Power Loss Characteristics

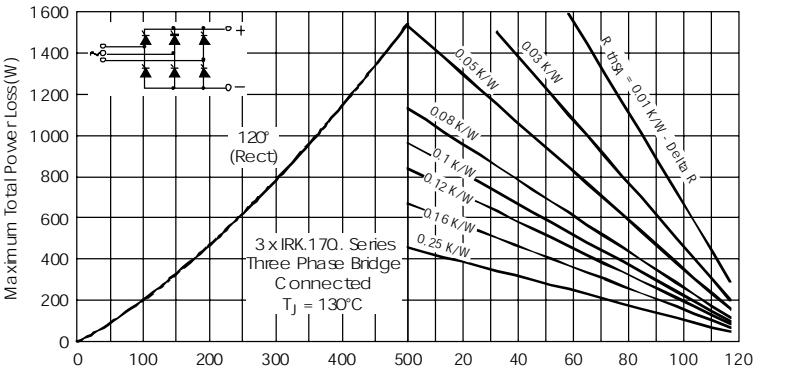


Fig. 9 - On-state Power Loss Characteristics

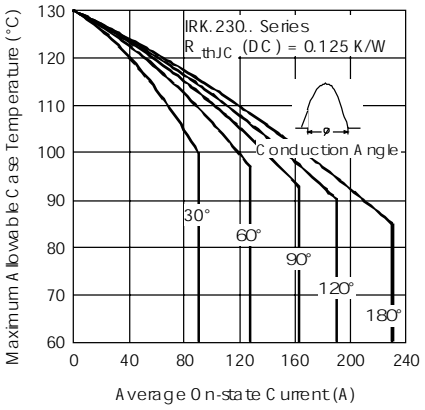


Fig. 10 - Current Ratings Characteristics

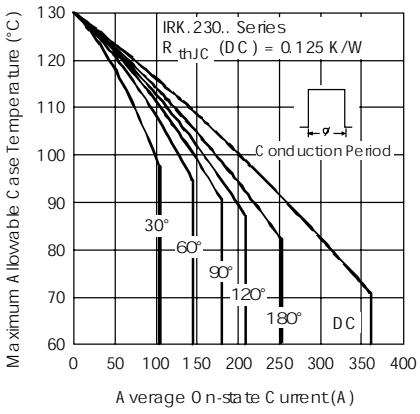


Fig. 11 - Current Ratings Characteristics

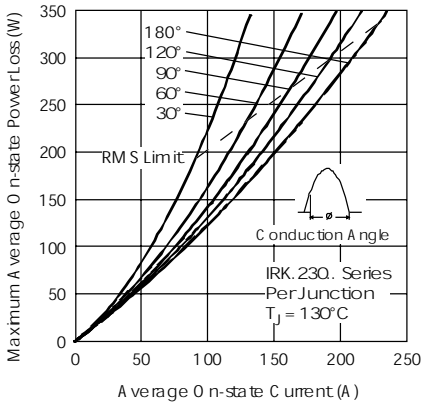


Fig. 12 - On-state Power Loss Characteristics

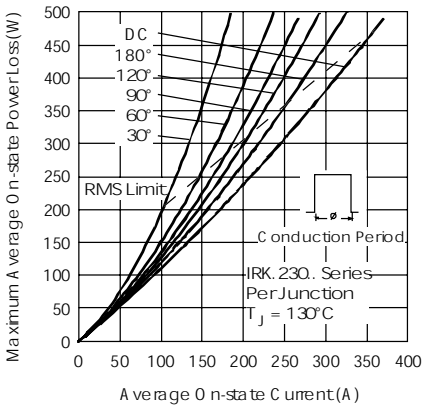


Fig. 13 - On-state Power Loss Characteristics

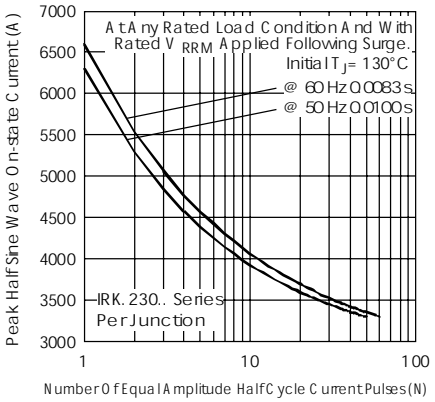


Fig. 14 - Maximum Non-Repetitive Surge Current

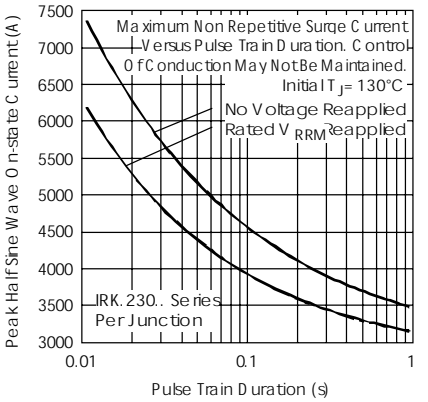


Fig. 15 - Maximum Non-Repetitive Surge Current

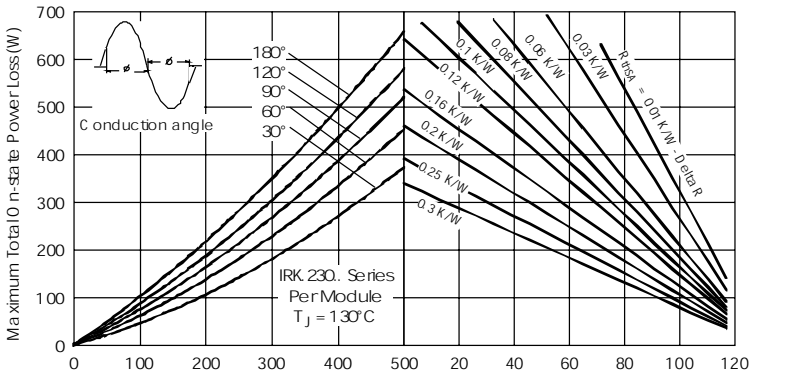


Fig. 16 - On-state Power Loss Characteristics

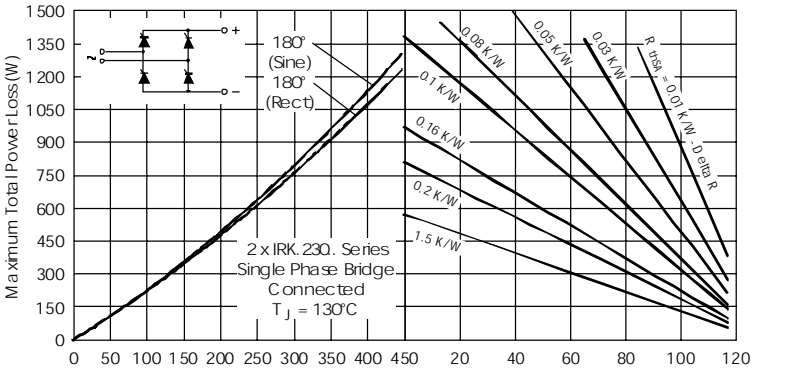


Fig. 17 - On-state Power Loss Characteristics

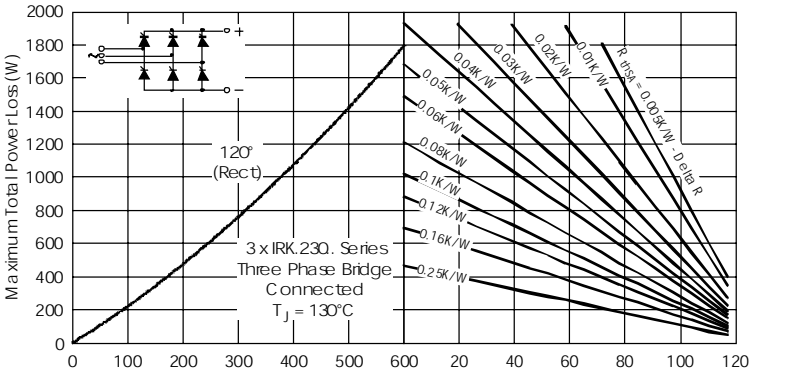


Fig. 18 - On-state Power Loss Characteristics

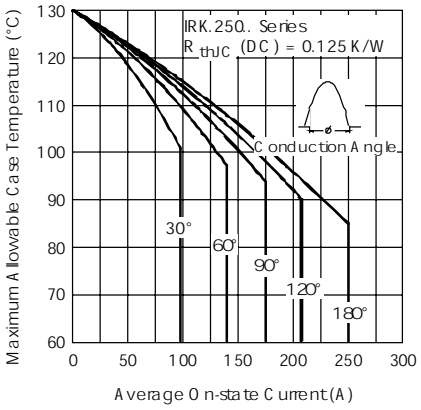


Fig. 19 - Current Ratings Chartacteristics

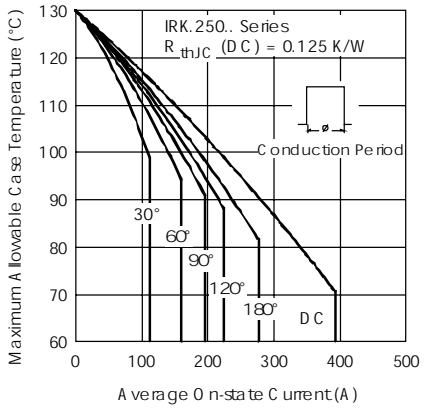


Fig. 20 - Current Ratings Chartacteristics

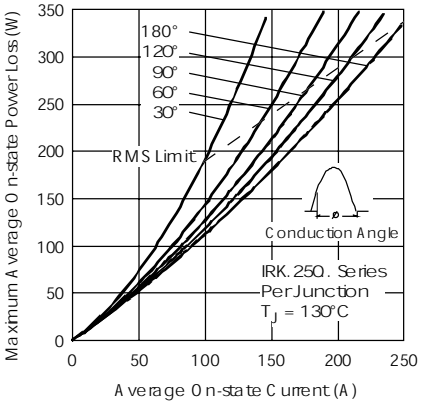


Fig. 21 - On-state Power Loss Characteristics

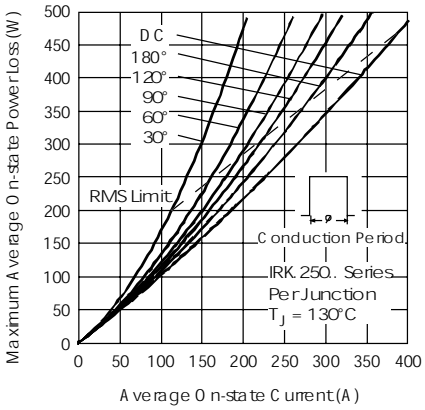


Fig. 22 - On-state Power Loss Characteristics

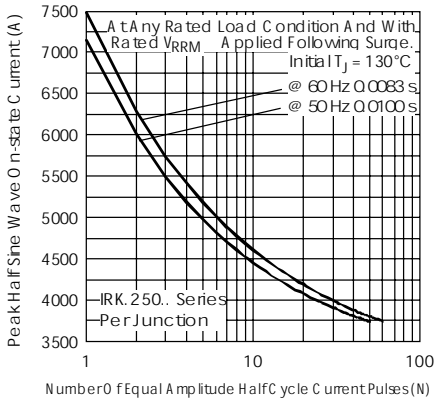


Fig. 23 - Maximum Non-Repetitive Surge Current

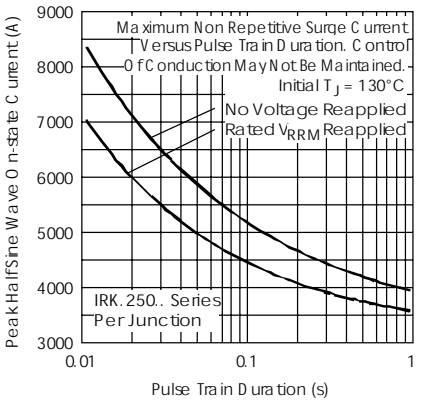


Fig. 24 - Maximum Non-Repetitive Surge Current

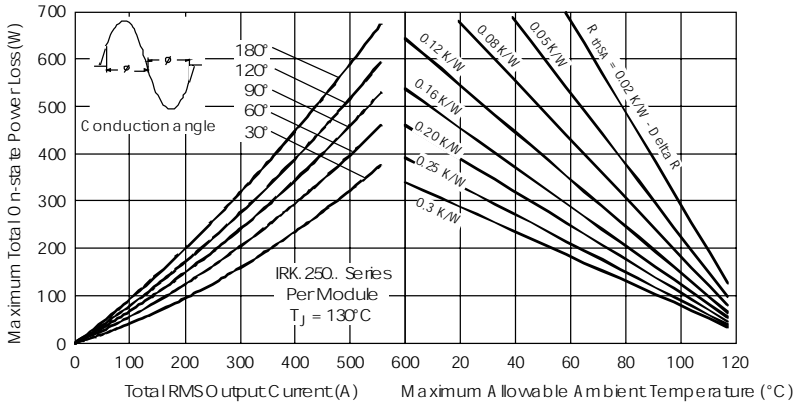


Fig. 25 - On-state Power Loss Characteristics

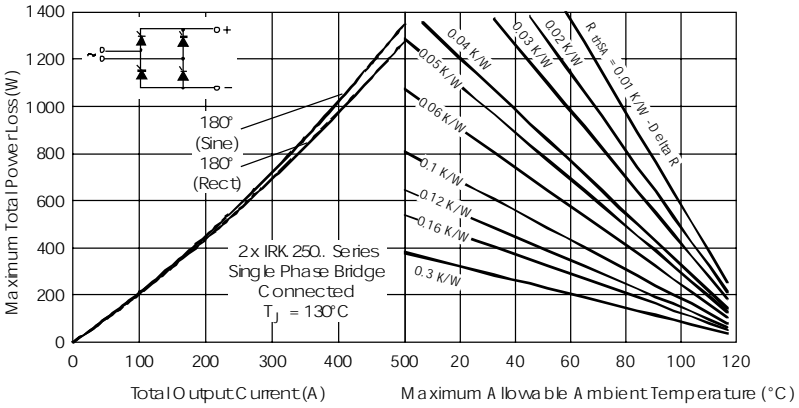


Fig. 26 - On-state Power Loss Characteristics

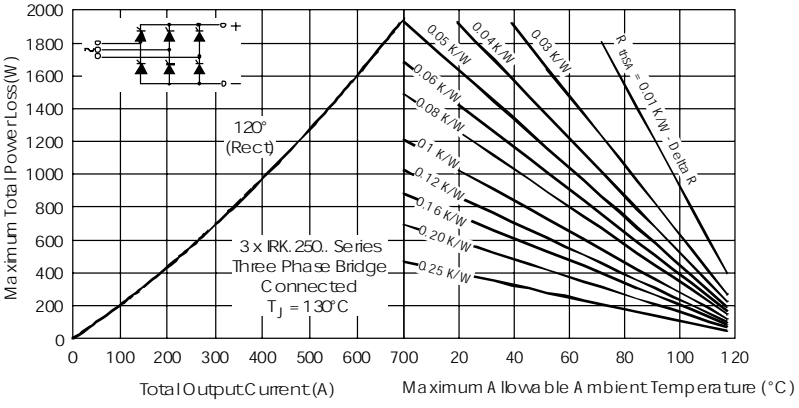


Fig.27 - On-state Power Loss Characteristics

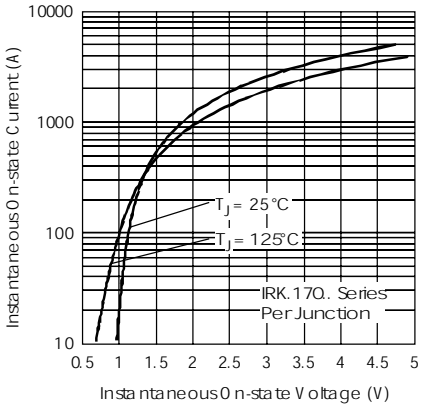


Fig. 28 - On-state Voltage Drop Characteristics

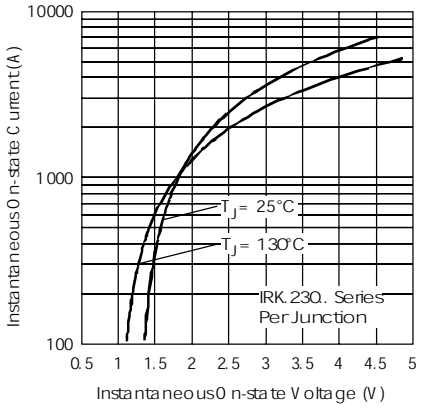


Fig. 29 - On-state Voltage Drop Characteristics

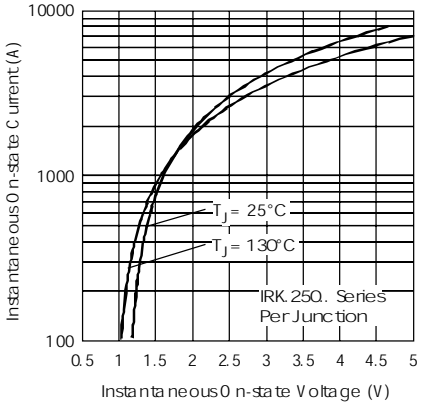


Fig. 30 - On-state Voltage Drop Characteristics

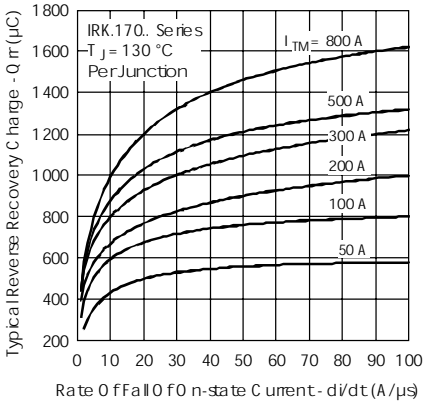


Fig. 31 - Reverse Recovery Charge Characteristics

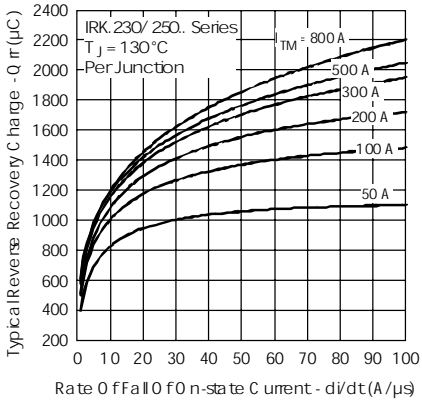


Fig. 32 - Reverse Recovery Charge Characteristics

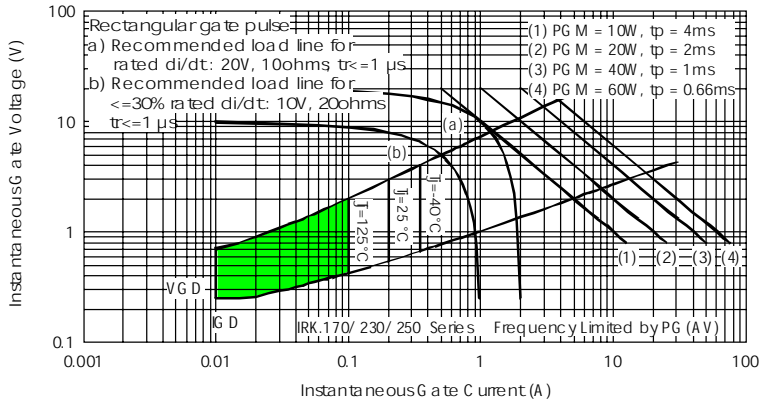


Fig. 33 - Gate Characteristics

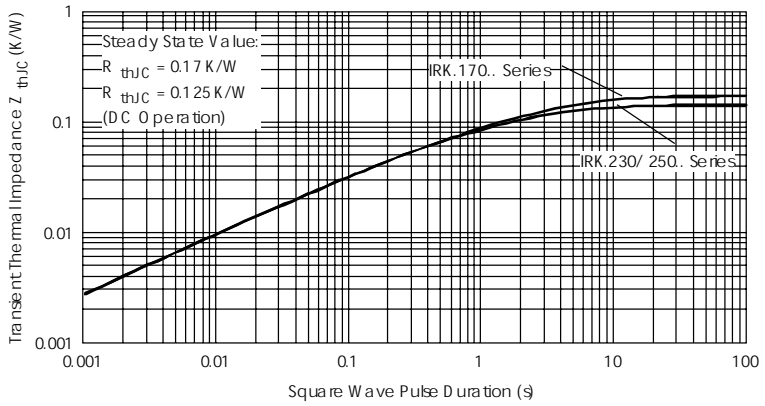


Fig. 34 - Thermal Impedance Z_{thJC} Characteristics