E981.07

Two Channel Sensor Interface PSI5

ADVANCE PRODUCT INFORMATION JUL 26, 2011

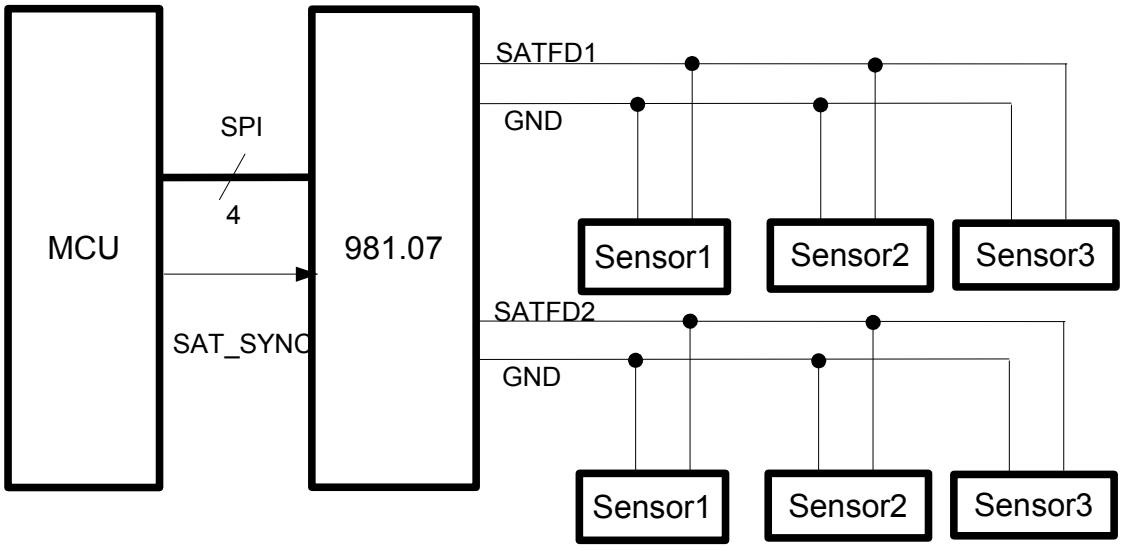
Features

- Two independent operating channels
- Device parameters comply with PSI5-P10P-500/3L (PSI5 spec 1.3)
- Applicable for parallel and universal mode (standard) as well, as daisy chain mode (increased)
- Channel output short circuit protected against 40V and GND.
- Channel output short circuit protected against every other channel.
- Current detection with adapted current threshold
- Data Manchester coded
- Operation with supply voltages of 5V and 3.3V typical
- SPI interface
- Over current switch off for every channel
- Temperature switch off for every channel

General Description

The circuit was developed to manage the connection and communication between a microcontroller unit (MCU) and up to six sensor satellites. It can be applied for example in a vehicle passenger restraint system. The device provide two independently operating channels. Every channel manages the communication with a maximum of three sensor satellites.
Each channel supplies the connected sensor devices with a regulated DC voltage, which is derived from an external source. The sensor data are extracted by measuring the current, modulated by the connected sensor devices, supplied by the regulator and communicated to the MCU via SPI interface. The current threshold is adapted to the quiescent current of the system. The data bits are coded using a Manchester format. The device operates with an external 4MHz/8MHz clock.

Typical Application



1 Package

1.1 Package Pinout QFN20L5 (lead less package 5x5 20 leads)

The device package follows JEDEC Specification MO-220-K (Variation VHHC-2).

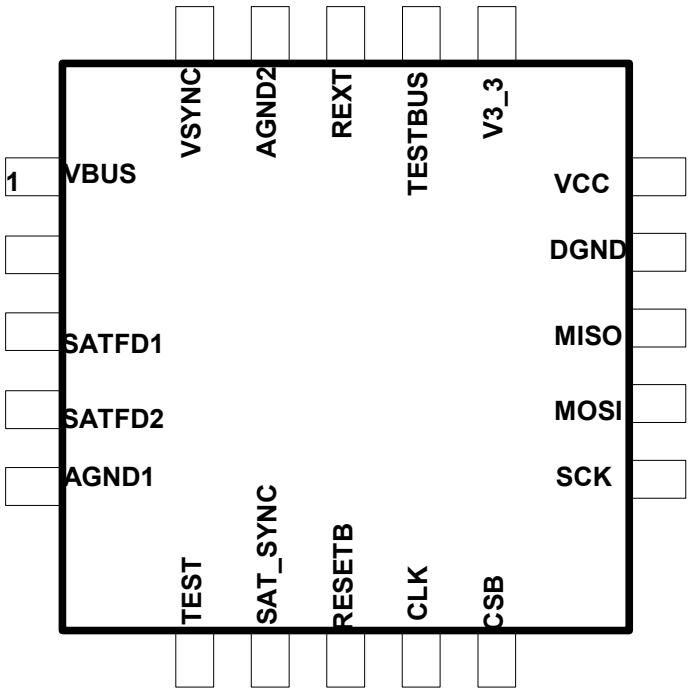


Figure 1.1-1 Package Pinout

1.2 Pin Function Description

Pin No.	Name	Description
1	VBUS	Supply voltage BUS
2	N.C.	Not connected to die
3	SATFD1	Satellite channel feed 1
4	SATFD2	Satellite channel feed 2
5	AGND1	Analogue Ground
6	TEST	Test Pin, connect to GND
7	SAT_SYNC	Sync pulse trigger input
8	RESETB	Reset input, active low
9	CLK	System clock input
10	CSB	Chip Select Input for SPI
11	SCK	Master Out Slave In, SPI CLock input
12	MOSI	Master Out Slave In, SPI Data input
13	MISO	Master In Slave Out, SPI Data output
14	DGND	Digital Ground
15	VCC	Input supply voltage, can be 5V or 3.3V. Has to be be connected to V3_3 in case of 3.3V input voltage. (Buffer cap higher than 22nF recommended)
16	V3_3	internal 3.3v regulator output: - in case Vcc = 5.0v: 47nF buffer cap recommended (22nF min) - in case Vcc = 3.3v: V3_3 to be shorted to Vcc
17	TESTBUS	Output analogue test bus, do not connect
18	REXT	External resistor for reference current
19	AGND2	Analogue Ground
20	VSYNC	Sync Supply Input
		Backside: exposed die Pad connected to AGND1 / AGND2 via bulk

2 Block Diagram

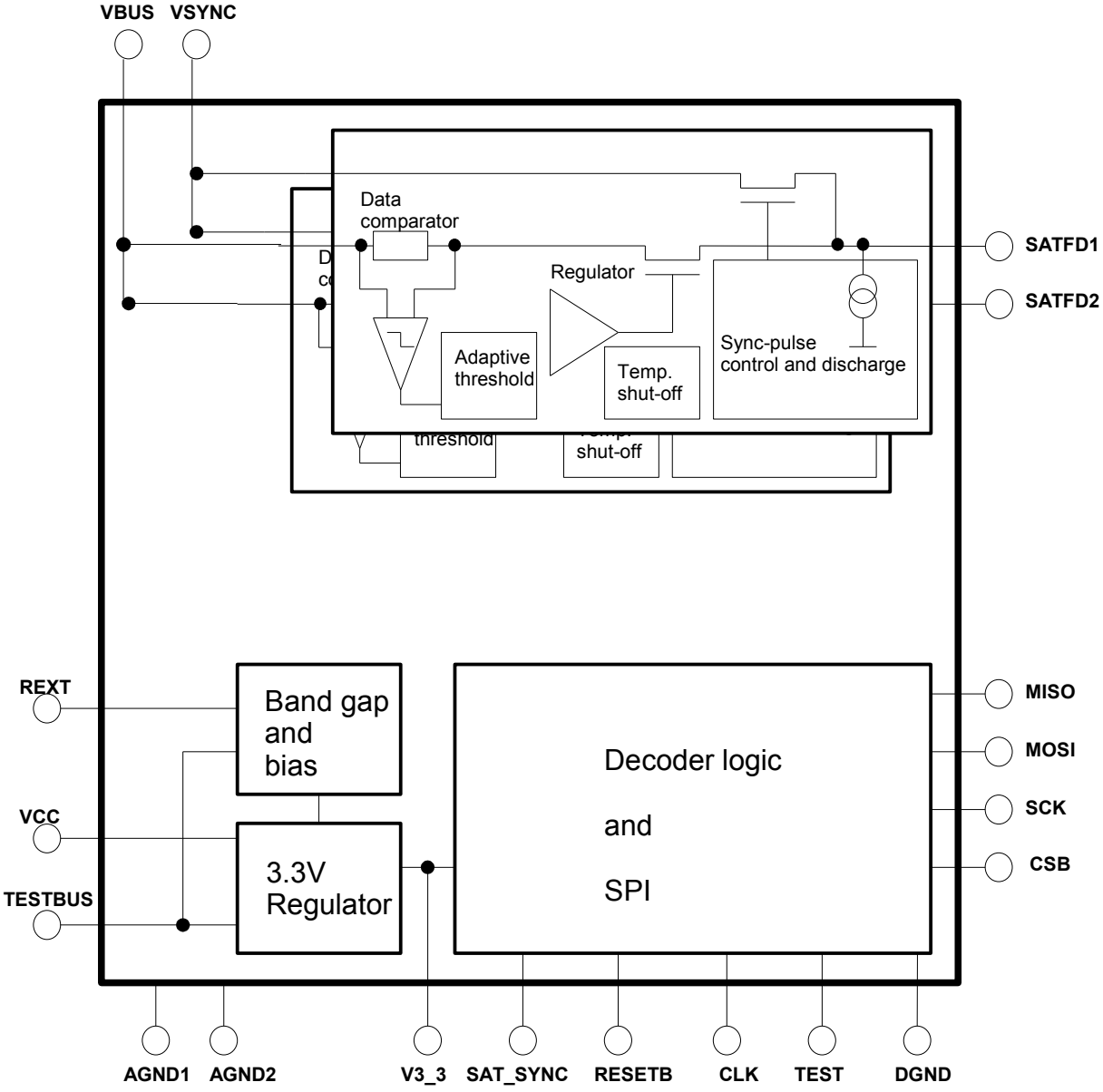


Figure 2-1 Block Diagram

3 Operation Conditions

3.1 Absolute Maximum Ratings

Operating the device beyond these limits may cause permanent damage.

No.	Parameter	Condition	Symbol	Min.	Max.	Unit
1	Supply voltage SYNC Pulse		VSYNC	-0.3	36	V
2	Voltage supply BUS		VBUS	-0.3	36	V
3	Voltage of satellite channel feed 1-2	Continuous	VSATFD1-2	-0.3	28	V
4	Voltage of satellite channel feed 1-2	t<500ms	VSATFD1-2	-1	40	V
5	Input voltage MOSI, CSB, SCK, MISO SAT_SYNC, CLK, RESETB, TEST, TESTBUS, REXT		VMOSI, VCSB, VSCK, VMISO VSAT_SYNC, VCLK, VRESETB, VTEST, VTESTBUS, VREXT	-0,3	VCC+0.3V	V
6	Input voltage V3_3			-0.3	3.8	V
7	Input voltage VCC		VCC	-0.3	6	V
8	Junction Temperature		T_J		150	°C
9	Thermal Resistance (junction–ambient) QFN20L5		R_{TJA}		23 1)	K/W
10	Operating Temperature ambient		T_{AMB}	-40	125	°C
11	Storage Temperature		T_{STG}	-55	150	°C

All voltages referred to DGND, AGND1, AGND2, All GND-pins have to be shorted
1) Value is based on method according to JEDEC standard JESD-51-5

3.2 Recommended Operating Conditions

Parameters are guaranteed within the range of operating conditions unless otherwise specified. All voltages are referred to GND, currents are specified positive, when flowing into the node, negative when flowing out of the node.

3.2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Bus voltage (normal mode)	$V_{SAT\_BUS\_SUP}$	8.5	25	V
Bus voltage (increased mode)	$V_{SAT\_BUS\_SUP}$	10	25	V
Sync pulse voltage (standard)	$V_{SAT\_SYNC\_SUP\_STD}$	14	35	V
Sync pulse voltage (increased)	$V_{SAT\_SYNC\_SUP\_INC}$	15.5	35	V
Oscillator frequency	CLK	3.92/7.84	4.08/8.16	MHz
VCC voltage (5V)	VCC_5V	4,5	5.5	V
VCC voltage (3V)	VCC_3V	3	3.6	V
Capacitance V3_3	C_{V3_3}	33	330	nF
SAT_SYNC duration time	$t_{SAT\_SYNC\_Duration}$	5	-	µs
External resistor Rext ①	REXT	9.7	10.3	kOhm

①REXT determines the short circuit currents and the data current threshold. All related parameters are specified for REXT=10k+/-3%. A variation of +/-3% is assumed over temperature/ lifetime. This variation will shift the above mentioned parameters accordingly.

3.2.2 Operating Conditions for Synchronous Parallel Bus Mode (PSI5-P10P-500/3L)

Parameter	Symbol	Min.	Typ.	Max.	unit.
ECU Bus capacitance	CE+CEopt	15		35	nF
ECU resistance	RE	5		12	Ω
ECU Bus capacitance	CEopt	0	22	-	nF
Satellite capacitance	CS	9	-	24	nF
Total Bus capacitance	CE+CSx (x=1...3)	24	-	107	nF
ECU connector resistance	RCE	-	0.2	-	Ω
Satellite connector resistance	RCS	-	0.2	-	Ω
Single wire resistance	RW/2	-	0.5	-	Ω
Overall wire resistance incl. wire	2*(RCE+RW/2+RCS)	-	-	2.5	Ω
Wire inductance	LW	-	-	8.7	µH
Wire capacitance	CW	-	-	600	pF
Sync signal period	T_{SYNC}	495	500	505	µs
Satellite bit rate functional range	$F_{SAT\_FUNC} = 1/T_{BIT}$	119	125	132	kHz
Satellite bit duty cycle	DC	47	50	53	%
Slot 1 start time (see figure 5.1-6)	t_{Slot1_Start}	44	-	-	µs
Slot 1 end time				170.8	µs
Gap time (see figure 5.1-6)	$T_{GAP>} T_{BIT}$	8,4	-	-	µs
Slot 2 start time (see figure 5.1-6)	t_{Slot2_Start}	177	181.3	-	µs
Slot 2 end time				318.4	µs
Slot 3 start time (see figure 5.1-6)	t_{Slot3_Start}	322	328.9	-	µs
Slot 3 end time (see figure 5.1-6)	t_{Slot3_End}	-	-	492	µs
Satellite quiescent current range	$I_{SAT\_Q\_range}$	-35	-	-4	mA
Satellite modulation current range	$I_{SAT\_mod\_range}$	-30	-26	-22	mA

① CE: ECU connector capacitance, CE+CEopt >22nF needed to ensure system-level ESD performance,

② RE: series resistor, improves damping in case of long wires and large inductive loads,

③ CEopt: capacitor at IC-pin, removes oscillations in short circuit conditions, min. and max. values for CE, RE, CEopt needed to be in accordance to PSI-5 specification.

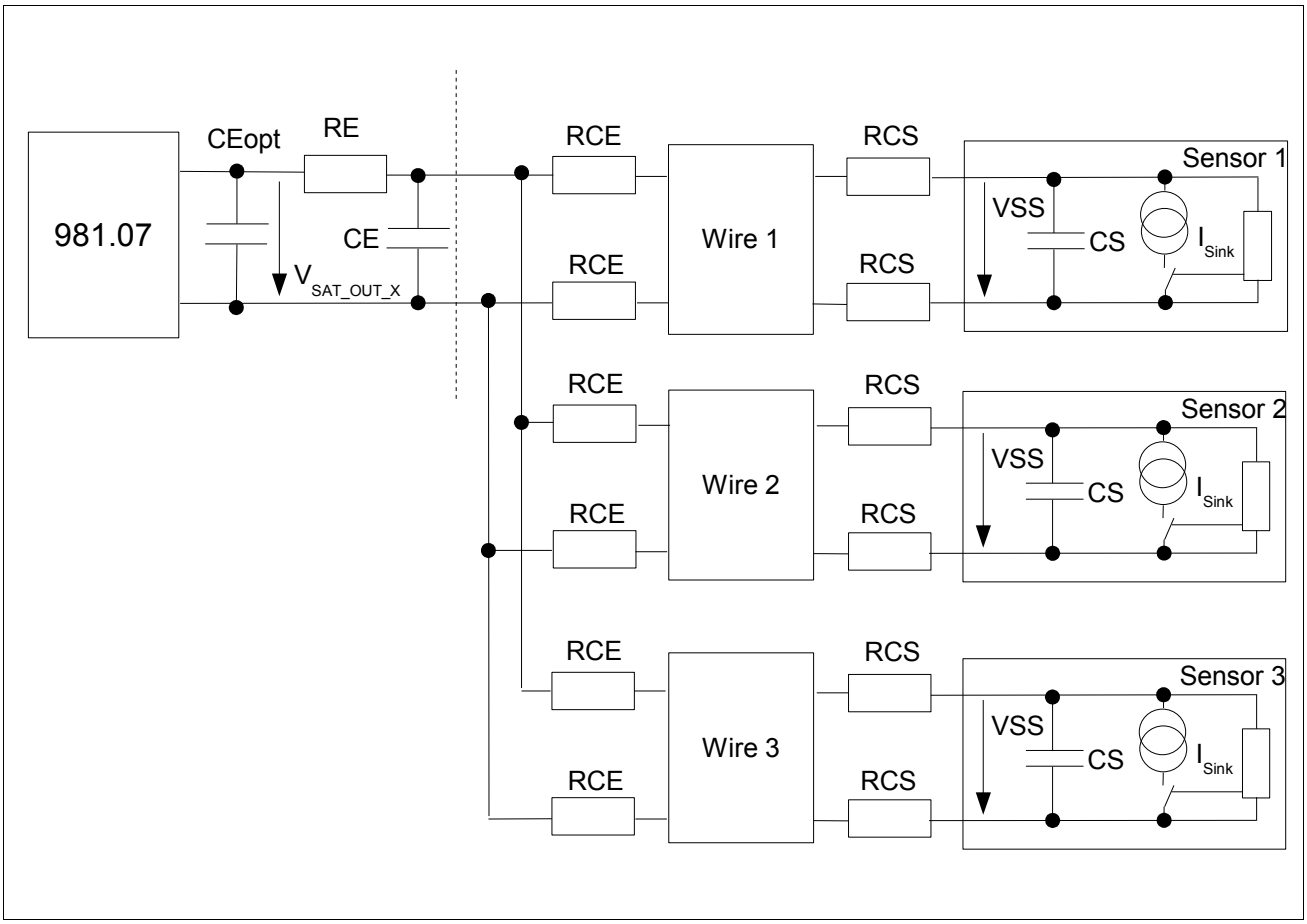


Figure 3.2-1 Application for Synchronous Parallel Bus Mode (PSI5-P10P-500/3L)

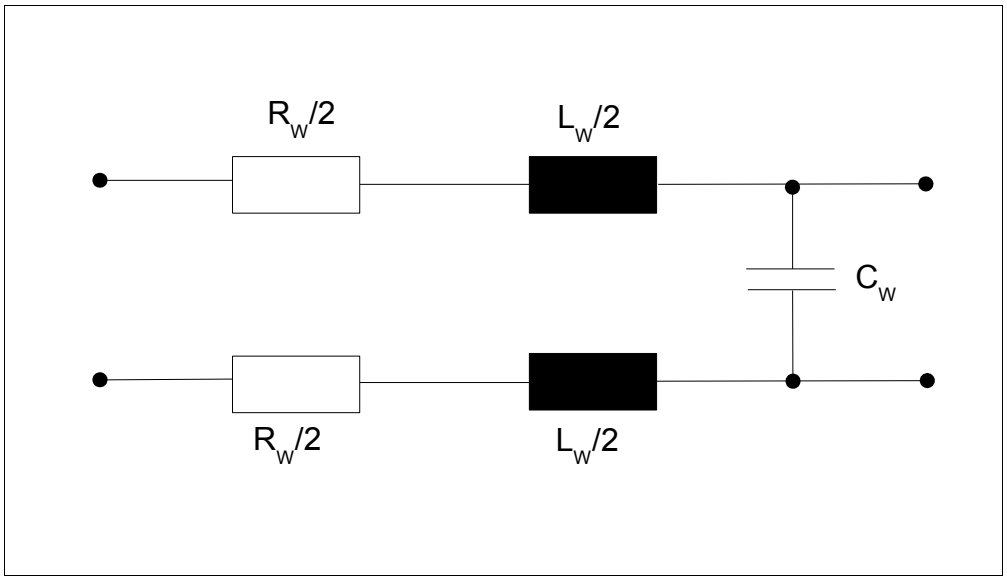


Figure 3.2-2 Wire substitution circuit

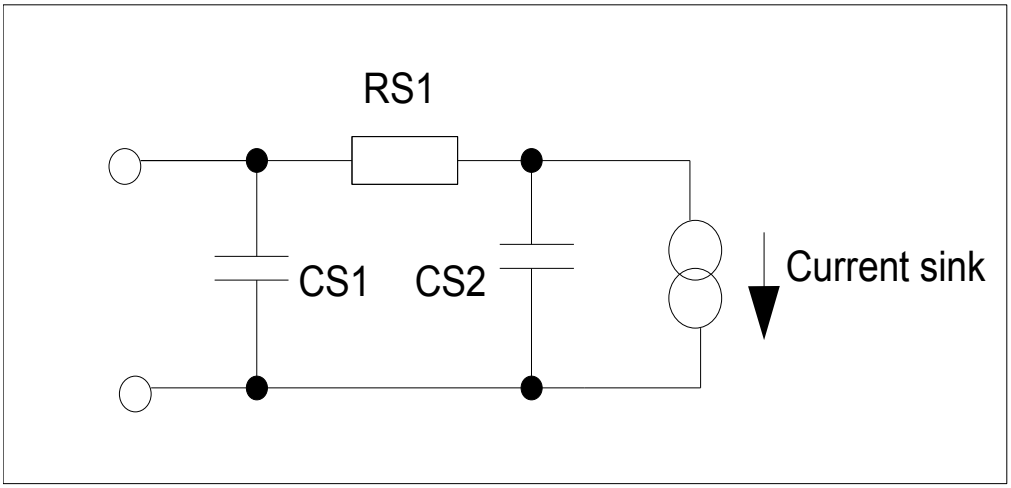


Figure 3.2-3 sensor substitution circuit

4 Detailed Electrical Specification

4.1 DC Parameter

4.1.1 Analogue Voltage Power Supply and Biasing Circuit

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Quiescent current consumption	$ISUP_{Quies.}$	$I_{SAT\_BUS\_Q}+I_{SAT\_SYNC\_Q}+I_{SAT\_VCC\_Q}$ Interfaces off	-	3	4	mA
2	Current consumption operating	$ISUP_{Op.}$	$I_{SAT\_BUS}+I_{SAT\_SYNC}+I_{SAT\_VCC}$ Interfaces on	-	7	10	mA
3	BUS quiescent current consumption	$I_{SAT\_BUS\_Q}$	Interfaces off	-	1	2	mA
4	BUS current consumption operating	I_{SAT_BUS}	Without load	-	3.5	6	mA
5	BUS current consumption operating	I_{SAT_BUS}	With load, $0<I_{SAT\_FDX}<65mA$ (load current to be added) with /without sync pulse		3.5	6	mA
6	SYNC quiescent current consumption	$I_{SAT\_SYNC\_Q}$	Without load, no sync-pulse, all interfaces on, no load	-	0.6	1	mA
7	SYNC current consumption operating	I_{SAT_SYNC}	Average current, all interfaces active, no load, 500µs Sync-cycle	-	0.7	2	mA
8	SYNC current consumption operating	I_{SAT_SYNC}	Average current, all interfaces active, $I_{SAT\_FDX}<35mA$, 500µs Sync-cycle (load current at SATFDx 2*35mA included, no cap. load) ②	-	3.5	4.8	mA
9	SYNC current consumption operating	I_{SAT_SYNC}	Dynamic (load current of C_{Bus}=100nF) ①		150		mA

① Not tested in production

② The SATFDx pin is supplied by VSYNC for 20µs (if VSYNC is larger VBUS, otherwise VBUS is always delivering the current), the average current consumption from VSYNC due to the load current can be calculated (here for 500µs sync-periode) by 20µs/500µs * load current * number of interfaces. A capacitive load increases the current consumption at VSYNC due to the charging of the bus-capacitance. The additional charging current can be calculated as follows: $I_{charging}$ = number of channels * V_{delta}* C_{load}/500µs; V_{delta}: sync pulse amplitude, about 5V)

4.1.2 Digital Voltage Power Supply

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Quiescent current consumption	$I_{SAT\_VCC\_Q}$	no CLK	-		1	mA
2	Logic supply operating current	I_{SAT_VCC}	CLK=4MHz/8MHz	-		2	mA

4.1.3 Channel Interface Parameter

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Interface DC output voltage (standard) (programmable via SPI)	$V_{SAT\_OUT\_X}$	$I_{SAT\_FDX} \leq 65mA$,	6	6,5	7	V
2	Interface DC output voltage (increased) (programmable via SPI)	$V_{SAT\_OUT\_X}$	$I_{SAT\_FDX} \leq 65mA$, $VBUS_{min} = 10V$	7,5	8	8,5	V
3	Interface DC output voltage in disabled state	$V_{SAT\_OUT\_X\_DIS}$		-		0,5	V
4	Interface ripple rejection from V_{BUS_SUP}	PSRR V_{BUS_SUP}	$50kHz \leq f_{Ripple} \leq 280kHz$, $I_{SAT\_FDX}<35mA$ CEopt=22nF, RE=5Ohm, CE=2.2nF, CS1=2nF, RS=5Ohm, CS2=15nF ①	23		-	dB
5	Interface ripple rejection from V_{BUS_SUP}	PSRR V_{BUS_SUP}	$280kHz \leq f_{Ripple} \leq 560kHz$ $I_{SAT\_FDX}<35mA$ ①	20		-	dB
6	Interface ripple voltage due to satellite current modulation	V_{SAT_RIPPLE}	① RE=5Ohm, CE=35nF, L=8,7µH, IQ=4mA, CS1 =2nF, RS=5Ohm, CS2=15nF			260	mV_{PP}
7	RSU regulator output current range	I_{SAT}	③	-65		0	mA
8	RSU output current limitation	I_{SAT_OCL}	REXT=10kOhm +/-3%	-130	-110	-85	mA
9	Satellite quiescent current measurement range	$I_{SAT\_Q\_range}$	REXT=10kOhm +/-3% ③	-37		-2	mA
10	Satellite quiescent current measurement accuracy	$I_{SAT\_Q\_acc}$	① REXT=10kOhm +/-3%	-1	-0,4		mA
11	Data comparator threshold current range	$I_{SAT\_TH\_RANGE}$	REXT=10kOhm +/-3%	-54,5		-2	mA
12	Data comparator threshold	$I_{SAT\_TH\_R}$	Data current rising REXT=10kOhm +/-3%	-17,5	-14,5	-11,5	mA

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
13	Data comparator threshold	$I_{SAT\_TH\_F}$	Data current falling REXT=10kOhm +/-3%	-14,5	-11,5	-8,5	mA
14	Data detection current hysteresis	$I_{SAT\_TH\_HYST}$	REXT=10kOhm +/-3%	-4	-3	-2	mA
15	SATFDX pull down current limit (discharge current of the line capacitor)	I_{SAT_PD}	REXT=10kOhm +/-3%	35	55	75	mA

① Not tested in production
③ Interface will be switched off, if the quiescent current exceeds the upper limit, debouncing some 10ms due to the settling speed of the adaptive threshold, HE bit will be set, see also 5.2.5.5 for all switch-off conditions

4.1.4 Sync Pulse Generation

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Sync pulse absolute voltage (standard)	$V_{SAT\_OUT\_X\_MAX}$		10,5	11,5	12,5	V
2	Sync pulse absolute voltage (increased)	$V_{SAT\_OUT\_X\_MAX}$		12	13	14	V
3	Sync signal sustain voltage		See Figure 5.1-3	$V_{SAT\_OUT\_X}$ + 4.3V	$V_{SAT\_OUT\_X}$ + 4.9V	$V_{SAT\_OUT\_X}$ + 5.5V	

4.1.5 Reference Voltage REXT

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Reference Voltage	Vref	REXT=10kOhm	1,18	1.23	1,3	V
2	Short circuit current		REXT=0	-1	-0,5		mA

The following parameters are directly depending on REXT: 4.1.3.8-15, i.e. pull up current limitation, pull down current limitation, data threshold and hysteresis, and quiescent current measurement range

4.1.6 Digital Inputs and Outputs SPI

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input threshold LOW MOSI, CSB, SCK,	V_{THMOSI_L} V_{THCSB_L} V_{THSCK_L}		0.8	-	-	V
2	Input threshold HIGH MOSI, CSB, SCK,	V_{THMOSI_H} V_{THCSB_H} V_{THSCK_H}		-	-	2.0	V
3	Output voltage LOW MISO	$V_{OUTMISO\_L}$	Iout=0.5mA	-	-	0.4	V
4	Output voltage HIGH MISO	$V_{OUTMISO\_H}$	Iout=-0.2mA	VCC-0.4	-	-	V
5	Pull-up-resistor CSB			100	150	200	kΩ

4.1.7 External Oscillator (CLK)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input threshold LOW CLK	V_{THCLK_L}		0.8	-	-	V
2	Input threshold HIGH CLK	V_{THCLK_H}		-	-	2.0	V
3	Pull-down-resistor CLK			100	150	200	kΩ

4.1.8 Power On Reset

The power-on-reset is only related to V3_3.

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Reset threshold high	V_{POR_R}	V3_3 rising,②			2.85	V
2	Reset threshold low	V_{POR_F}	V3_3 falling,②	2.4			V
3	Hysteresis	V_{POR_HYST}	①		0.05		V

① Not tested in production

② VPOR_F/R is defined for VBUS/VSYNC down to 0V. VCC=V3_§ (in V5 and 3.3V supply mode)

4.1.9 External Reset

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input threshold LOW RESETB	$V_{THRESETB\_L}$		0.8	-	-	V
2	Input threshold HIGH RESETB	$V_{THRESETB\_H}$		-	-	2.0	V
3	Pull-down-resistor RESETB			100	150	200	kΩ

4.1.10 Trigger Signal for Sync Pulse

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input threshold LOW SAT_SYNC	V_{THSYNC_L}		0.8	-	-	V
2	Input threshold HIGH SAT_SYNC	V_{THSYNC_H}		-	-	2.0	V
3	Pull-down-resistor SAT_SYNC			100	150	200	kΩ

4.1.11 REXT Check

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Resistor at Pin REXT too low	REXT	①			1	kΩ
2	Resistor at Pin REXT too high	REXT	①	30			kΩ

① Hardware error bit will be set if REXT is lower 1kOhm or larger 30kOhm, the interfaces will be switched off

4.1.12 VSATFDx over-voltage protection

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Voltage at pin SATFDX out of range	$V_{SAT\_OUT\_X\_OOR\_STD}$	Standard mode ①	7.5		9.5	V
2	Voltage at pin SATFDX out of range	$V_{SAT\_OUT\_X\_OOR\_inc}$	Increased mode ①	9		11	V
3	Pull-down current at SATFD too large		②	35		70	mA

① Hardware error bit is set if the voltage at SATFDX is above the specified values. The hardware error bit is also set if the pull-down current is above the specified value. The affected interfaces will be switched off.

② Will be activated at 0.5V above the output voltage SATFDX. After a debouncing time of 512µs, the channel will be switched off (see table in chapter 5.2.5.5

4.1.13 Supply_Check

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	VBUS ①	$V_{VBUS\_too\_LOW}$		6	7	8.3	V
2	VSYNC ①	$V_{VSYNC\_too\_LOW}$		10	11	12	V

①Hardware error bit will be set if the voltages are below the specified values. Interfaces will be switched off

4.2 AC Parameter

4.2.1 Channel Interface Parameters

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1a	Interface (high/low-side) over current start up delay	$t_{SAT\_OC\_SDEL\_ST}$	standard mode (SV=0) ③	5.12 $-T_{CLK}$	5.12	5.12 $+T_{CLK}$	ms
1b	Interface (high/low side) over current start up delay	$t_{SAT\_OC\_SDEL\_IN}$	increased mode (SV=1) ③	10.24 $-T_{CLK}$	10.24	10.24 $+T_{CLK}$	ms
2a	Interface high side over current shut down delay	$t_{SAT\_OC\_ODEL\_ST}$	standard mode (SV=0) ③ short to GND	512 $-T_{CLK}$	512	512 $+T_{CLK}$	µs
2b	Interface high side over current shut down delay	$t_{SAT\_OC\_ODEL\_IN}$	increased mode (SV=1) ③ short to GND	10.24 $-T_{CLK}$	10.24	10.24 $+T_{CLK}$	ms
3	Interface low side over current shut down delay	$t_{SAT\_OC\_ODEL\_LS}$	short to battery ③	512 $-T_{CLK}$	512	512 $+T_{CLK}$	µs
4	Data detection delay difference between negative and positive edge	$t_{SAT\_TH\_DEL\_DELTA}$	②	-	-	250	ns
5	Sync pulse delay first slot	$t_{SAT\_Sync\_Delay}$	See figure 5.1-6, ①	2.0	-	4	µs
6	Sync pulse jitter	t_{jitter}	See figure 5.1-6, ② ③	0	-	250	ns
7	REXT out of range debouncing	t_{OOR_DEB}		-	512	-	µs
8a	VBUS/VSYNC too low delay		after power-on reset, depends on internal clock $f_{OSC\_}$ (see 4.2.4.1)	0.57	0.85	2.0	ms
8b	VBUS/VSYNC too low delay		interface operating, depends on external clock CLK (see 3.2.1.8)	-	32	-	µs

① The parameter $t_{SAT\_Sync\_Delay}$ will be measured from the rising edge of the SAT_SYNC signal ($t_{SAT\_Sync\_start}$) until the voltage at SATFDX is equal Vt0 (Vt0=VSATFDX+0.5V). See figures 5.1-4 and 5.1-6 .

②Not tested in production

③ T_{CLK}= 250 ns plus external clock tolerance

4.2.2 Sync Pulse Generation

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Sync Pulse rise time with resistive load	$t_{SAT\_SYNC\_rise}$	Transition from 10% to 90% of pulse amplitude, C=14.7nF, Rload=400Ω	3	4	6	µs
2	Sync slope slew rate rise	t_{SL_rise}	See Figure 5.1-4 24nF < $C_{BUS, max}$ <107nF, 4mA<I_{SAT_Q} <35mA ①	0.43	1	1.5	V/µs
3	Sync slope slew rate fall	t_{SL_fall}	See Figure 5.1-4	-1.5	-1		V/µs
4	Delay time of the satellite interfaces	t_{SYNC_DEL}	programmable in steps of 0.5 µs+/-250ns default is 4 µs, see figure 5.1-6 and chapter 5.2.6.2.5	3.75	4	4.25	µs

① Note that the slew rate is dependent on the external capacitor and the difference of the load current and the current limitation 4.1.3.8 (I=C*du/dt).
Measurement condition: ($V_{SAT\_OUT\_X}$(@Vt2=3.5V)-$V_{SAT\_OUT\_X}$(@Vt0=0.5))/ (t2-t0) See Figure 5.1-4

4.2.3 Digital Outputs SPI

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Data output access time MISO	t_a	C=<80pF①	-	-	35	ns
2	Data output (MISO) valid after SCK	t_{V_5V}	C=<80pF, VCC=5V① ②	-	-	30	ns
2a	Data output (MISO) valid after SCK	t_{V_3V3}	C=<50pF, VCC=3.3V① ③	-	-	30	ns
2b	Data output (MISO) valid after SCK	t_{V_3V3}	C=<80pF, VCC=3.3V① ③	-	-	45	ns
2c	Data output (MISO) valid after SCK	t_{V_3V3}	C=<50pF, VCC=5V① ③	-	-	23	ns
3	Data output (MISO) lag time	t_{MISO_lag}	C=<80pF①	0	-	-	ns
4	Data output (MISO) disable time	t_{dis}	C=<80pF① ④	-	-	50	ns

① to be tested by appropriate SPI-protocols during production test
②SCK input 2.4V/0.4V; MISO 10% / 90% of VCC
③ SCK input 2.4V/0.4V; MISO 20% / 80% of VCC
④ Measurement condition: 1k Pull-Up resp. Pull-down resistor on pin MISO. Measurement from 90%CSB to 10%MISO rise, resp. 90% MISO fall (see Figure 5.2-4)

4.2.4 General SPI operating conditions

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SPI clock (SCK) operating frequency	f_{SCK}	①	-		8.1	MHz
2	SPI clock (SCK) period	t_{SCK}	①	123,4		-	ns
3	Clock (SCK) high time	t_{SCKH}	①	47,5		-	ns
4	Clock (SCK) low time	t_{SCKL}	①	47,5		-	ns
5	Clock (SCK) fall time	t_{fall}	①	0		13	ns
6	Clock (SCK) rise time	t_{rise}	①	0		13	ns
7	Data input setup time	t_{setup}	①	12.5		-	ns
8	Data input hold time	t_{hold}	①	30		-	ns
9	Enable (CSB) lead time	t_{lead}	①	61,8		-	ns
10	Enable (CSB) lag time	t_{CSB_lag}	①	61,8		-	ns
11	Sequential transfer delay	t_{td}	①	371,1		-	ns
12	Capacitive load at SPI pins MISO	C_{MISO}	①	-		80	pF

① These timings are given by the MCU. The IC`s SPI circuit is designed to be fully operational under these worse case timings. SPI functionality test at WC timings is done during production test.

4.2.5 Internal Oscillator

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Oscillator frequency	f_{OSC}		0,5	1,2	1,8	MHz

4.2.6 Over Temperature Switch Off

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Switch off threshold	T_{OFF}	①,②		170		°C
2	Switch on threshold	T_{ON}	②		160		°C
3	Hysteresis		②		10		°C

① When the temperature switch off threshold of the affected channel, the hardware error bit will be set and the corresponding interface will be switched off.
②Not tested in production

5 Functional Description

5.1 RSU Interface

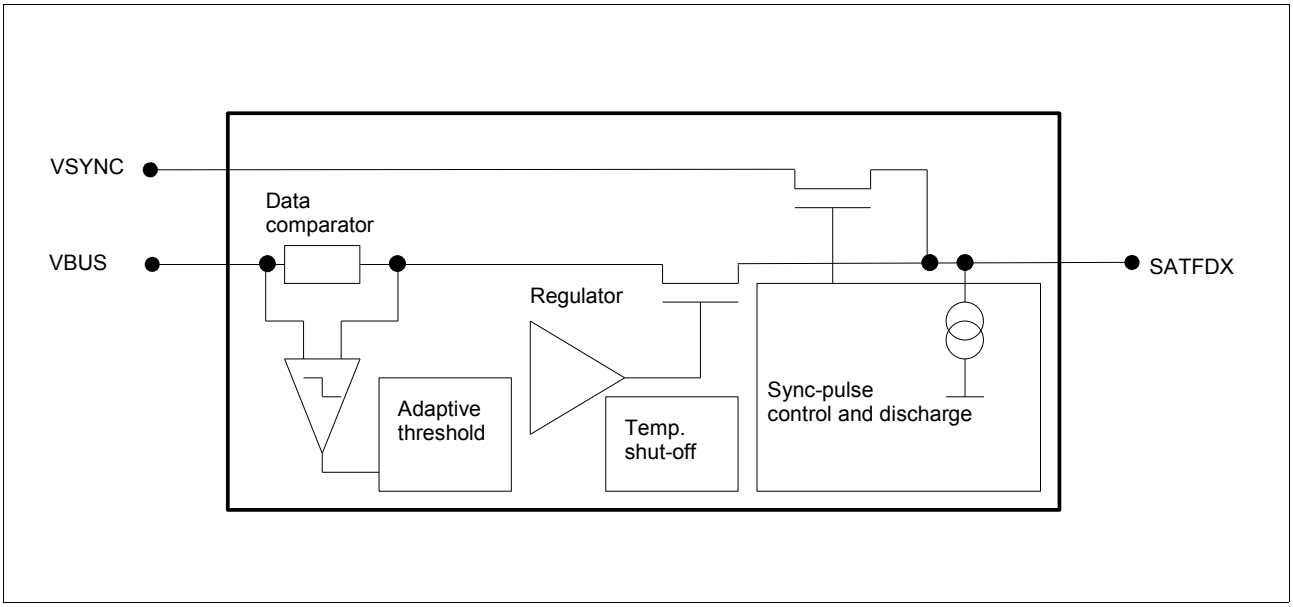


Figure 5.1-1 Satellite Interface Block Diagram

5.1.1 Functional Description

Each of the four RSU interfaces provides a regulated voltage to the connected satellite sensor. The interfaces are short circuit protected to 40V and GND. The four interfaces operate independently. Distortion on one channel will not effect the operation of the others.
The RSU interfaces can be activated and deactivated independently via an SPI command. Because enabling a channel results an in-rush current on the line, any time a channel is activated, a startup delay counter is started. During this entire delay time $t_{SAT\_OC\_SDEL}$ the Manchester Decoder, the sync pulse generation and the over-current detection for the particular channel are disabled. When the startup delay counter expires, the channel enters its normal operating mode.

5.1.2 Voltage Regulation

The voltage regulator provides 2 different voltage settings: In the “standard” mode, the regulator provides 6.5V. This mode is intended to be used for universal ana parallel configuration. In “increased” mode the regulator provides an 8V supply. This mode is intended to be used for daisy-chain configuration. The selection is done by the SPI-command “LINE_SUPPLY_MODE”.

5.1.3 Current Comparator

The satellite sensors modulate the current through the RSU line, in order to realise a Manchester coded data transmission.
The “low” level of the current is represented by the quiescent current $I_{SAT\_Q\_range}$ of the sensors, while a “high” level is created by switching on a current sink to the line, which increases the current to I_{SAT_OP} (see Figure 5.1-2).
A current transition in the middle of the bit time represents the logical value of the transferred data. A “high current-low current” transition stand for a logical '1', a “low current-high current” transition for a logical '0'.
This current can be detected by measuring the voltage drop via an internal shunt. The current threshold is automatically adapted to the quiescent current of the sensors in each RSU line.

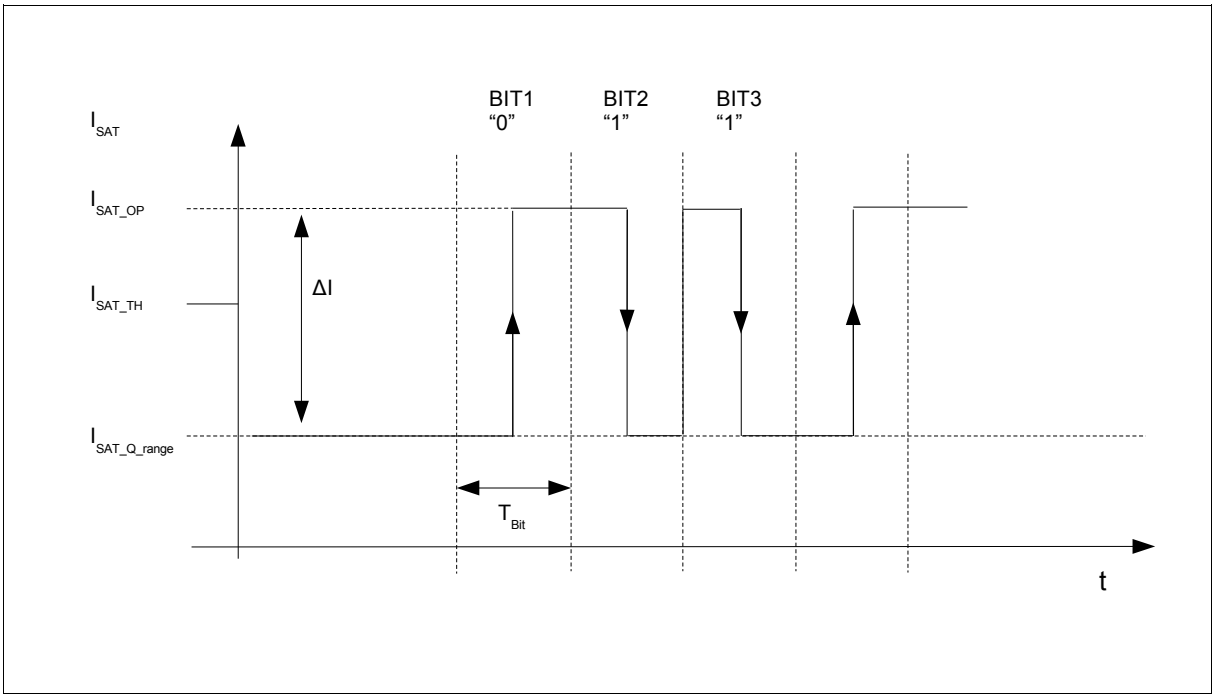


Figure 5.1-2 Current During Operation

5.1.4 Sync Pulse Generation

Each data transmission is initiated by a synchronisation signal generated by the device. The MCU will provide a trigger signal SAT_SYNC, which initiates the device to rise the voltage on the bus from typically 6.5V to typically 11.5 V (resp. 8V to 13V) slew rate controlled for a time of typically 23 µs. The Figure 5.1-3 shows the timing of the sync pulse generation.

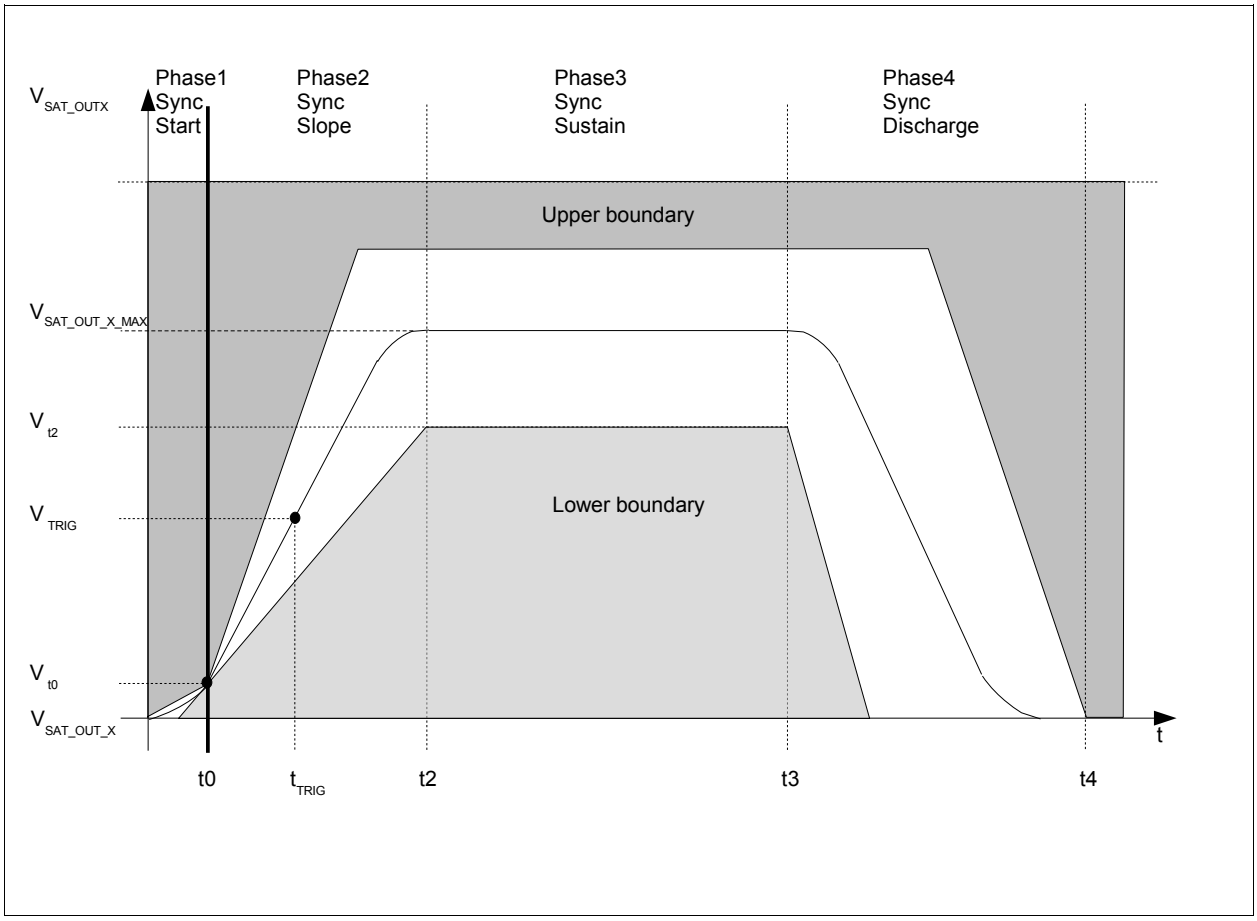


Figure 5.1-3 Synchronisation Pulse Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sync signal start	t_0	@V_{t0} =0.5V		0		µs
Sync signal sustain start	t_2	@V_{t2} =3.5V		7		µs
Sync signal sustain time	t_3			16		µs
Discharge time limit	t_4			35		µs
Sync rise time	t_{SYNC_rise}			4.6		µs

5.1.5 Current Limitation

The circuit provides an over current protection of the RSU interfaces. When the current measured by the current comparator exceeds typically 100 mA, the error flag HE is set and the voltage will be turned off after a delay $T_{sat\_oc\_del\_xx}$. To allow “in-rush” current when the channel is turned ON the error condition is masked for $T_{sat\_oc\_sdel\_xx}$. During this delay, the HE-bit is not set. (xx refers to supply mode: “standard” or “increased”: refer to §4.2.1-1a,1b, 2a, 2b)

5.1.6 Over Voltage Protection

The RSU interfaces are voltage protected against 40V. When the output voltage increases to 0.5V above the nominal voltage, a pull down current is activated (see 4. 1.12.3) . When the current reaches the specified limit the error flag OE is set and the voltage will be turned off after a delay $T_{sat\_oc\_odel\_ls}$. If a short to V+ occurs prior to the channel activation the error condition is masked for a delay $T_{sat\_oc\_sdel\_xx}$). During this delay the OE bit is not set. (xx refers to supply-mode: “standard” or “increased”: refer to §4.2.1, 1a, .1b, 3)

5.1.7 Synchronous Parallel Bus Mode (PSI5-P10P-500/3L)

In parallel bus mode application, the sensors are connected in parallel to the bus line like shown in Figure 5.1-4. It is possible to connect up to three sensor to each channel of the 981.07. The sync cycle time is 500µs with a data transmission rate of 125kbit/s. The synchronisation pulse for the satellite channel feeds SATFD1-SATFD2 can be activated by MCU via the SAT_SYNC pin of the device. When a rising edge is detected, the 981.07 outputs sync pulses on channels SATFD1-SATFD2 in sequence to reduce the average current inrush to the satellites as shown in Figure 5.1-5. The satellites can transmit from one to three messages per sync pulse received. The Figure 5.1-6 shows the timing for one channel.

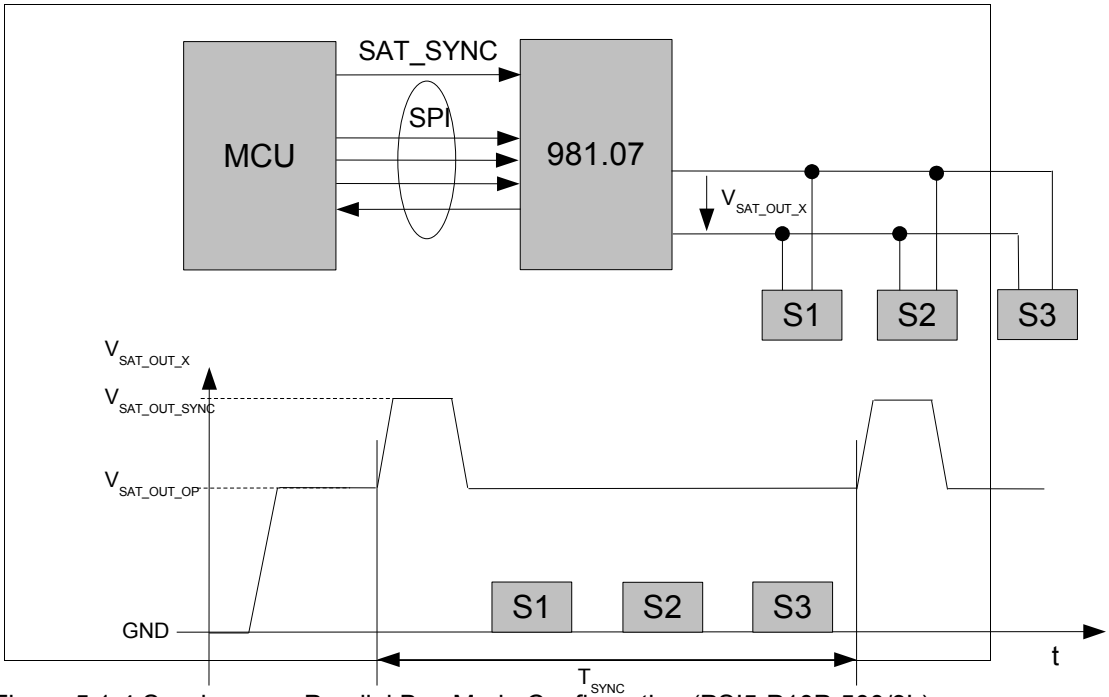


Figure 5.1-4 Synchronous Parallel Bus Mode Configuration (PSI5-P10P-500/3L)

In order to avoid EMC problems, the synchronisations pulses of the satellites will not be performed at the same time, but consecutively like it is shown in the figure below.

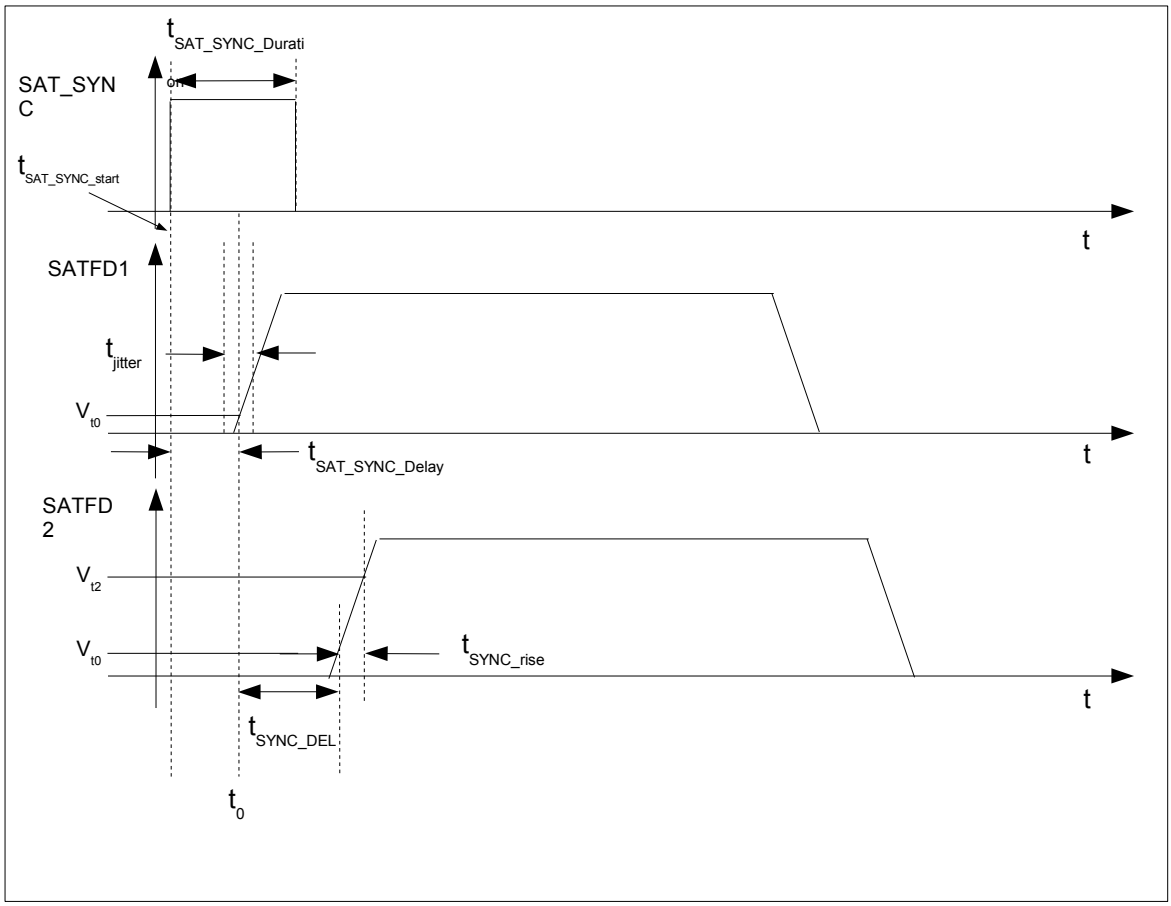


Figure 5.1-5 Satellite Synchronisation Pulses

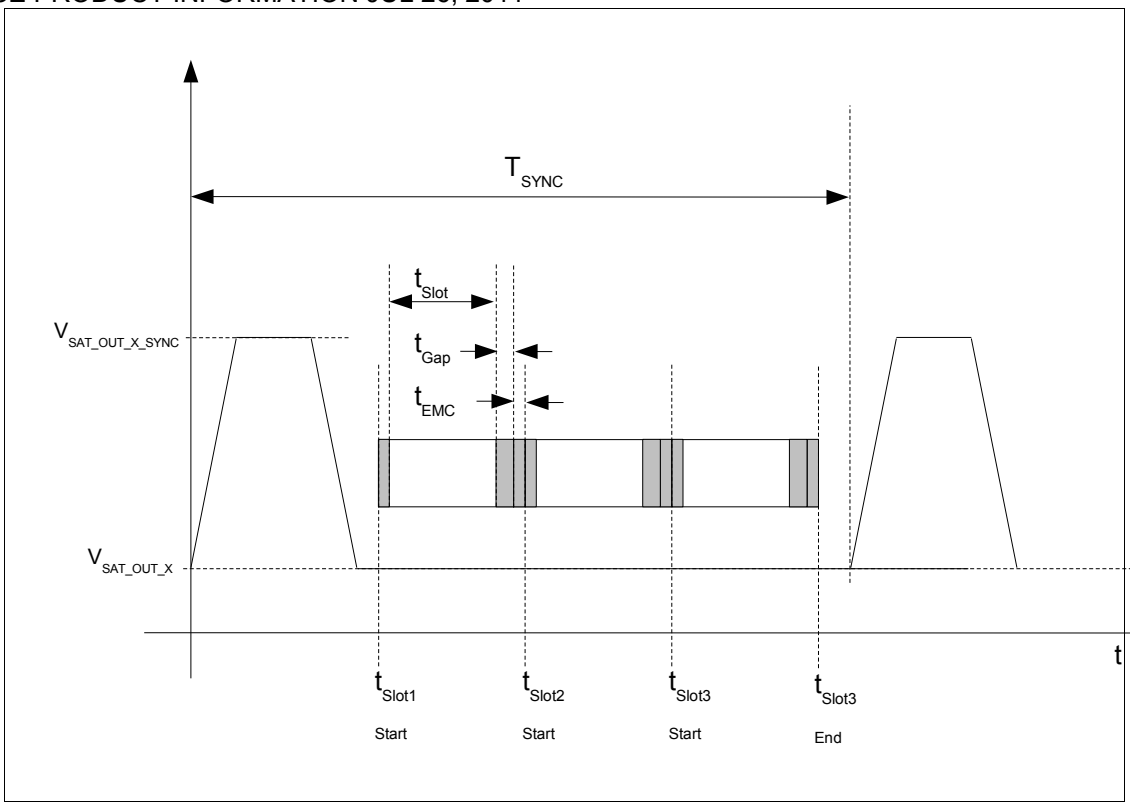


Figure 5.1-6 Timing for Synchronous Parallel Bus Mode (PSI5-P10P-500/3L)

5.1.8 Daisy chain bus mode (PSI5-D10P-500/3L)

The device is able to operate in Daisy chain bus configuration . In this configuration the sensors are connected in series (see figure 6.3/4). The chain contains switches, which can be used for auto addressing of the sensors. Because of a possible voltage drop, via the switches, it is recommended to program the device output voltage to 8V.

5.1.9 Bidirectional communication

In the above mentioned operating modes, it is possible to communicate, not only from sensor to ECU, but also from ECU to sensor. The communication from MCU to RSU is made using a specifiec sync-pattern (please refer to PSI-5 spec.) The sync-pattern is made using the SPI-command SYNC_ENABLE which allows masking the SYNC pulse independently on each SATFD output.

5.2 Control Logic

5.2.1 Block Diagram

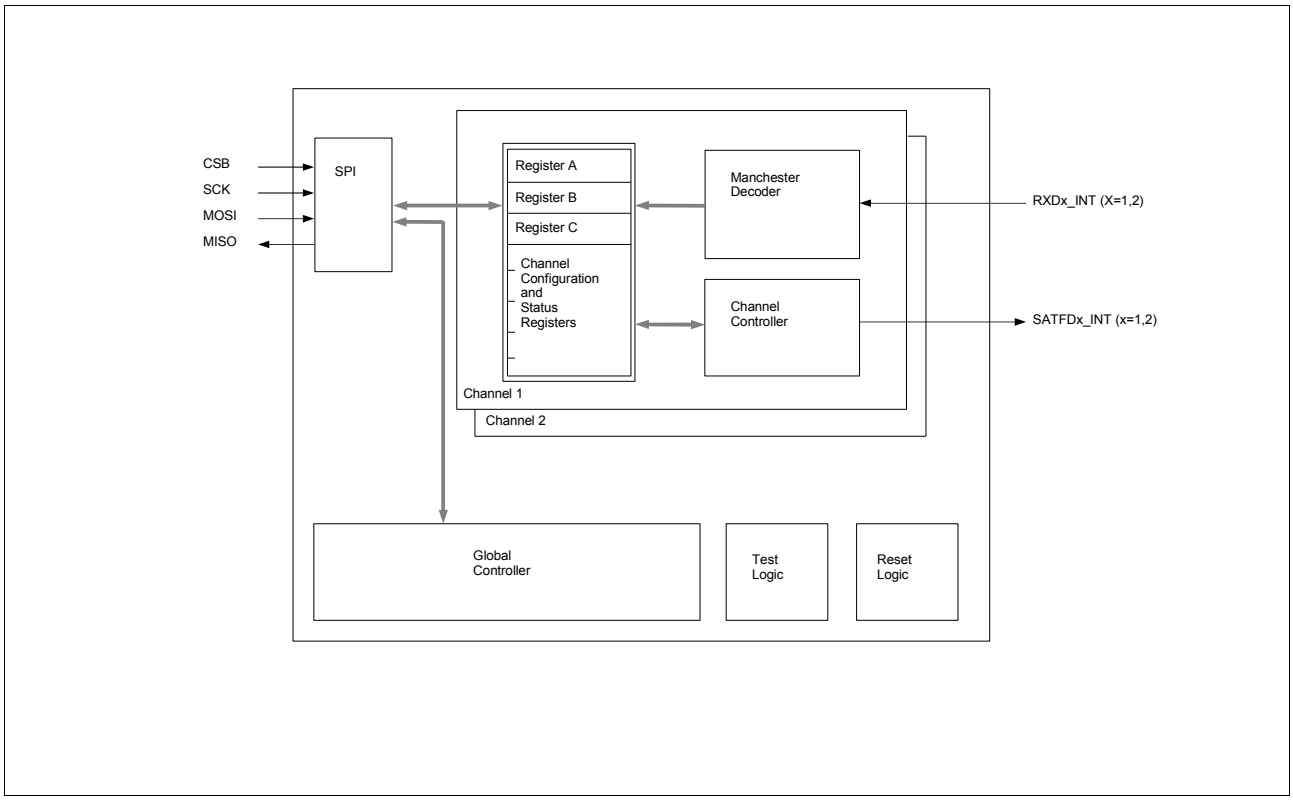


Figure 5.2-1 Block Diagram: Control Logic

5.2.2 Functional Description

The MCU and the 981.07 are communicating over an SPI bus in a master-slave operation mode. The MCU acts always as master and transmits commands over the MOSI (Master Out Slave In) line. The 981.07 acts always as slave and sends back status or RSU data to the MCU over the MISO (Master In Slave Out) line.

5.2.3 SPI Communication

The data transfer between the MCU and 981.07 is done serially with a four wire system:

Signal	Description	Direction
MOSI	Master Out Slave In	MCU ⇒ 981.07
MISO	Master In Slave Out	981.07 ⇒ MCU
SCK	Serial Clock	MCU ⇒ 981.07
CSB	Chip Select (low active)	MCU ⇒ 981.07

Bits are transmitted simultaneously to (MOSI) and from (MISO) the 981.07 when CSB is active (LOW) and each bit is synchronised by the clock SCK. The responses are transferred to the MCU in a single-stage pipeline fashion, where the response for a given request is transmitted in the frame immediately following the request as shown below in Figure 5.2-2.
Commands received during the transmission are executed by the 981.07 on the rising edge of CSB. Only commands with 16 clock cycles are executed.
Each transmission starts with a falling edge on CSB and ends with the rising edge. During the transmission command and data shift are controlled by SCK and CSB according to the following rules:

- Frame size is 16 bits
- Commands and data are shifted MSB first, LSB last
- Each bit is sampled on the rising edge of SCK (MOSI line)
- Each RSU-data-/status-bits is shifted out on the falling edge of SCK (MISO line)
- MISO becomes active during CSB='0' and is tristate during CSB='1'

Incoming commands are validated on the rising edge of CSB and executed in case that 16 clock cycles are counted during the transmission, glitches at CSB do not lead to a re-execution of the previous command.
The SPI is reset in case of power-on-reset or external reset.

The response on MISO to the first command after external reset or internal reset is a non-sensor data error response with RE bit is set, and the DU bit is cleared (RE=1, DU=0).

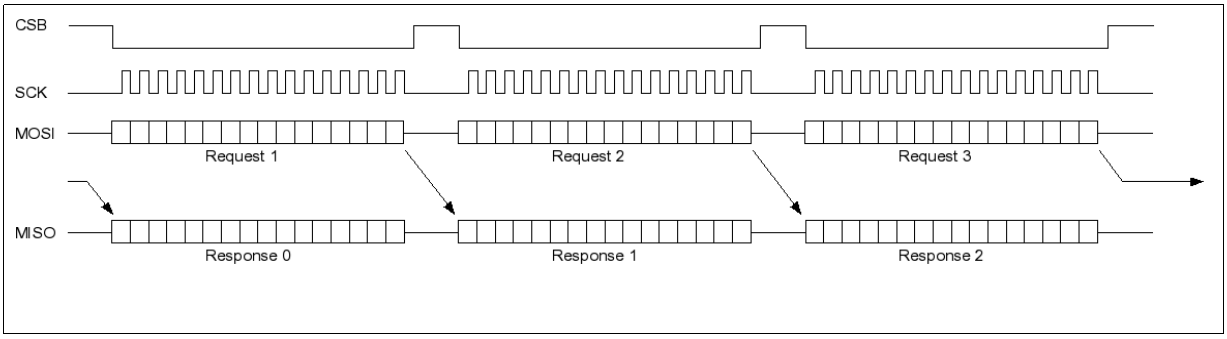


Figure 5.2-2: SPI Response Latency

5.2.4 SPI Timing

Figure 5.2-3 shows the SPI timing diagram.

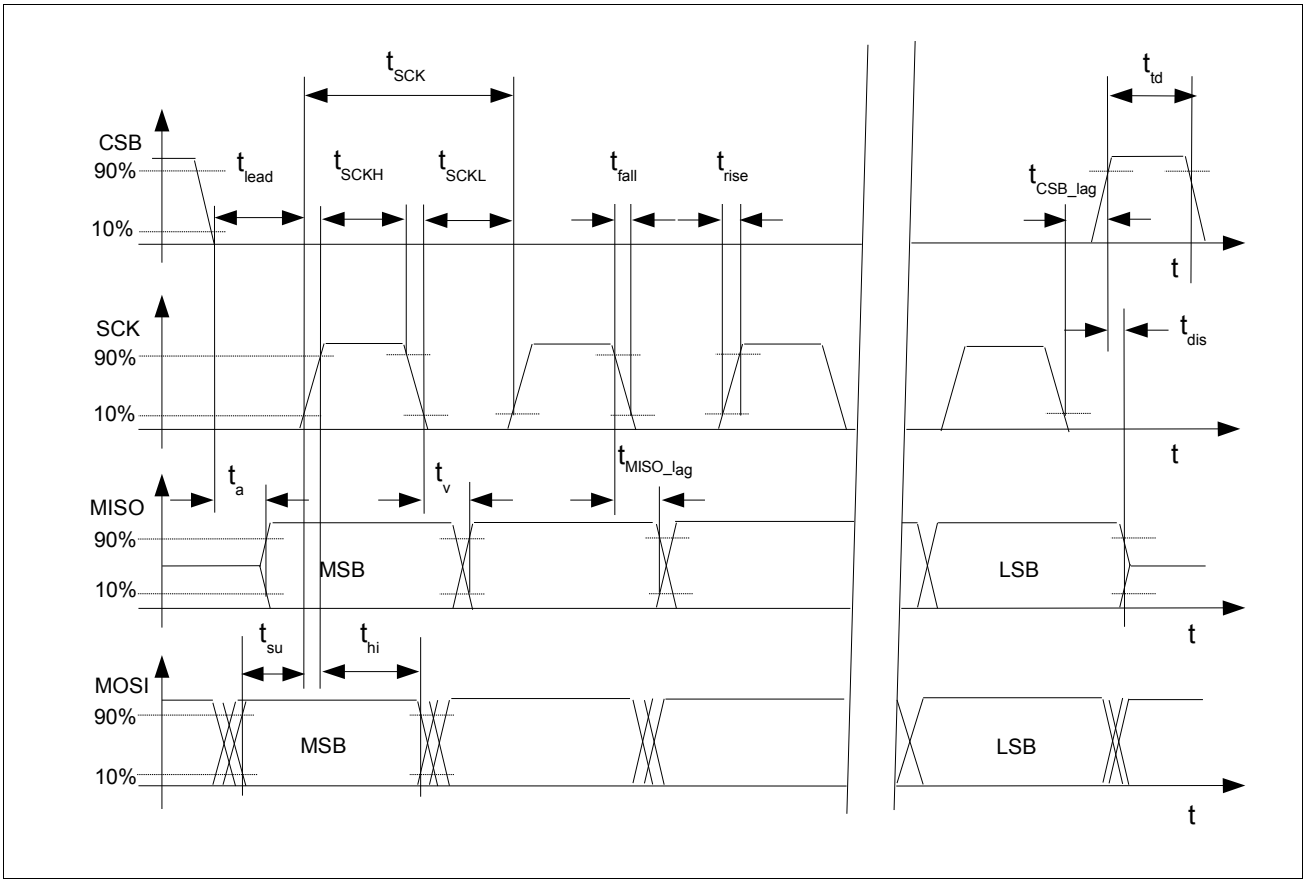


Figure 5.2-3: SPI Timing Diagram

5.2.5 SPI Message Format

The 981.07 supports two message types: a sensor related message type which is used to retrieve data from the connected sensors and another message type for non sensor requests like configuration and control information. The message type is defined by the bit 13 (SEN) in the MOSI request frame. The sequence identifier (SQx) bits are only used by the MCU for controlling purposes. The transmitted SQx bits are sent back by MISO during the following SPI-protocol.

5.2.5.1 SPI Sensor Data Request / Response Format

5.2.5.1.1 Sensor Data MOSI Request

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ1	SQ0	SEN	SQ2	0	0	0	0	0	0	0	0	LC3	LC2	LC1	LC0

5.2.5.1.2 Sensor Data MISO Response

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ2	SQ1	SQ0	P	ST1	ST0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Status Decode

↓	↓	
0	0	Unused
0	1	Sensor Data
1	0	Reserved
1	1	ES1 ES0 Exception Data

Exception status code

	↓	↓								
Slave error status	0	0	0	0	OE	ND	CNC	HE	ME	DE
Reserved	0	1	x	x	x	x	x	x	x	x
Reserved	1	0	x	x	x	x	x	x	x	x
Reserved	1	1	x	x	x	x	x	x	x	x

5.2.5.2 SPI Sensor Data Request / Response Bit Definitions

5.2.5.2.1 Sensor Data Request MOSI Bit Definition

Name	Bit position	Definition
SQ2:SQ0	15,14,12	Sequence Identifier-used for synchronising samples
SEN	13	Sensor Bit, defines request as Sensor data request or non sensor data request
LC3:LC0	3:0	Local channel select

5.2.5.2.2 Sensor Data Response MISO Bit Definition

Name	Bit position	Definition
SQ2:SQ0	15:13	Sequence Identifier-used for synchronising samples
P	12	Parity, Ensures odd parity for bits 15:0 of MISO
ST1:ST0	11:10	Status - identifies contents in D9:D0 of MISO (sensor data, self test data, error etc.)
ES1:ES0	9:8	Exception status – identifies contents of exception data (receiver/ on board sensor, error status or satellite error)
OE	5	Over current error, over current of low side driver (short to battery)
ND	4	No Data (channel specific): Sensor data not available
CNC	3	Condition not correct for operation (channel specific): as defined elsewhere Request cannot be fulfilled because channel is off, or in the wrong mode etc.
HE	2	Hardware Error in slave (channel/channel pair specific): caused by hardware errors defined elsewhere, such as over temperature, over current of high side driver (short to GND), reference out of range etc.
ME	1	Manchester Error (channel specific): incorrect number of bits, timing violation etc. in bit stream
DE	0	Data Error (channel specific): parity error in manchester data
D9:D0	9:0	Sensor data, for ST1:ST0=01

5.2.5.3 SPI Non Sensor Data Request / Response

5.2.5.3.1 Non Sensor Data MOSI Request

	MSB															LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OP1	OP0	SEN	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	↓	↓														
1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x
2	0	1	0	Write Address					Write Data							
3	1	0	0	Read Address					x	x	x	x	x	x	x	x
4	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x

1 Reserved
2 Write
3 Read
4 Test

5.2.5.3.2 Non Sensor Data MISO Response

	MSB															LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	OP1	OP0	P	ST1	ST0	ES1	ES0	D7	D6	D5	D4	D3	D2	D1	D0
		↓	↓													
1		0	0	P	1	1	1	0	0	0	0	0	0	SE	RE	DU
2		0	1	P	1	1	1	0	Slave Status							
3		1	0	P	1	1	1	0	Read Data							
4		1	1	P	1	1	1	0	x	x	x	x	x	x	x	x

1 Error Response
2 Write Response
3 Read Response
4 Test Response

5.2.5.4 Logical Channel Assignment

The Logical Channel field is used to address one of the six possible satellites connected to the two physical channels of the 981.07. Each physical channel can support up to three satellites. Each of these three satellites is assigned to a separate time slot on the bus. Each time slot has a appropriate sensor data register (A, B, C). The 981.07 response to requests for undefined physical channels with an error message with the CNC bit is set (CNC=1). This illustrated in the table below.

Logical Channel LC[3:0]	Physical Channel	Time Slot	Sensor Data Register
0000	1	1	A1
0001	1	2	B1
0010	1	3	C1
0011	undefined	-	-
0100	2	1	A2
0101	2	2	B2
0110	2	3	C2
other	undefined	-	-

5.2.5.5 Error and Status Bits

The conditions for setting and clearing of status bits in Sensor Data Request message are defined in the table below.

Bit	Description	Setting Condition	Clearing Condition	Channel Behaviour
OE	Over-current Error	Satellite channel short to V+ condition	• External reset • Internal reset • LINE_ENABLE command with LEx=0 (OFF) for the affected channel	Channel is deactivated
ND	No Data	• no sensor data arrived since enabling of the channel • second attempt to read sensor data from one logical channel, although no new sensor data has been received intermediately	Cleared after a new satellite data is received	None
CNC	Conditions Not Correct	• Request for undefined channel • request for a channel not yet turned on	• External reset • Internal reset • requesting an activated channel	None
HE	Hardware Error	• Satellite channel short to GND condition • Satellite average Iq too high • Channel over-temperature • REXT out of range • CLK malfunction • VSYNC too low • VBUS too low	• External reset • Internal reset • LINE_ENABLE command with LEx=0 (OFF) for the affected channel	Channel is deactivated
ME	Manchester Error	Improper manchester data: • Invalid bit count • Invalid bit timing	• External reset • Internal reset • Cleared when read	None
DE	Data Error	• Satellite Data Parity Error	• External reset • Internal reset • Cleared when read	None

The next tables summarises the error handling and the error priority.

Error	Logical channel activated	Logical channel defined, not activated	Undefined logical channel LC[3:0] "XX11"	Undefined logical channel LC[3:0] "1XXX"
Global ASIC HE (Clk, Rext missing, VBUS...)	HE cleared by clearing all LEx=0 and error source disappear	HE cleared by clearing all LEx and error source diappears	CNC	Not possible, CNC
Channel HE (SC to gnd ..)	HE cleared by clearing the corresponding LEx=0	Not possible, CNC	Not possible, CNC	Not possible, CNC
Channel OE (SC to VBAT)	OE cleared by clearing the corresponding LEx=0	Not possible, CNC	Not possible, CNC	Not possible, CNC
Manchester Error ME	ME cleared by SPI-readout or LEx off/on sequence	Not possible, CNC	Not possible, CNC	Not possible, CNC
Data error DE	DE cleared by SPI-readout or LEx off/on sequence	Not possible, CNC	Not possible, CNC	Not possible, CNC
No data	ND cleared by SPI-readout or LEx off/on sequence	CNC, cleared when LEx=1	Not possible, CNC	Not possible, CNC
Data received	data cleared by SPI-readout or LEx off/on sequence	Not possible, CNC	Not possible, CNC	Not possible, CNC

The behaviour of Hardware Error handling is described in following table.

Hardware Error HE	Behaviour when device power on	Behaviour when Line Enable=1 SV=0 (standard mode)	Behaviour when Line Enable=1 SV=1 (increased/daisy chain mode)
Short to GND (high side over current)	mask when channel is deactivated	• mask for 5.12 ms after channel activation • 512 us debouncing	• mask for 10.24 ms after channel activation • 10.24 ms debouncing
Iq out of range (Satellite quiescent current above upper limit)	mask when channel is deactivated	• mask for 5.12 ms after channel activation • no debouncing	• mask for 10.24 ms after channel activation • no debouncing
Over Temperature	mask when channel is deactivated	• mask for 100 µs after channel activation • no debouncing	• mask for 100 µs after channel activation • no debouncing
External resistor out of range	mask for 1 ms	• 512 µs debouncing	• 512 µs debouncing
No CLK	mask for 1 ms	• no debouncing	• no debouncing
VBUS/VSYNC too low delay	mask for 1 ms	• 32 µs debouncing	• 32 µs debouncing

The behaviour of Over Current Error handling is described in following table.

Over current Error OE	Behaviour when device power on	Behaviour when Line Enable=1 SV=0 (standard mode)	Behaviour when Line Enable=1 SV=1 (increased/daisy chain mode)
Short to V+ (low side over current)	mask when channel is deactivated	• mask for 5.12 ms after channel activation • 512 µs debouncing	• mask for 10.24 ms after channel activation • 512 µs debouncing

HE and OE are reset with external or internal reset or SPI_LINE_ENABLE command with LEx=0 (OFF) for the affected channel. V_Sync and V_Bus error can be active some seconds after power on and a HE is set without any channel is activated. To activate a channel in this case first the HE must be reset with the SPI_LINE_ENABLE command with LEx=0 (OFF).

5.2.5.6 SPI Sensor Non Sensor Data Request / Response Bit Definitions

5.2.5.6.1 Slave Command MOSI Bit Definition

Name	Bit Position	Definition
OP1:OP0	14:13	Opcode, defines operation (Read,Write)
SEN	13	Sensor Bit, defines request as Sensor data request or non sensor data request
A4:A0	12:8	Address, for read of write operation
D7:D0	7:0	Data, for write operation

5.2.5.6.2 Slave Responses MISO Bit Definition

Name	Bit Position	Definition
OP1:OP0	14:13	Opcode, identifies contents of Read or Write Data in D7:D0.
P	12	Parity, ensures odd parity for Bits 15:0 of MISO
ST1:ST0	11:10	Status, always “11” for non sensor response
ES1:ES0	9:8	Exception status, always “10” for non sensor response
D7:D0	7:0	Read Data / Error Data / Status
SE	2	SPI error, set to '1' for request (MOSI) frame violations
RE	1	Request error, set to '1' for illegal or unknown requests
DU	0	Data Unavailable, set to '1' if data for READ request is not available

5.2.6 SPI Commands

5.2.6.1 SENSOR_DATA

The SENSOR_DATA command is used to sample sensor data from the 981.07, and is the only command which uses the sensor data request/response format. The sampling moment is the first rising SCK edge within the response frame. If the sensor data within the Manchester decoder changes at the same time then this sampling is repeated at the second rising SCK edge. Details of this command are defined in section SPI Sensor Data Request / Response Format.

5.2.6.2 NON_SENSOR_DATA

The NON_SENSOR_DATA command is used write configuration data into the 981.07 configuration registers and read back status information. Details of this command are defined in section SPI Non Sensor Data Request / Response Format.

5.2.6.2.1 LINE_ENABLE

The LINE_ENABLE command is used to activate or deactivate the satellite receiver channels individually. The command is latched until a subsequent SPI update, reset, or any condition which deactivates the channel, such as thermal, or over current shutdown. The response indicates the current state (①) of the line activation and the over temperature status for each channel. By default all satellite channels are disabled.

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	0	0	0	0	1	1	x	x	x	x	x	x	LE2	LE1
MISO	0	0	1	P	1	1	1	0	0	0	OT2	OT1	0	0	LE2	LE1

READ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	0	1	1	x	x	x	x	x	x	x	x
MISO	0	1	0	P	1	1	1	0	0	0	OT2	OT1	0	0	LE2	LE1

OTx	Over Temperature Shutdown Indicator
0	No over temperature shut down on channel x
1	Over temperature shut down on channel x

LEx	Line Enable
0	Channel x OFF (default)
1	Channel x ON

① At the begin of the response.

5.2.6.2.2 LINE_SUPPLY_MODE

The LINE_SUPPLY_MODE command is used to configure the satellite voltage of each channel and the frequency of the external oscillator.

Satellite voltages VSAT_OUT of 6.5V or 8.0V can be adjusted. The default voltage is 6.5V. If a satellite voltage of 8V is requested the satellite voltage bit for the channel must be set.

For every channel the SVx bit influences some DC parameters in table Fehler: Referenz nicht gefunden and some AC parameters in table 4.2.1.

An external frequency of 4MHz or 8MHz can be adjusted. The default frequency is 4MHz. If an external frequency of 8MHz is requested the frequency select bit must be set.

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	0	1	1	1	1	0	x	x	x	F	X	X	SV2	SV1
MISO	0	0	1	P	1	1	1	0	0	0	0	F	0	0	SV2	SV1

READ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	1	1	1	1	0	x	x	x	x	x	x	x	x
MISO	0	1	0	P	1	1	1	0	0	0	0	F	0	0	SV2	SV1

SVx	Satellite Voltage
0	VSAT_OUT=6.5V standard mode (default)
1	VSAT_OUT=8.0V increased mode (daisy chain)

F	Frequency Select
0	CLK=4MHz (default)
1	CLK=8MHz

5.2.6.2.3 SYNC_ENABLE

The SYNC_ENABLE command is used to enable the sync pulses for the specified channels. It can be used for bidirectional communication between the MCU and the satellite sensors. The response indicates the current state (①) of the line sync pulse enable bits for each channel. By default all sync pulses are enabled. The command is latched until a subsequent SPI update, reset, or any condition which deactivates the channel, such as thermal, or over current shutdown.

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	0	0	0	1	0	0	x	x	x	x	X	X	SE2	SE1
MISO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	SE2	SE1

READ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x
MISO	0	1	0	P	1	1	1	0	0	0	0	0	0	0	SE2	SE1

SEx	Sync Enable
0	Sync Pulse for Channel x disable
1	Sync Pulse for Channel x enable (default)

① At the begin of the response.

5.2.6.2.4 NOP

The NOP command is used for retrieving the response from a previous command without altering anything within the RSU receiver. The response is a fixed write response with all data bits set to '0'. NOP is always a write command. Attempted read access to NOP will result in a SPI Error with the RE bit is set (RE=1).

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	0	1	0	1	1	1	x	x	x	x	x	x	x	x
MISO	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0

READ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	1	0	1	1	1	x	x	x	x	x	x	x	x
MISO	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0

5.2.6.2.5 SYNC_DELAY

The SYNC_DELAY command is used to control the time delay between two consecutive rising edges of the four SYNC pulses. If the eight SD bits are interpreted as an unsigned integer number, then the delay between two consecutive SYNC pulses t_{SYNC_DEL} can be calculated as

$$t_{SYNC\_DEL} = 0.5*SD\ \mu s$$

The default value is SD=8 (decimal), corresponding to $t_{SYNC\_DEL} = 4\ \mu s$.
The response indicates the current SD value. The command is latched until a subsequent SPI update or reset happens.

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	0	1	1	1	1	1	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
MISO	0	0	1	P	1	1	1	0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

READ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	1	1	1	1	1	x	x	x	x	x	x	x	x
MISO	0	1	0	P	1	1	1	0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

5.2.6.2.6 GRANT_TESTMODE

The GRANT_TESTMODE command must not be used except for ELMOS production test. To enter the device's test modes two conditions have to be satisfied:

- the TEST pin has to be pulled high.
- the GRANT_TESTMODE request has to be the next SPI frame that is issued.

Within test mode, the device provides extended functionality which is used for production test purposes.

WRITE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	0	1	0	0	1	0	x	x	x	x	x	x	x	x
MISO	N.A.															

5.2.6.3 SPI Failure Mode

5.2.6.3.1 SPI Errors

SPI Errors are defined as a condition, where the SPI frame format is incorrect. When detected, the 981.07 response with an error response message on MISO with the SPI Error (SE) bit is set.

The following conditions generate a SPI Error:

- Incorrect number of SPI SCK cycles while CSB is active (low). In case of zero SCK cycles no error bit is set.
- SCK is high at CSB falling edge.

5.2.6.3.2 SPI Request Errors

SPI Request Errors are defined as conditions where the contents of a SPI request message are incorrect. When detected, the 981.07 responds with an error response message on MISO with the Request Error (RE) bit being set.

The following conditions generate an SPI Request Error:

- Undefined command (incorrect address in bits [12:8])

5.2.7 Remote Sensor Decoder

5.2.7.1 Functional Description

The remote sensor interface is a two-wire unidirectional current interface used for the connection of a remote sensing unit (RSU).
The device includes four such interfaces which are fully independent on one another.

5.2.7.2 Manchester Code

The input data is Manchester 2 coded with a baud rate of 125 kbit/s (T_{BIT} = 8µs). The RSU receiving unit of the 981.07 is clocked with CLK or CLK/2 to get a nominal sampling frequency of 4 MHz. Every bit is coded by two consecutive pulses of equal length. A logical '1' is coded by a low pulse followed by a high pulse, a logical '0' is coded by a high pulse followed by a low pulse. Figure 5.2-4 shows an example.

Example:

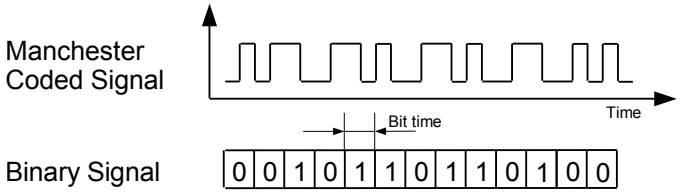


Figure 5.2-4: Manchester Code

5.2.7.3 Message Protocol Format

As shown in Figure 5.2-5 each transmitted telegram consists of 2 start bits, 10 data bits and 1 parity bit. Data bits are transferred with LSB first. Both start bits are logical '0'. The parity is even and is calculated over data bits D0 to D9. The time per bit is 8 µs and consequently the complete 13-bit data frame is transferred in 104µs.

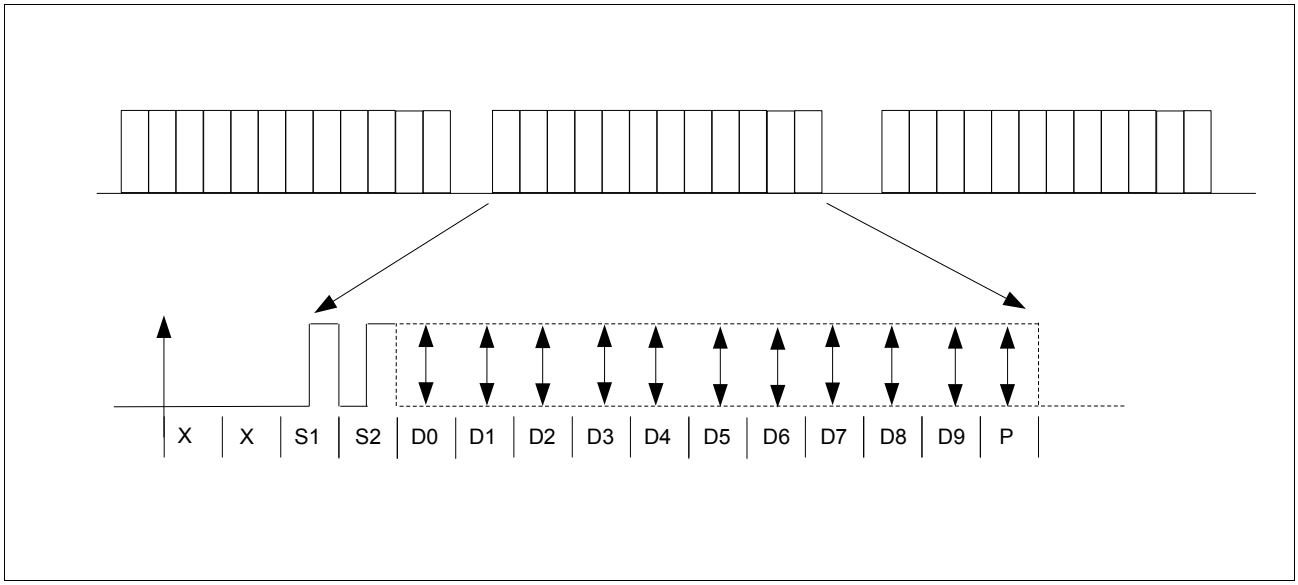


Figure 5.2-5: Message Protocol Format

5.2.7.4 Manchester Decoder

The Manchester Decoder tolerates satellite communication as per PSI5 specification for P10P-500/3L mode of operation. The received data bits are first stored in a receive register in order to check the consistency of the data word.
Depending on the time slot where the telegram is transmitted, the received data word is stored into the appropriate sensor data register (see 5.2.5.4).
A Manchester Error (ME) is set if two valid start bits are detected and the transmitted telegram has not exactly 13 valid bits or the bit timing is incorrect.
A transmitted telegram which is not within one of the three time slots result also into a Manchester Error:

Start of Transmission within	End of Transmission within	Manchester Error is stored in sensor data register
Time slot 1	Time slot 2	A
Time slot 2	Time slot 3	B
Time slot 3	After time slot 3	C
After time slot 3	After time slot 3	C

A Data Error (DE) is set when the parity bit is wrong.

5.3 External Oscillator

The received data messages are stored in data registers, which can be read out by the MCU via the SPI interface. In order to realise a time base for the sampling of the satellite data, an external clock of typical 4MHz respectively 8MHz (CLK) is provided to the device. In case of a disconnection of CLK, the channels will be switched off.

In case of disconnection of the oscillator the sensor data response is a hardware error.

5.4 Power On Reset

The power-on reset enables the logic. The reset is only related to V3_3. The logic can operate without a supply from VBUS and VSYNC.

5.5 Over Temperature Switch Off

The circuit provides an over temperature protection independent for each channel. Due to a failure like short circuit, the circuit will react as follows.

When the chip temperature increases up to 170° C, the over temperature protection will be activated and the affected satellite interface will be switched off. The temperature switch off operates independently from the external system clock (CLK) and is only dependent on the internal oscillator (f_{osc}).

The failure mode is reported as an hardware error via SPI. The hardware error bit can be cleared, by clearing the LE bit in the LINE_ENABLE command. The regulator can be reactivated manually by setting the LE bit in the LINE_ENABLE command to '1'.

6 Application notes

6.1 Recommended application circuits

To ensure proper operation of the interfaces with the wiring harness and the sensors the following recommendations have to be taken into account.
The regulator in the interface does not need a stabilisation capacitance to prevent instability. Nevertheless external components are needed to reduce ringing at the output, especially in case of large inductors connected to the pin.

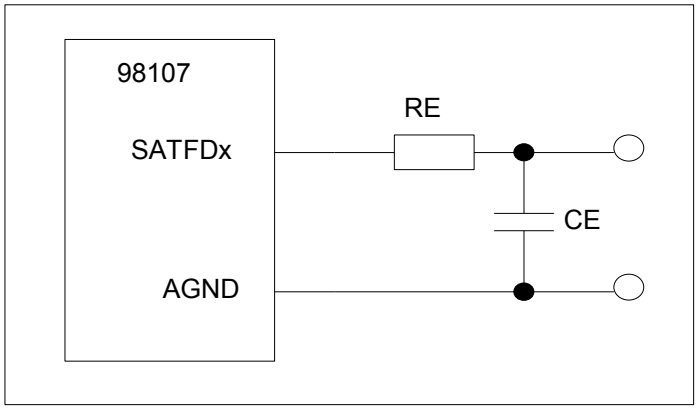


Figure 6.1-1: Recommended ECU-board circuitry

RE should be between 3.3Ohms and 12Ohms (5Ohms are the minimum resistance conform to PSI-5 specification). The resistor reduces the oscillations coming from the wiring harness. It damps the influence of the wiring inductor and leads to an, over the frequency range constant, termination resistor.
The capacitor CE ensures a minimum input capacitance and is also mandatory to achieve a sufficient ESD-performance. The next figure shows further possible ECU-circuits. The capacitor CEopt removes potential oscillations in short circuit conditions. If RE is chosen to be less than 3.3Ohms CEopt should be larger 4.7nF, with 10nF no oscillation in short circuit conditions have been observed

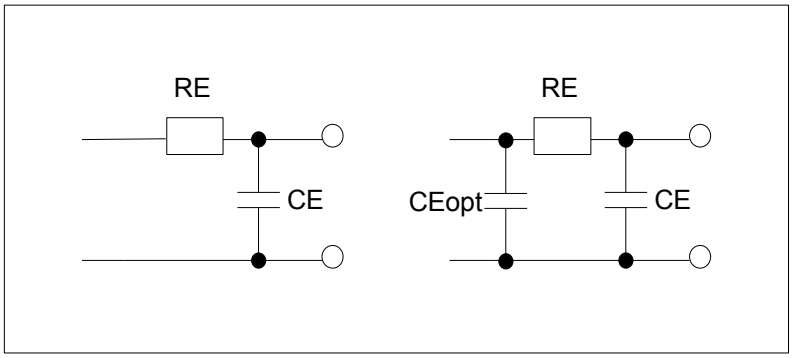


Figure 6.1-2: further recommended ECU-board circuits

The ECU-circuitry should be optimised for the connected wiring harness. The proposed circuits work well in case of point-to-point connection and parallel bus lines.
For serial bus connections (and daisy-chain operation) the wiring harness, together with the sensor capacitors, form coupled LC-resonant circuits which can only hardly be damped by the resistor on the ECU-board.

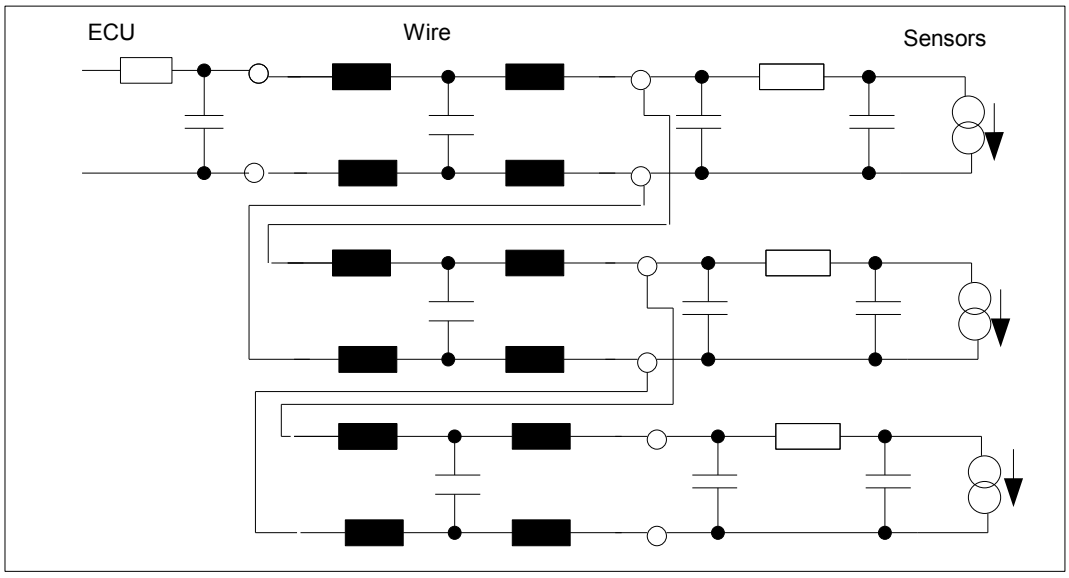


Figure 6.1-3: serial bus connection

The oscillations which can occur in case of wiring harness shown in figure 6.3 can be damped by including additional series resistors in the wiring harness.

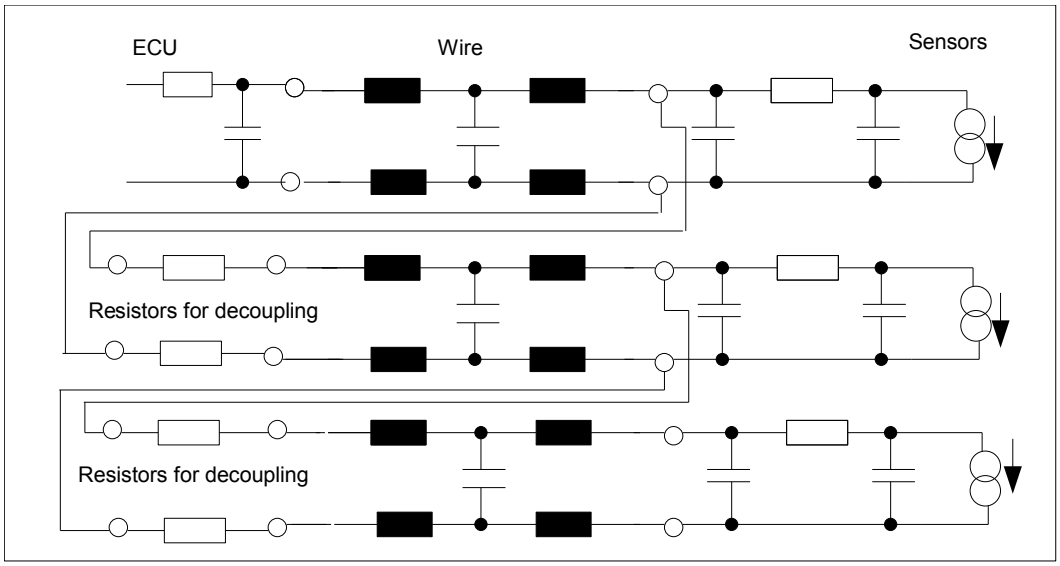


Figure 6.1-4: serial bus connection with damping resistors

The decoupling resistors damp the LC-resonant circuits (wire inductance + sensor capacitance). In the figure 6.4 a pair of resistors is shown. It is also possible to use only one resistor in the supply-line. The value of the resistor is about 2-4Ohms.
Without damping the data current show oscillations at the rising and falling edge of the data current. This can lead to a disturbed communication and has to be avoided.

7 ESD and Latchup

7.1 ESD Protection Circuit

7.2 ESD Sensitivity Classification Test Method

7.2.1 ESD Classification: Human Body Model

The ESD Protection circuitry is measured following AECQ 100 (Human Body Model) under following conditions:

Pins	Condition
SATFD1-2	VIN= 3kV, R_{EXT}=1.5kΩ, C_{EXT}=100pF
Others	VIN= 2kV, R_{EXT}=1.5kΩ, C_{EXT}=100pF

7.2.2 System-level ESD-Test

Pins	Condition
SATFD1-2	VIN= +/-4kV, 330Ohm, 150pF against AGND1, 2, DGND (all shorted) with CEopt=22nF, RE=5Ω, CE=2.2nF to gnd at SATFD1,2
SATFD1-2	VIN= +/-8kV, 330Ohm, 150pF against AGND1, 2, DGND (all shorted) with CEopt=22nF, RE=5, CE=2.2nF, to gnd at SATFD1,2. An additional 33V zener diode in parallel to the output is needed.

7.3 Latch-up

Pins	Condition
SATFD1-2, VBUS, VSYNC, MOSI, CSB, SCK, SAT_SYNC, CLK, RESETB	Following JEDEC-78

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