Intronics Power ®

Low Power/High Performance 16-Bit A/D Converter

ADC1143

FEATURES

Low Power Consumption:
- 175mW max, V_S = ±15V
- 150mW max, V_S = ±12V

Guaranteed Nonlinearity:
- ±0.006% FSR max (ADC1143J)
- ±0.003% FSR max (ADC1143K)

Guaranteed Differential Nonlinearity:
- ±0.006% FSR max (ADC1143J)
- ±0.003% FSR max (ADC1143K)

Low Differential Nonlinearity T.C.:
- ±2ppm/°C max (ADC1143J)
- ±1ppm/°C max (ADC1143K)

Fast Conversion Time:
- 70µs max (ADC1143J)
- 100µs max (ADC1143K)

Wide Power Supply Operation:
- V_S = ±11.4V to ±18.0V
- V_D = +3.0V to +18.0V

APPLICATIONS

Seismic Data Acquisition
Oil Well Instrumentation
Portable Industrial Scales
Portable Test Equipment
Robotics

GENERAL DESCRIPTION

The ADC1143 is a low power 16-bit successive-approximation analog-to-digital converter with a maximum power consumption of 175mW at V_S = ±15V, 150mW at V_S = ±12V, and is contained in a 2" × 2" × 0.4" module.

High performance like integral nonlinearity of ±0.006% FSR (ADC1143J)/ ±0.003% FSR (ADC1143K) and differential nonlinearity of ±0.006% FSR (ADC1143J)/ ±0.003% FSR (ADC1143K) are guaranteed. Additional guaranteed performance includes: differential nonlinearity T.C. of ±2ppm/°C (ADC1143J)/ ±1ppm/°C (ADC1143K), offset T.C. ±40µV/°C and gain T.C. ±12ppm/°C.

The ADC1143 makes extensive use of CMOS integrated circuits and thin-film components to obtain low power consumption, excellent performance and small size. The internal 16-bit CMOS DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary current steering switches. CMOS successive-approximation registers, low power comparator and low noise reference are also used to optimize the performance of the ADC1143 (shown in Figure 1).

The ADC1143 can operate with power supply voltages ranging from ±11.4V dc to ±18.0V dc for V_S and +3V dc to +18V dc for the V_D supply. An internal voltage reference is provided, but an external reference can be used. Five analog input voltage ranges are selectable via user pin programming: +5V, +10V, +20V, ±5V and ±10V. Digital output coding in unipolar operation is true binary; for bipolar operation, the coding is offset binary or two's complement. Digital outputs are provided in both parallel and serial formats.

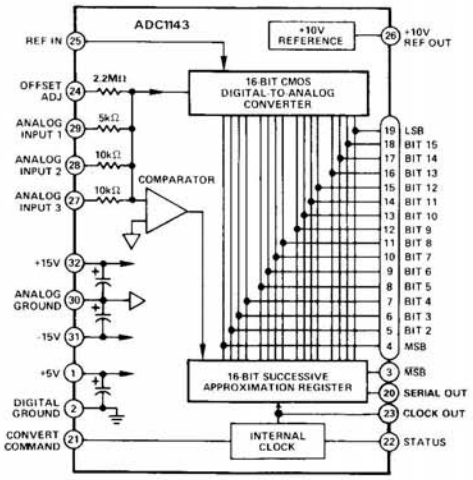

Figure 1. ADC1143 Functional Block Diagram

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SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15V$, $V_D = +5V$, $V_{REF} = +10V$ unless otherwise specified)

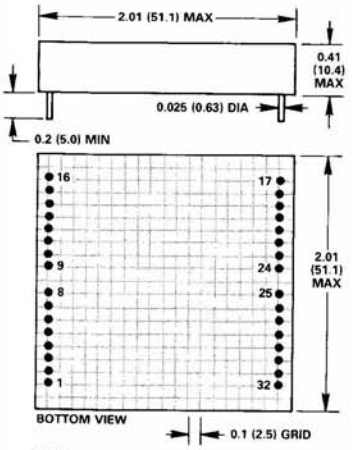
MODEL	ADC1143J	ADC1143K
RESOLUTION	16 Bits	*
CONVERSION TIME	70µs (max)	100µs (max)
ACCURACY		
Integral Nonlinearity	± 0.006% FSR[1] (max)	± 0.003% FSR[1] (max)
Differential Nonlinearity	± 0.006% FSR[1] (max)	± 0.003% FSR[1] (max)
No Missing Codes (0 to + 50°C)		
13 Bits	Guaranteed	
14 Bits		Guaranteed
STABILITY		
Differential Nonlinearity	± 2ppm/°C (max)	± 1ppm/°C (max)
Offset	± 40µV/°C (max)	*
Bipolar Offset	± 9ppm/°C (max)	*
Gain	± 12ppm/°C (max)	*
ANALOG INPUT		
Voltage Range		
Unipolar	+ 5V, + 10V, + 20V	*
Bipolar	± 5V, ± 10V	*
Input Resistance		
+ 5V	2.5kΩ	*
+ 10V, ± 5V	5.0kΩ	*
+ 20V, ± 10V	10.0kΩ	*
External Reference Input		
Voltage Range[2]	0 to + 12V	*
Input Resistance	10kΩ	*
DIGITAL INPUTS		
Convert Command	Positive Pulse, 1µs width (min) negative edge triggered	*
Logic Loading	CMOS Compatible	*
DIGITAL OUTPUTS		
Parallel Output Data		
Unipolar	Binary (BIN)	*
Bipolar	Offset Binary (OBIN), Two's Comp	*
Output Drive	CMOS Comp, 2LSTTL Loads	*
Status	"0" During Conversion	*
Output Drive	CMOS Comp, 2LSTTL Loads	*
Serial Output		
Output Drive	CMOS Comp, 1 LSTTL Load[3]	*
Clock Output		
Output Drive	CMOS Comp, 1 LSTTL Load	*
INTERNAL REFERENCE (V_{REF})		
Voltage	+ 10V, ± 0.3%	*
External Load Current	2mA max	*
Temperature Stability	± 8.5ppm/°C max	*
POWER REQUIREMENTS		
Voltage (rated performance)	± 15V(± 5%), + 5V(± 5%)	*
Voltage (operating)	± 11.4V to ± 18V, + 3V to + 18V	*
Supply Current Drain		
$+V_S = +15V$	4mA	*
$-V_S = -15V$	5mA	*
$+V_D = +5V$	4mA	*
Total Power		
$V_S = \pm 12V, V_D = +5V$	150mW max	*
$V_S = \pm 15V, V_D = +5V$	175mW max	*
POWER SUPPLY SENSITIVITY		
Offset	± 0.001%FSR/% $\pm V_S$	*
Gain	± 0.001%FSR/% $\pm V_S$	*
TEMPERATURE RANGE		
Rated Performance	0 to + 70°C	*
Operating	− 25°C to + 85°C	*
Storage	− 25°C to + 85°C	*
Relative Humidity	Meets MIL-STD 202E, Method 103B	*
SIZE	2" × 2" × 0.4" (50.8 × 50.8 × 10.16mm)	*
Weight	33g	*
PRICE		
(1–9)	$199	$229
(100-249)	$149	$172

NOTES:
[1]FSR Means Full Scale Range.
[2]Rated performance is specified with + 10.0V reference.
[3]LSTTL drive requires 2.2kΩ pulldown resistor.

Offset and gain errors are adjustable to zero by means of external potentiometers. See Figure 3 for proper connections.
Recommend Power Supply: Analog Devices Model 923
*Specifications same as ADC1143J
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS AC1584-3 (2 REQUIRED) PRICE (1-9) $10

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	CLOCK OUT
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	SERIAL OUT
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OPERATION

For operation, the only connections to the ADC1143 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.

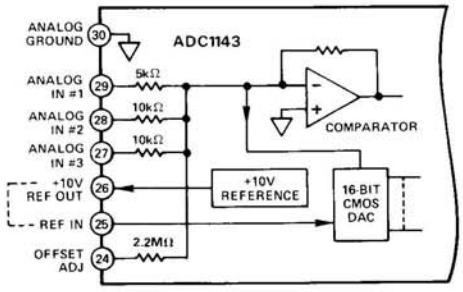


Figure 2. Analog Input Block Diagram

ANALOG INPUT RANGE

The analog input voltage section of the ADC1143 consists of three analog input terminals (see Figure 2). Analog input voltage range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a +5V, +10V or +20V input signal can be applied. These input voltages develop a 0 to +2mA current which is compared to the 0 to −2mA current output of the internal reference DAC in the ADC1143. In the bipolar mode, a ±5V or ±10V input signal can be applied. These input voltages develop a ±1mA current which is compared to a 0 to −2mA current of the internal reference DAC which is offset by +1mA, to produce a ±1mA current.

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage reference used as a signal source must be very stable and have the capability of being set within ±1μV of the desired value. The potentiometers should be good quality cermet type. Multiturn potentiometers having ten to fifteen turns and ±100ppm/°C temperature coefficients will be adequate. The temperature coefficient contribution will be less than ±0.1ppm/°C.

By adjusting the offset first, gain and offset adjustment will remain independent of each other.

OFFSET CALIBRATION

For +5V range, set the input voltage to precisely +38μV; for +10V range, set it to +76μV; for +20V range, set it to +153μV.

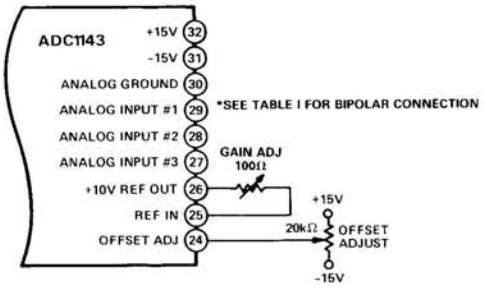


Figure 3. Offset and Gain Calibration

Adjust the offset potentiometer until the binary output code is on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage to precisely −4.999924V; for ±10V range, set it to −9.999847V. Adjust the offset potentiometer until the offset binary code is on the verge of switching between 000 . . . 00 and 000 . . . 01, and two's complement coded units are switching from 100 . . . 00 to 100 . . . 01.

GAIN CALIBRATION

For +5V range, set the input voltage to precisely +4.99988V; for +10V range, set it to +9.99977V; for +20V range, set it to +19.9995V. Adjust the gain potentiometer until the binary output code is on the verge of switching from 111 . . . 10 to 111 . . . 11.

For ±5V range, set the input voltage to precisely +4.99977V; for ±10V range, set it to +9.99954V. Adjust the gain potentiometer until the offset binary code is on the verge of switching from 111 . . . 10 to 111 . . . 11, and the two's complement coded units are switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally in the ADC1143, thus the connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1143 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

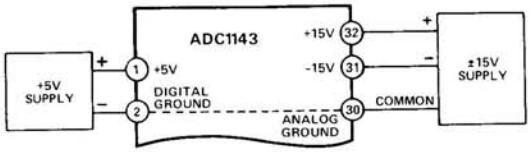


Figure 4. Power Supply and Grounding Techniques

Input Voltage Range	Output Coding	Connect Input Signal To Pin(s)	Connect Pin* 26 to Pin #	Connect Pin 30 to Pin(s)
+5V	BIN	27, 28, 29	open	2
+10V	BIN	27, 28	open	2, 29
+20V	BIN	27	open	2, 28, 29
±5V	OBIN, 2's Comp	29	27	2, 28
±10V	OBIN, 2's Comp	28	27	2, 29

*If internal reference is used, Pins 25 and 26 must be connected together through a 100Ω potentiometer or 49.9Ω fixed resistor (see Figure 3 and Gain Calibration Section).

Table I. Analog Input Voltage Range Pin Programming

EXTERNAL REFERENCE

The ADC1143 is capable of operating with an external reference. Simply disconnect the gain trim potentiometer from Pin 26 and connect it to the external reference as shown in Figure 5. The ADC1143 is tested and specified with a +10.0V reference. An external reference with a voltage of 0 to +12V can be applied. The external reference must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained.

When using an external reference, the digital output coding can be determined by the formula shown in Figure 5.

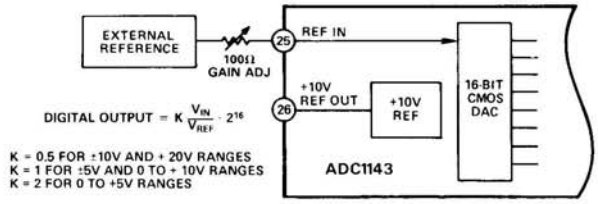


Figure 5. External Reference

ADC1143 TIMING

Conversion is initiated with the negative going edge of the convert command pulse as shown in Figure 6. The convert command pulse width must be a minimum of 1μs. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the convert command pulse, all internal logic is reset. The MSB is set high with the remaining bits set to logic low. The status line is set low and remains low through the full conversion cycle.

During conversion, each bit starting with the MSB is set high on the rising edge of the internal clock. The ADC's internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete conversion of the ADC1143J and ADC1143K

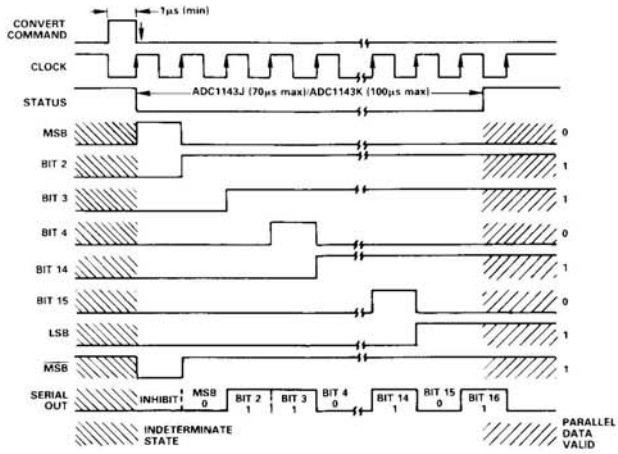


Figure 6. ADC1143 Timing Diagram

taking 70μs max and 100μs max respectively. The parallel output data is valid on the rising edge of the status line.

Serial output data is valid for each bit at the completion of clock cycle used to make the bit decision as shown in Figure 6.

SEISMIC DATA ACQUISITION APPLICATION

The ADC1143's low power consumption and high performance make it ideally suited for portable seismic data acquisition systems like the one shown in Figure 7. In seismic data acquisition systems, geophones are used to receive reflected shock waves from subsurface strata, induced by controlled discharge of explosives. These reflected signals may travel several miles before reaching the geophones and are difficult to discern from noise or other interference like ground roll. The low level signals from the geophones are amplified and filtered appropriately to remove the undesired signals. The conditioned signal is amplified by the PGA then held by SHA and converted to digital form by the ADC1143. The digital data is stored on an on-site recorder for later data collection and processing.

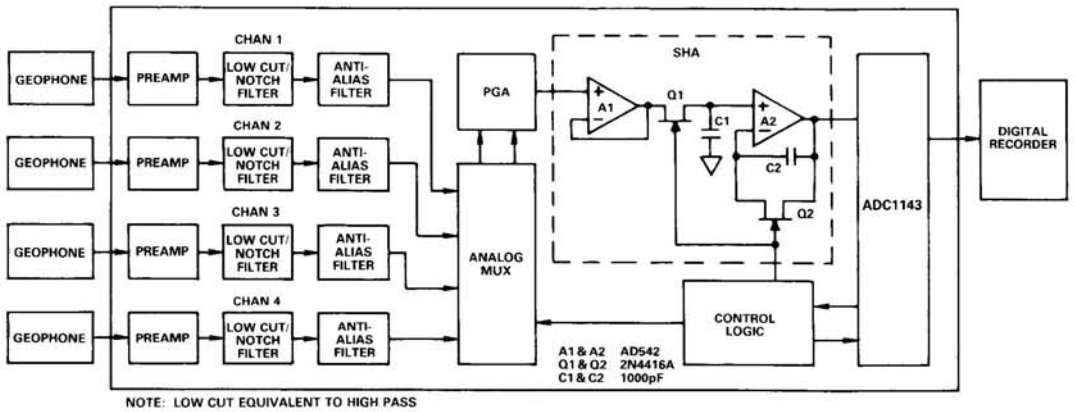


Figure 7. Seismic Data Acquisition System Block Diagram