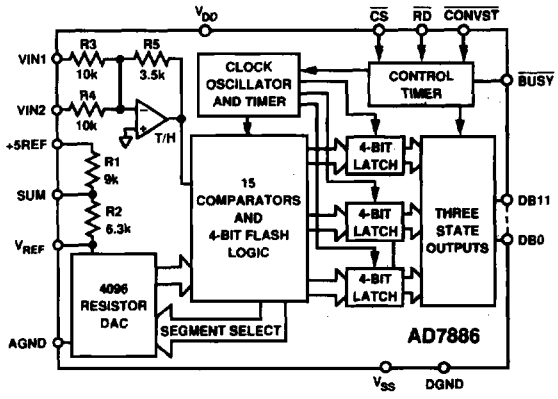
LC²MOS
12-Bit, 750 kHz/1 MHz, Sampling ADC
AD7886

2

FEATURES
750 kHz/1 MHz Throughput Rate
1 μs/750 ns Conversion Time
12-Bit No Missed Codes Over Temperature
67 dB SNR at 100 kHz Input Frequency
Low Power—250 mW typ
Fast Bus Access Time—57 ns max

APPLICATIONS
Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7886 is 12-bit ADC with a sample-and-hold amplifier offering high speed performance combined with low power dissipation. The AD7886 is a triple pass flash ADC, which uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 μs/750 ns conversion time. An on-chip clock oscillator provides the appropriate timing for each of the three conversion stages eliminating the need for any external clocks. Acquisition time of the sample-and-hold amplifier gives a resulting throughput rate of 750 kHz/1 MHz.*

The AD7886 operates from ±5 V power supplies. Pin-strappable inputs offer a choice of three analog input ranges; 0 to 5 V, 0 to 10 V or ±5 V.

In addition to the traditional dc accuracy specifications such as linearity, offset and full-scale errors, the AD7886 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7886 has a high speed digital interface with three-state data outputs. Conversion control is provided by a $\overline{\text{CONVST}}$ input. Data access is controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs, standard microprocessor signals. The data access time of less than 57 ns means that the AD7886 can interface directly to most modern microprocessors including DSP processors.

*Contact your local salesperson for further information on the 1 MHz version.

The AD7886 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

The AD7886 is available in both a 28-pin DIP and in a 28-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. Fast 1.33 μs/1 μs Throughput Time.
   Fast throughput time makes the AD7886 suitable for a wide range of data acquisition applications.
2. Dynamic Specifications for DSP Users.
   The AD7886 is specified for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast Microprocessor Interface.
   Standard control signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, and fast bus access times make the AD7886 easy to interface to microprocessors.
4. Low Power.
   LC²MOS fabrication process gives low power dissipation of 250 mW.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7886—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, V_{REF} = −3.5 V, connected as shown in Figure 2. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply for 750 kHz version.)

Parameter	J Version[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3] (SNR)	65	67	65	dB min	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Total Harmonic Distortion (THD)	−75	−75	−75	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Peak Harmonic or Spurious Noise	−77	−77	−77	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−80	dB typ	f_a = 96 kHz, f_b = 103 kHz, f_{SAMPLE} = 750 kHz
Third Order Terms	−80	−80	−80	dB typ	
ACCURACY					
Resolution	12	12	12	Bits	
Integral Linearity T_{min} to T_{max}		±2	±2	LSB max	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Unipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Unipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
ANALOG INPUT					
Unipolar Input Current	1.5	1.5	1.5	mA max	Input Ranges: 0 to 5 V or 0 to 10 V
Bipolar Input Current	±0.75	±0.75	±0.75	mA max	Input Range: ±5 V
REFERENCE INPUT					
V_{REF}	−3.5	−3.5	−3.5	Volts	±2% For Specified Performance
Input Reference Current	−10	−10	−10	mA max	
R1, Resistance	9	9	9	kΩ nom	±25%
R2, Resistance	6.3	6.3	6.3	kΩ nom	±25%
R2/R1 Ratio	0.7	0.7	0.7	nom	±0.1%
POWER SUPPLY REJECTION					
V_{DD} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{SS} = −5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{DD} = +5 V, V_{SS} = −4.75 V to −5.25 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB11–DB0, $\overline{BUSY}$					
Output High Voltage, V_{OH}	4	4	4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Output Capacitance[4]	15	15	15	pF max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	35	35	35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	−35	−35	−35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	250	250	250	mW typ	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
	350	350	350	mW max	

NOTES

[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; B Version: −40°C to +85°C; T Version: −55°C to +125°C.

[2]Applies to all three input ranges, VIN = 0 to FS, pk-to-pk V.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @+25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K Versions)	Limit at T_{min}, T_{max} (B Version)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
	1	1	1	μs max	
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_4	**60**	**60**	75	ns min	$\overline{RD}$ Pulse Width
t_5	100	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay, (C_L = 10 pF)
t_6[2]	**57**	**57**	**70**	ns max	Data Access Time After $\overline{RD}$
t_7[3]	**10**	**10**	**10**	ns min	Bus Relinquish Time After $\overline{RD}$
	50	**50**	**60**	ns max	
t_8	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_9[3]	10	10	10	ns min	Bus Relinquish Time After $\overline{CONVST}$
	100	100	100	ns max	
t_{10}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low
t_{11}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low
t_{12}	250	250	250	ns typ	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, SHA Acquisition Time
t_{13}	1.333	1.333	1.333	μs min	Sampling Interval
t_{CONV}	950	950	950	ns typ	Conversion Time
	1000	**1000**	**1000**	ns max	

NOTES
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_7 and t_9 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the load capacitor, C_L. This means that the times, t_7 and t_9, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

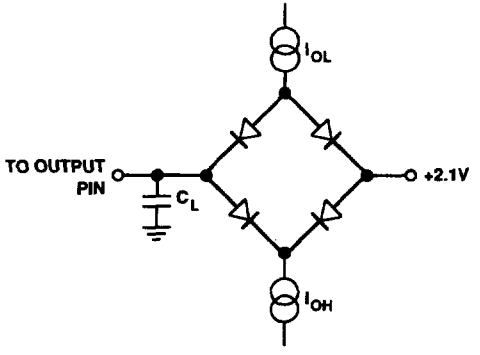


Figure 1. Load Circuit for Bus Access and Relinquish Time

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
VIN1, VIN2, SUM, +5REF to AGND . . . . −15 V to +15 V
V_{REF} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
$\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR (dBs)	Integral Nonlinearity (LSBs)	Package Option[3]
AD7886JD	0°C to +70°C	65		D-28
AD7886KD	0°C to +70°C	67	±2.0	D-28
AD7886JP	0°C to +70°C	65		P-28A[2]
AD7886KP	0°C to +70°C	67	±2.0	P-28A[2]
AD7886BD	−40°C to +85°C	67	±2.0	D-28
AD7886TD	−55°C to +125°C	65	±2.0	D-28

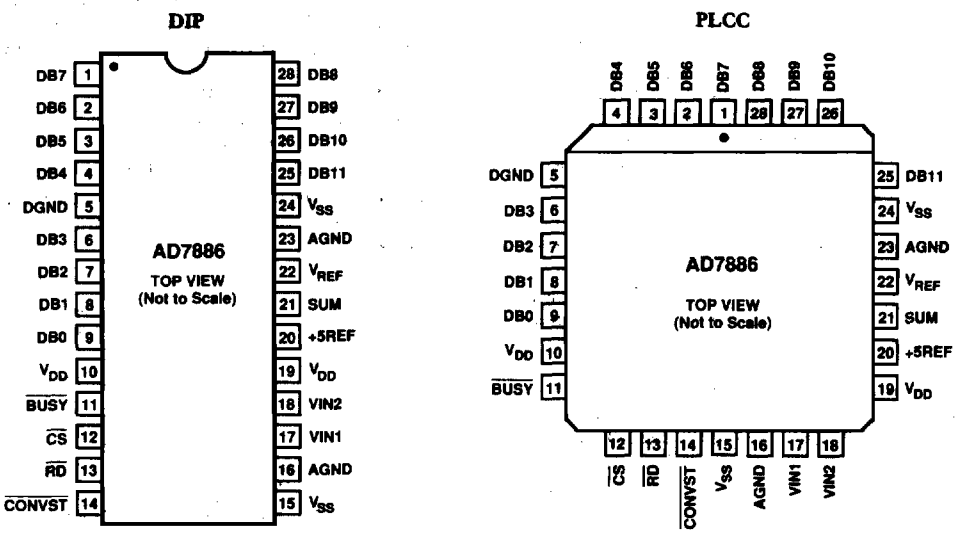
NOTES
[1]Contact your sales office for availability of AD7886BD, AD7886TD and 1 MHz version.
[2]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier (JLCCC) in lieu of PLCC packages.
[3]D = Ceramic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

DIP Pin Number	Mnemonic	Description
Power Supply		
10 & 19	V_{DD}	Positive Power Supply, +5 V ± 5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins must be tied together.
16 & 23	AGND	Analog Ground. Both AGND pins must be tied together.
5	DGND	Digital Ground.
Analog and Reference Inputs		
17 & 18	VIN	Analog Inputs, VIN1 and VIN2. The part can be pin strapped for any one of three analog input ranges;
20	+5REF	+5 V Reference input. This input is used in conjunction with SUM and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
21	SUM	Summing Point. This input is used in conjunction with +5REF and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
22	V_{REF}	Voltage Reference Input. The AD7886 is specified with V_{REF} = −3.5 V.
Interface and Control		
1–4, 6–9, 25–28	DB7–DB4 DB3–DB0 DB11–DB8	Three-state data outputs. These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the Most Significant Bit (MSB).
11	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers.
14	$\overline{CONVST}$	Conversion Start Input. This input is used to start conversion.

Range	Pin Strap	Signal Input
0 to 5 V	Connect VIN2 to VIN1	VIN1 & VIN2
0 to 10 V	Connect VIN2 to GND	VIN1
±5 V	Connect VIN2 to +5 V	VIN1

PIN CONFIGURATIONS



TERMINOLOGY

Unipolar Offset Error

The ideal first code transition should occur when the analog input is 1 LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

Bipolar Zero Error

The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000 for the ±5 V range should occur when the analog input is at zero volts. Bipolar zero error is the deviation of the actual transition from that point.

Gain Error

In the unipolar mode, gain error is measured with respect to the first and last code transition points. The ideal difference between these points if FS−2 LSBs. For bipolar applications, the gain error is measured from the midscale transition to both the first and last code transitions. The ideal difference in this case is FS/2−1 LSB. The gain error is defined as the deviation between the ideal difference, given above, and the measured difference. For the bipolar case, there are two gain errors, the figure in the specification page represents the worst case. Ideal FS depends on the +5REF input; for the 0 to 5 V input, ideal FS = +5REF and for the 0 to 10 V and ±5 V ranges, ideal FS = 2 × +5REF.

CONVERTER DETAILS

The AD7886 is a triple-pass flash ADC which uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the V_{REF}/16 voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

REFERENCE INPUT

The AD7886 operates from a −3.5 V reference which must be provided at the V_{REF} input. Two on-chip resistors for use with an external amplifier can be used for deriving −3.5 V from standard 5 V references. Figure 2 shows an example with the AD586 which a is a high performance voltage reference which exhibits excellent stability performance, 5 ppm/°C max. The external amplifier serves a second function of force/sensing the V_{REF} input. Force/sensing minimizes error contributions from

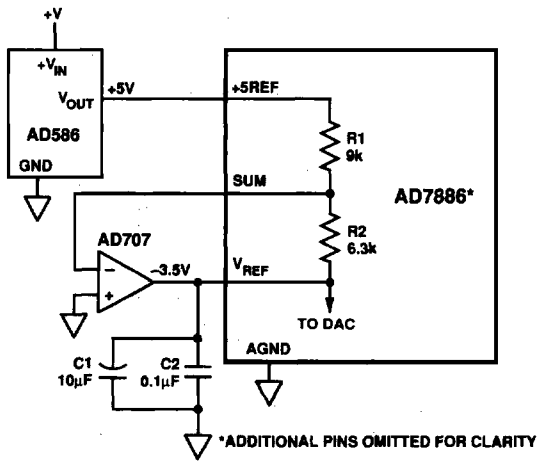


Figure 2. Typical Reference Circuitry

voltage or IR drops along the internal conductors. IR drops in the reference path cause a gain error, and typically the external amplifier reduces this error by 2 LSBs. In systems where a −3.5 V reference is available then it can be applied to the V_{REF} input directly causing a slight increase in gain error. A low op amp offset voltage is important as any offset voltage will add directly to the voltage that is being force/sensed. Suitable op amps for this application are precision op amps such as the AD705 or the AD707 which feature offset voltages of less than 100 μV.

Proper decoupling on the op amp output is important to suppress high speed transients during the conversion procedure. Note, connecting capacitors directly to op amp outputs can cause stability problems. However, the use of large capacitors, 10 μF in Figure 2, limits the open-loop bandwidth preventing any closed-loop oscillations.

TRACK-AND-HOLD AMPLIFIER

The analog input is sampled by an on-chip track-and-hold amplifier before being applied to the ADC. The 3dB bandwidth of this amplifier is typically 20 MHz which is much greater than the Nyquist limit of the ADC, so it can be used for undersampling applications. The track-and-hold amplifier acquires the input signal to 12-bit accuracy in less than 333 ns. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time which is 1.333 μs for the AD7886.

The operation of the track/hold amplifier is essentially transparent to the user. The track-to-hold transition occurs at the start of conversion on the falling edge of $\overline{\text{CONVST}}$. The conversion procedure does not start until the rising edge of $\overline{\text{CONVST}}$. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to-hold settling time. The track/hold reverts back to the track mode at the end of conversion when $\overline{\text{BUSY}}$ has returned high.

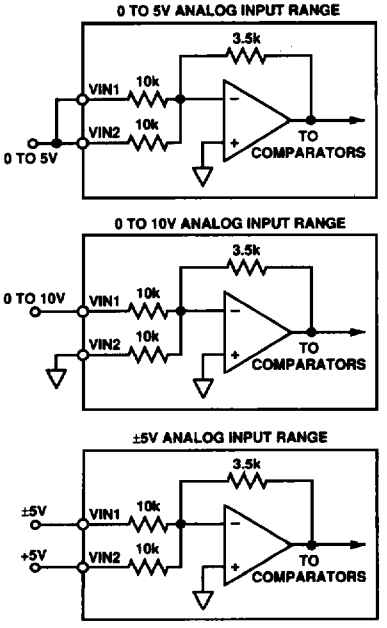


Figure 3. Analog Input Range Configurations

ANALOG INPUT RANGES

The AD7886 has three user selectable analog input ranges: 0 to 5 V, 0 to 10 V and ±5 V. Figure 3 shows how to configure the two analog inputs (VIN1 and VIN2) for these ranges.

UNIPOLAR OPERATION

Figure 4 shows a typical unipolar circuit for the AD7886. The ideal input/output characteristic is shown in Figure 5. The designed code transitions occur on integer multiples of 1 LSB.

The output code is natural binary with 1 LSB = FS/4096. FS is either +5 V or +10 V depending on how the analog inputs are configured.

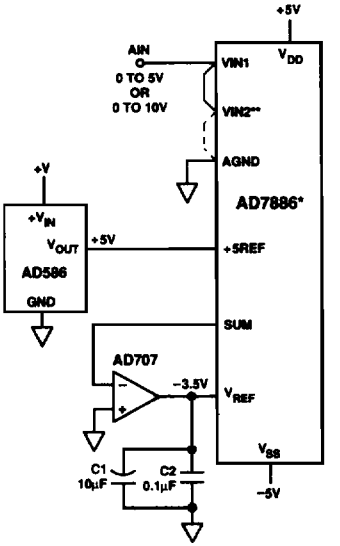


Figure 4. Unipolar Operation

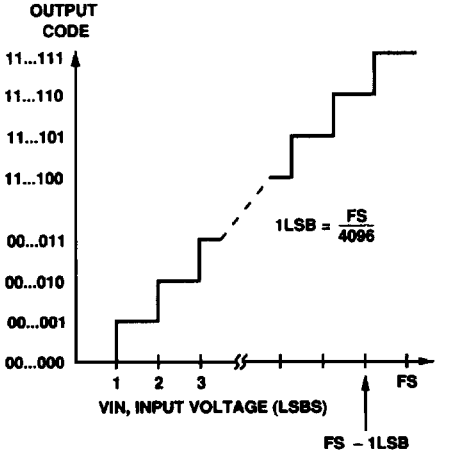


Figure 5. Ideal Input/Output Transfer Characteristic for Unipolar Operation