ASIX AX88875AP

10/100BASE 5-Port
Dual Speed “Bripeater” Controller
Data Sheets (10/16/’00)

Always contact ASIX for possible updates
before starting a design.

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FIGURES

1.0 AX88875A Overview

The AX88875A 10/100Mbps Dual Speed "**Bripeater"** Controller is **"a dual speed repeater with build in bridge function"** It is design for low cost dumb HUB application. The AX88875A directly supports up-to **five** 10/100Mbps automatic links MII interfaces specially for SOHO market. The AX88875A is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" It is fully compatible with IEEE 802.3u standard.

1.1 General Description

The AX88875A Repeater Controller is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. The AX88875A has five Media Independent Interfaces (MII) to connect to PHY or MAC devices.

The AX88875A supports 5 MII interfaces ports, a bridge packet buffer SRAM interface and LED display interface. AX88875A without support expansion port to cascade to other AX88850 and AX88860 pure 100Mbps repeater chips..

The AX88875A supports stand along 10/100Mbps dual speed repeater applications with two LED display mode.

The AX88871A has two LED display mode.

Mode 0	Direct LED display mode.
Mode 1	Rich LED display mode.

1.2 Features

- IEEE 802.3u repeater compatible
- Supports per port 10/100Mbps alternative with auto detected
- Build in 10/100Mbps bridge engine with following features
  1. Minimum 32K bytes, maximum 128K bytes SRAM to buffer packets
  2. Seamless buffer management without waste any space of buffer memory
  3. Simple asynchronous 8-bit SRAM interface to reduce system cost
  4. 256 or 1024 entries is supported
  5. Auto learning and filtering
  6. Two forwarding modes are supported : Store-n-Forward and fragment-free
  7. Flow-control is supported optionally.
  8. Buffer RAM auto testing
  9. Routing and Learning at wire speed (148810 packets/sec at 100Mbps)
- Supports 5 10/100Mbps network connections
- 5 dedicated MII interfaces can support 100BASE-TX/T4/FX PHY interfaces
- 5th Port can connect to bridge, switch or MAC type device optionally.
- Low latency design supports Class II repeater implementation
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Per-port LED display for Jabber, Partition, Activity. Global partition, RAM test fail and collision, utilization (%) for 10/100Mbps presentation
- Power on LED diagnosis. All the LED display will follow the “ON-OFF-ON-OFF-Normal” operation procedure during/after power on reset
- 160-pin PQFP

1.3 Block Diagram

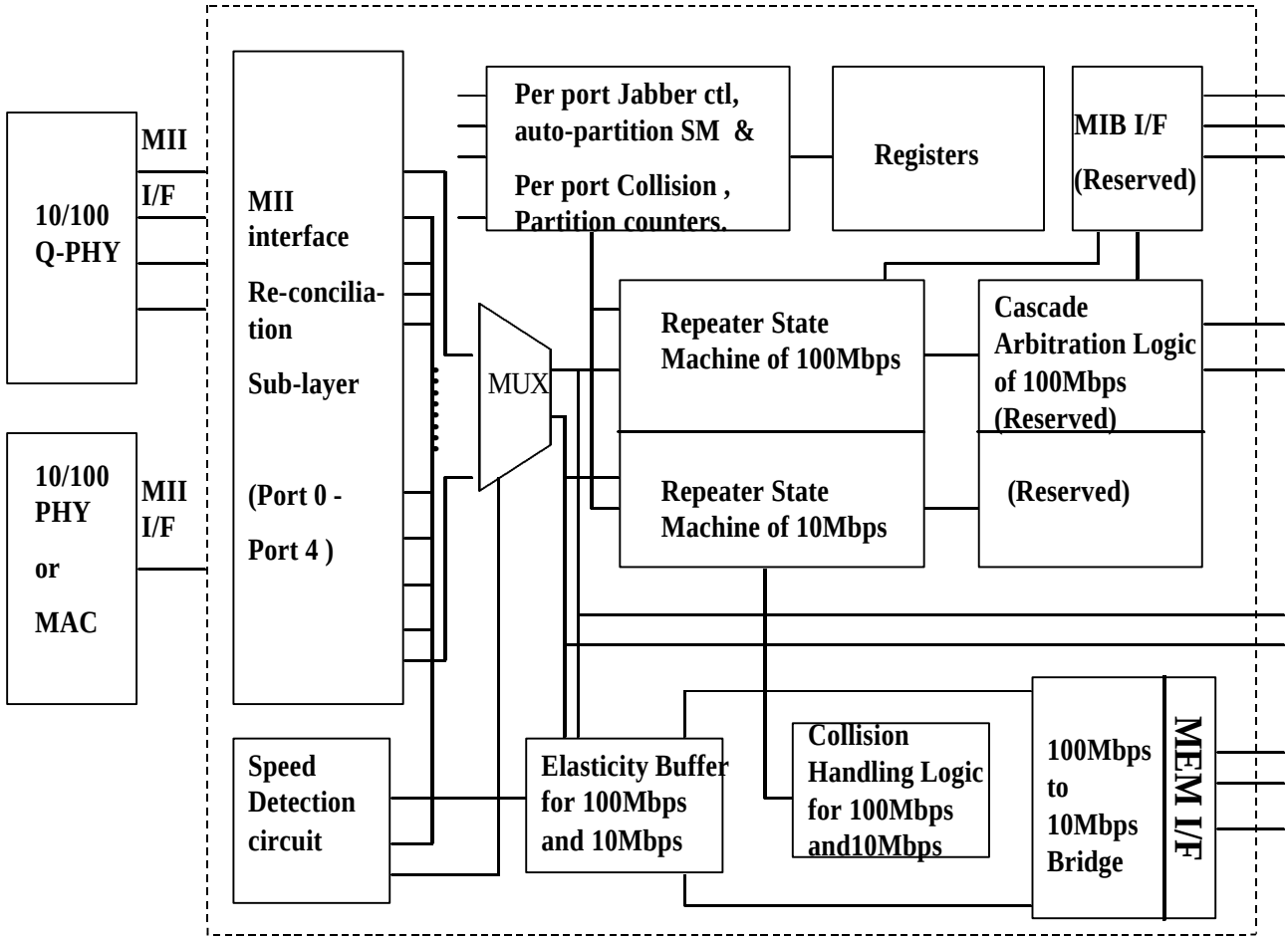


Fig - 1 Chip Block Diagram

1.4 Pin Connection Diagram (Mode 0)

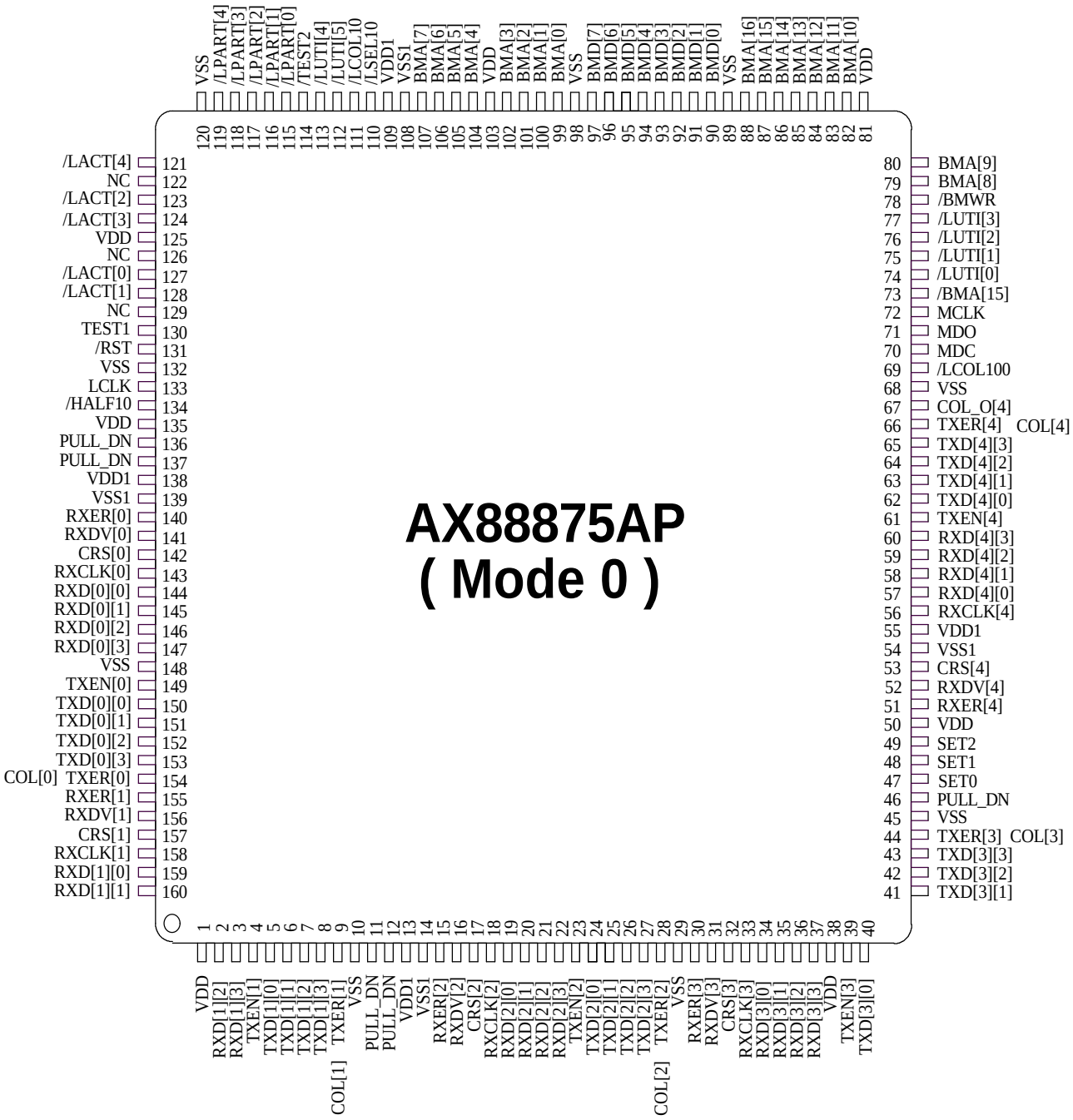


Fig - 2 Pin Connection Diagram (Mode 0)

Note : Power on configuration setup signals refer section 2.5 cross referance table

1.5 Pin Connection Diagram (Mode 1)

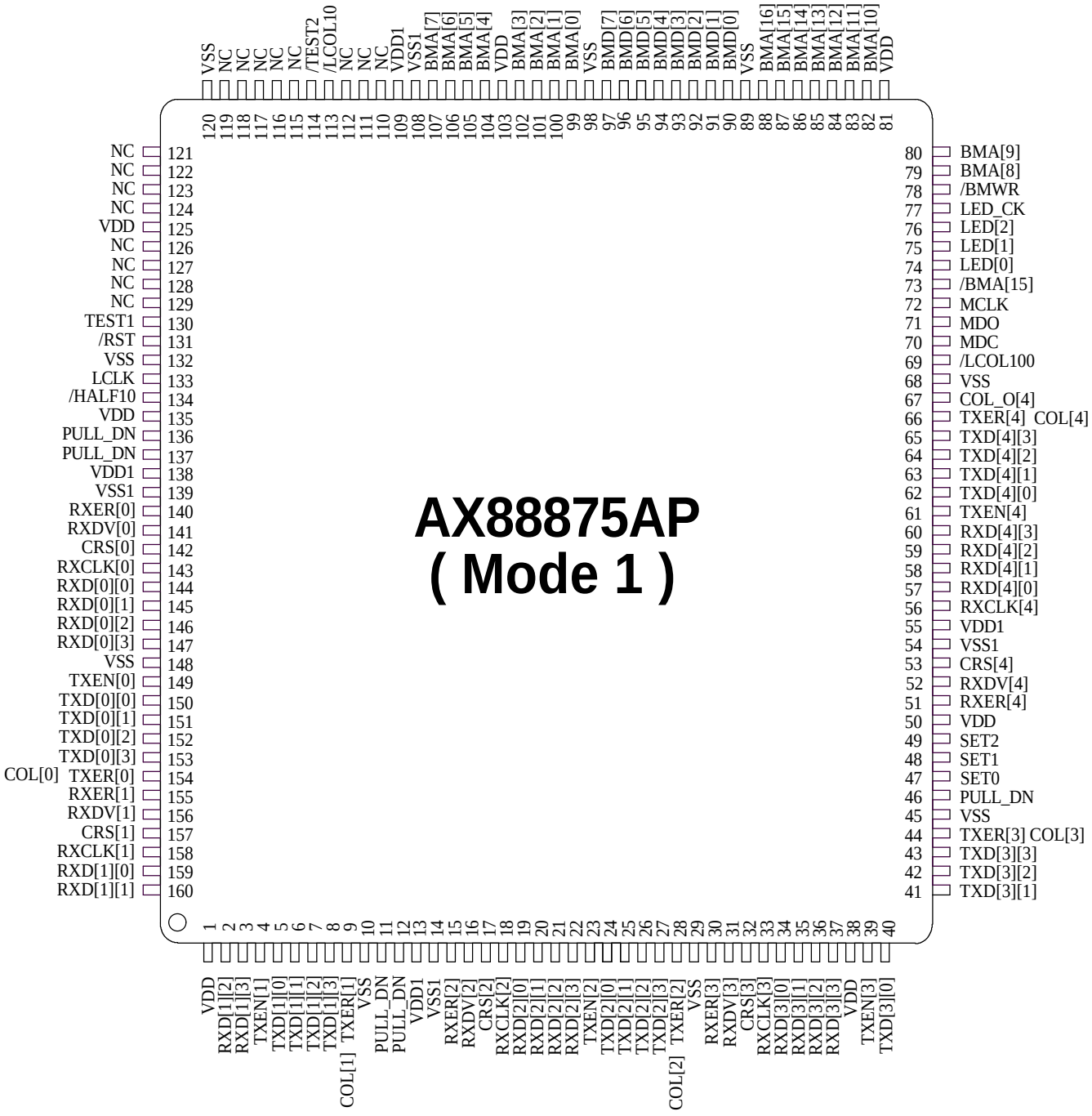


Fig - 3 Pin Connection Diagram (Mode 1)

Note : Power on configuration setup signals refer section 2.5 cross referance table

2.0 Pin Description

The following terms describe the AX88875A pinout:

All pin names with the "/" suffix are asserted low.

I	=	Input
O	=	Output
I/O	=	Input /Output

2.1 MII interfaces

Signal Name	Type	Pin No.	Description
TXER[4:0] Or COL[4:0]	O or I	66, 44, 28 9, 154	Transmit Error : When /HALF10 pin set to "high". TXER is transition synchronously with respect to the rising edge of TXCLK . Asserted high when a code violation is request to be send Collision : When /HALF10 pin set to "low". COL is input from PHY, when 10Mbps PHY is in half-duplex mode.
TXD[4:0][3:0]	O	65 – 62, 43 – 40 27 – 24, 8 – 5 153 - 150	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TXCLK. For each TXCLK period in which TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TXEN[4:0]	O	61, 39, 23 4, 149	Transmit Enable : TXEN is transition synchronously with respect to the rising edge of TXCLK. TXEN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
RXD[4:0][3:0]	I	60 – 57, 37 – 34 22 – 19, 3, 2 160, 159, 147 - 144	Receive Data : RXD [3:0] is driven by the PHY synchronously with respect to RXCLK.
RXER[4:0]	I	51, 30, 15, 155, 140	Receive Error : RXER ,is driven by PHY and synchronous to RXCLK, is asserted for one or more RXCLK periods to indicate to the port that an error has detected.
RXCLK[4:0]	I	56, 33, 18, 158, 143	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RXDV,RXD [3:0] and RXER signals from the PHY to the MII port of the repeater.
RXDV[4:0]	I	52, 31, 16, 156, 141	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RXCLK. Asserted high when valid data is present on RXD [3:0].
CRS[4:0]	I	53, 32, 17, 157, 142	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when receive medium is non-idle at full duplex mode.
COL_O[4]	O	67	Collision : Collision detection signal for port 4

2.2 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[2:0]

or
/LUTI[2:0]</td><td>O</td><td>76 - 74</td><td>LED Display Information : When MODE=”1” , Those signals indicate each port‘s Partition, Jabber, Activity, Collision (global), Repeater ID, Utilization % (global), Collision % (global) in sequence. For detail , see the LED timing specification
/LUTI[2:0] : When MODE=”0” , Those pins drive utilization[2:0] LEDs directly.

The Utilization % display define as following : (See Note 1 also)
<table>
<tr><th>Utilization %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>40</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>80+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
The Collision % display define as following :
<table>
<tr><th>Collision %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>60+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>LED_CK
or

/LUTI[3]</td><td>O</td><td>77</td><td>LED clock signal : When MODE=”1” , The signal is a discontinue clock for LED signals serial shift out. The clock period width is 40nS and last 16 cycle with every 125ms repeated.
/LUTI[3] : When MODE=”0” , This pin drive utilization[3] LED directly.</td></tr>
<tr><td>/LCOL10
or
/LUTI[4]</td><td>O/Z</td><td>113</td><td>Collision LED for 10Mbps : When MODE=”1” , This pin indicates 10Mbps repeater collision occurred.
/LUTI[4] : When MODE=”0” , This pin drive utilization[4] LED directly.</td></tr>
<tr><td>NC
or
/LUTI[5]</td><td>O</td><td>112</td><td>NC : When MODE=”1” , The pin function is reserved.

/LUTI[5] : When MODE=”0” , This pin drive utilization[5] LED directly.</td></tr>
<tr><td>/LCOL100</td><td>O/Z</td><td>69</td><td>Collision LED for 100Mbps : This pin indicates 100Mbps repeater collision occurred.</td></tr>
<tr><td>NC
or
/LACT[4:0]</td><td>O</td><td>121, 124
123, 128
127</td><td>NC : When MODE=”1” , The pin function is reserved.

/LACT[4:0] : When MODE=”0”,Those pins drive activity[4:0] LEDs directly.</td></tr>
<tr><td>NC or
/LPART[4:0]</td><td>O/OC</td><td>119-115</td><td>NC : When MODE=”1” , The pin function is reserved. or
/LPART[4:0] : When MODE=”0”, Those pins drive partition[4:0] LEDs directly.</td></tr>
</table>

Note : The Utilization % display define as following for Mode 0 LED direct driving.

Utilization %	/LUTI0	/LUTI1	/LUTI2	/LUTI3	/LUTI4	/LUTI5
0	1	1	1	1	1	1
1	0	1	1	1	1	1
5	0	0	1	1	1	1
10	0	0	0	1	1	1
15	0	0	0	0	1	1
30	0	0	0	0	0	1
60	0	0	0	0	0	0

Note 1 :
The calculation formulas of Traffic Utilization between ASIX and NetCom is difference, so you will get different results when using SmartBit (SB) testing this item.
We found the SmartBit calculate the Utilization without include 96 Bit time inter frame gap. So the utilization value can be 100%. As well as we found SB used min packet size (64 byte) and min IFG (96 bit-time) as 100% utilization. In theory, when max packet size(1518 byte) and min IFG the utilization will be more than 100%, but SB also treat it as 100%.
In our AX88875 design, we use real cable bandwidth as calculation base. We calculate the bit counts of carrier within a unit time. Because of the existence of inter frame gap, In our calculation 100% utilization is impossible. So the above two cases (64 byte packet size and 1518 byte packet size with min. IFG), we will count as 85.7% and 99.2%.
If using SB test result to indicate utilization LED the value must be modified. See the following reference table.

ASIX's Utilization%	1	5	10	15	30	60
SmartBit's Utilization%	2	7	12	17	34	68

2.3 Buffer memory pins group

Signal Name	Type	Pin No.	Description
BMA[16:0]	O	88-82, 80, 79, 107-104, 102-99	Buffer address bus.
BMD[7:0]	I/O	97-90	Buffer data bus.
/BMWR	I/O	78	Memory control pin for write.
/BMA[15]	I/O	73	Invert Buffer address 15.

2.4 Miscellaneous

Signal Name	Type	Pin No.	Description
LCLK	I	133	Local Clock : Must be run at 25Mhz . Used for transmit data to PHY devices,
/RST	I	131	Reset : The chip is reset when this signal is asserted Low.
NC or /LSEL10	I/PU	110	NC : No Connection When MODE="1". /LSEL10 : When MODE="0" , This pin select 10Mbps global LED status (utilization (%) and collision (%)) when 'low' ; Otherwise , 100Mbps LED status is selected.
NC or /LCOL10	O/ML	111	NC : No Connection When MODE="1". /LCOL : When MODE="0" , This pin drives 10Mbps collision LED directly.
MCLK	O	72	MII Clock Out : 2.5MHz 10Mbps MII reference clock
MDO	O	71	Station Management Data Out : For setup PHY auto-negotiation registers. A burst write commands are issue to setup PHY register after reset. The PHY address 4h, 5h, 6h, 7h, 8h, 9h,Ah and Bh will be written as register 4h to value 00A1h (Advertise register set to 10/100 half-duplex mode)and register 0h to value 1000h(Enable auto-negotiation).
MDC	O	70	Station Management Data Clock Out : For MDO reference clock.
TEST1	I/PD	130	Test Pin : The pin is just for test mode setting purpose only. Must be pull low when normal operation.
/TEST2	I/PU	114	Test Pin : The pin is just for test mode setting purpose only. Must be pull high when normal operation.
/HALF10	I/PU	134	Half-duplex mode in 10Mbps : Pull low with 10K ohm resister for 10Mbps PHY in half-duplex mode.
PULL_DN	I	11, 12, 46 136, 137	Pull Down : Those pins are not use for application. Designer must pull them down or tie to ground.
SET2, SET1, SET0	O	49, 48, 47	Setup Pins : Those pins are power on configuration use. Default internal pull high. If necessary, pull low with 10K ohm resister. **Tie to ground is prohibited.**
VDD	I	1, 13, 38 50, 55, 81 103, 109 125, 135 138	POWER : +5V +/-5%
VSS	I	10, 14, 29 45, 54, 68 89, 98, 108, 120, 132, 139 148,	POWER: 0V

2.5 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
OPT[4]	COL_O[4]	OPT[4] : Option for external device type to connect to port 4. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
TXM_MODE	SET2	TXM_MODE : Option for internal used. Default 'high' user may pull the pin 'low' with 10K ohm resister for reserve transmition mode alternaty.
MODE	SET1	MODE = 0 : Direct LED display mode. MODE = 1 : Rich LED display mode.
EN_FLOW_CTL	SET0	EN_FLOW_CTL = 0 : Disable flow control function. EN_FLOW_CTL = 1 : Enable flow control function.
ST_FW	TXD[4][3]	ST_FW = 0 : Fragment free forwording mode. ST_FW = 1 : Store & forword forwording mode.
ENTRIES	TXD[4][2]	ENTRIES = 0 : 1024 entries supported ENTRIES = 1 : 256 entries supported
MEM_SIZE[1] MEM_SIZE[0]	TXD[4][1] TXD[4][0]	MEM_SIZE[1] MEM_SIZE[0] SIZE (K) 1 1 32K 1 0 64K 0 1 128K 0 0 N/A
/IR_ACT_EN	/BMWR	Inter Repeater Active Input Pin Enable : Designer must keep the pin pull high to disable the function.

All of the above signals are pull-up for default values.

3.0 Functional Description

3.1 Repeater State Machine

The repeater state machine is used to control repeater behavior, generates right signal in corresponding states. The repeater state machine is in Idle state when there is no carrier presented on any ports **.** When there is only one port has receive activity, the repeater state machine will enter Data - forwarding State to ensure correct data forwarding to other connected ports. If collision happens anytime, The repeater state machine detects collision then send jam pattern to all ports until collision ceases.

idle State

The idle state happens when these conditions exists:

a. /RST is low.
b. All CRS[4:0] are not asserted high in single chip application.

Data Forwarding State

The state happens when the condition exists:

a. Only one signal asserted among CRS[4:0] in single chip application.

The repeater state machine stores receiving packet and transmits to all other ports except for

1. The port is jabbered.
2. The port is isolated.

Collision State

The Collision State happens when these conditions exists:

a. There are two or more signals asserted high among CRS[4:0] in single chip system.
b. Only one carrier exists but RXDV still low exceeds 4 clock cycles in 100BASE-T. The repeater sends collision pattern to all ports.

One Port Left State

The state happens only when there is no collision but still one port which experienced collision has receive activity. The repeater remains send collision pattern to all ports except the port.

3.2 RXE /TXE CONTROL

Idle state

The repeater sends no data to any port.

RXE(ALL) = 0.
TXE(ALL) = 0.

Data Forwarding state

If ACTIVE(X) = 1, X is the local connected port,

RXE(X) = 1, RXE(ALL-X) = 0.
TXE(X) = 0, TXE(ALL-X) = 1.

Collision state

The repeater sends jam pattern to all ports.

RXE(ALL) = 0.
TXE(ALL) = 1.

One Port Left state

The repeater sends jam pattern to all other port except for the still activity port.

RXE(ALL) = 0.
TXE(ALL-X) = 1. Suppose X is the one left port.

3.3 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration (64K bit times for AX88875A), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber function will be clear and re-enable reception and transmission.

3.4 Partition State Machine

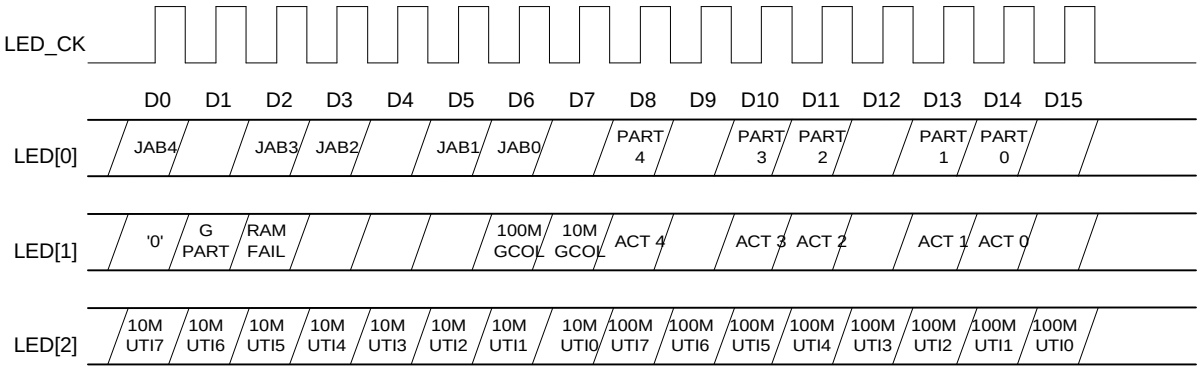
The partition state machine is used to protect network from being upset when a port suffer continuous collision, each port uses a partition state machine to detect and prevent this condition. When a port suffer from continuous 64 times of collision events, then it goes to partition state. The partitioned port will be not released until a packet without collision be transmitted(more than 512 bit times for AX88875A) or reset the repeater.

3.5 LED Display Interface

AX88875A provides per-port LED status indication for partition, jabber, activity and support rate - based LED for global partition and collision, utilization (%) for 10/100Mbps. .Detail function is described on the previous pin description(LED interface). LED[2:0] are all active low. There are two display ways : complicated and simple way. It depends on the setting of MODE.

Rich LED display application (MODE = 1)

LED[2:0] Status Driver Wave-form as follows :



Notes: a. PART4~0indicates partition status for each port
b. JAB4~0 indicates jabber status for each port
c. ACT4~0 indicates activity status for each port
d. RID2~0 is the ID of repeater chip
e. 10M UTI4~0 indicate global utilization rate of 10Mbps for each 104.8ms sampling period.
f. 100M UTI4~0 indicate global utilization rate of 100Mbps for each 104.8ms sampling period.
g. 10M GCOL indicate global collision
h. 100M GCOL indicate global collision
i. GPART : indicate global partition.
J. RAM FAIL : Bridge RAM test fail.

It must use external shift register to decode data on LED[2:0]. The application shows as follows:

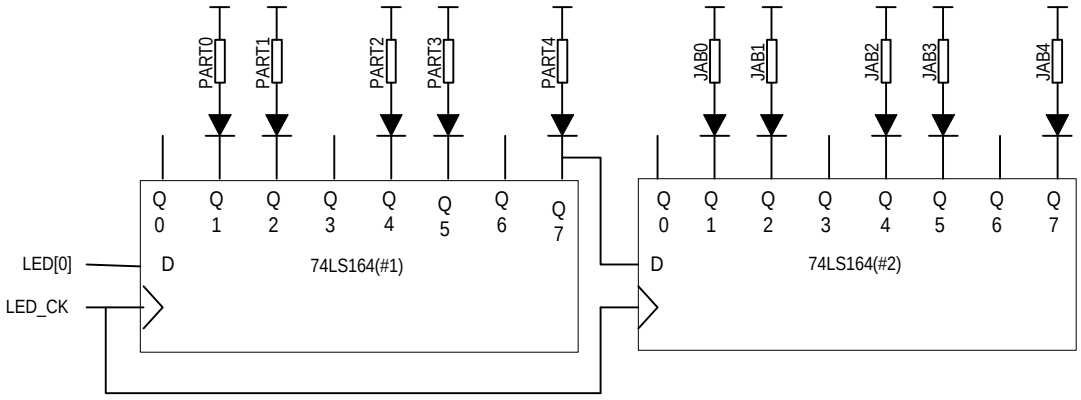


Fig - 4 Application for LED display

If the user don‘t want to show jabber status, take away the latter 74LS164(#2). The application is the same for LED[2:1].

Simple LED display application (MODE=0)

LED display for mode 1 vs. mode 0 referance table.

Mode 1	Mode 0	Mode 1	Mode 0	Mode 1	Mode 0
NC	/PART[0]	NC	/ACT[0]	LED[0]	/UTI[0]
NC	/PART[1]	NC	/ACT[1]	LED[1]	/UTI[1]
NC	/PART[2]	NC	/ACT[2]	LED[2]	/UTI[2]
NC	/PART[3]	NC	/ACT[3]	LED_CK	/UTI[3]
NC	/PART[4]	NC	/ACT[4]	NC	/UTI[4]
				NC	/UTI[5]
				NC	/LCOL10
				/LCOL100	/LCOL100

4.0 INTERNAL REGISTERS

4.1 Configuration Register (CONFIG)

Bit	Bit Name	Access	Bit Description
D9	/HALF10	R/W	Half-duplex mode in 10Mbps : “low” resister to 10Mbps PHY in half-duplex mode. “high” resister to 10Mbps PHY in full-duplex mode.
D8	OPT[4]	R/W	OPT[4] : Option for external device type to connect to port 4. Default ‘high’ is for PHY type device. Otherwise, ‘low’ for bridge, switch or MAC type device.
D7	TXM_MODE	R/W	TXM_MODE : Option for internal used. Default ‘high’ user may pull the pin ‘low’ with 10K ohm resister for reserve transmition mode alternaty.
D6	MODE	R/W	MODE = 0 : Single chip repeater application. MODE = 1 : Multiple chips cascaded repeater application.
D5	EN_FLOW_ CTL	R/W	EN_FLOW_CTL = 0 : Disable flow control function. EN_FLOW_CTL = 1 : Enable flow control function.
D4	ST_FW	R/W	ST_FW = 0 : fragment-free mode ST_FW =1 : Store-n-Forward mode
D3	ENTRIES	R/W	ENTRIES = 0 : 1024 entries supported ENTRIES = 1 : 256 entries supported
D2-1	MEM_SIZE[1] MEM_SIZE[0]	R/W	MEM_SIZE[1] MEM_SIZE[1] SIZE (K) 1 1 32K 1 0 64K 0 1 128K 0 0 N/A
D0	/IR_ACT_EN	R/W	Inter Repeater Active Input Pin Enable : Designer must keep the pin pull high to disable the function.

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.5	+7	V
Input Voltage	Vin	Vss-0.5	Vdd+0.5	V
Output Voltage	Vout	Vss-0.5	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+235	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+4.75	+5.25	V

5.3 DC Characteristics

(Vdd=4.75V to 5.25V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.5	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

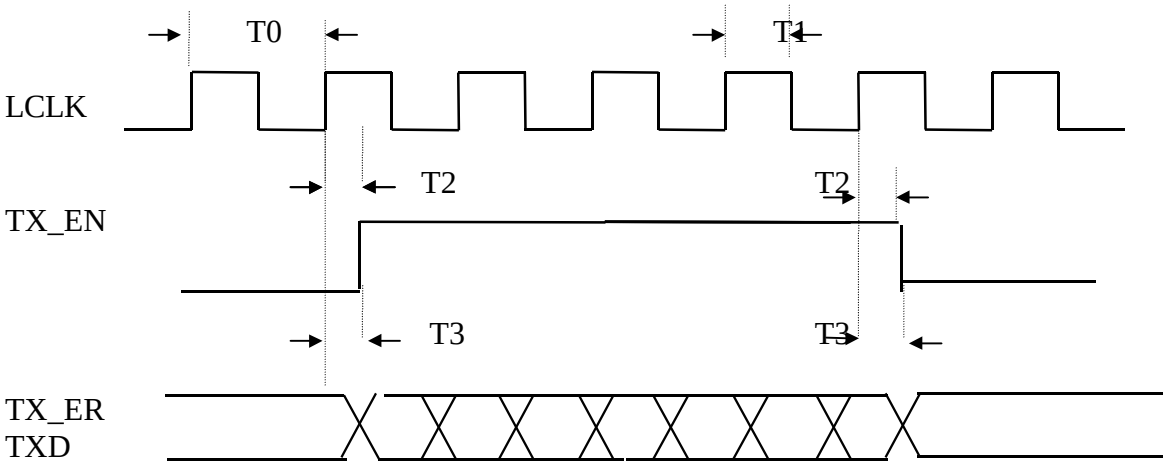
Description	SYM	Min	Tpy	Max	Units
Power Consumption	Pc		120	160	mA

Note :

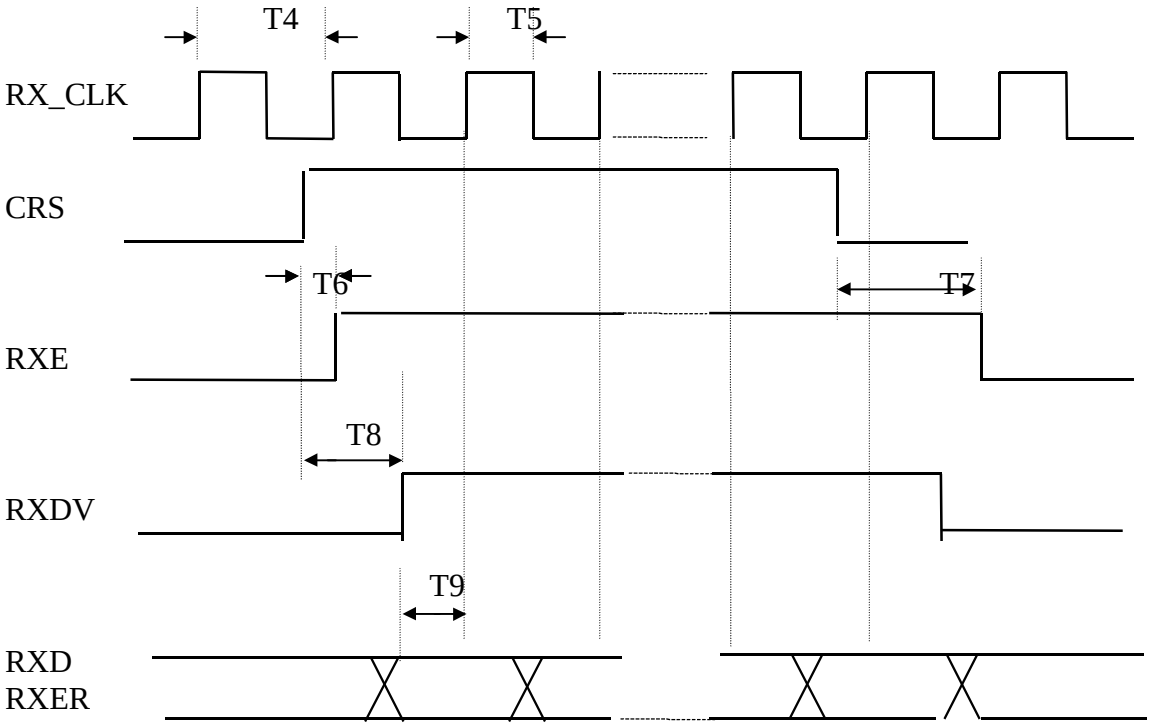
1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

5.4 AC specifications

5.4.1 MII Interface Timing Tx & Rx

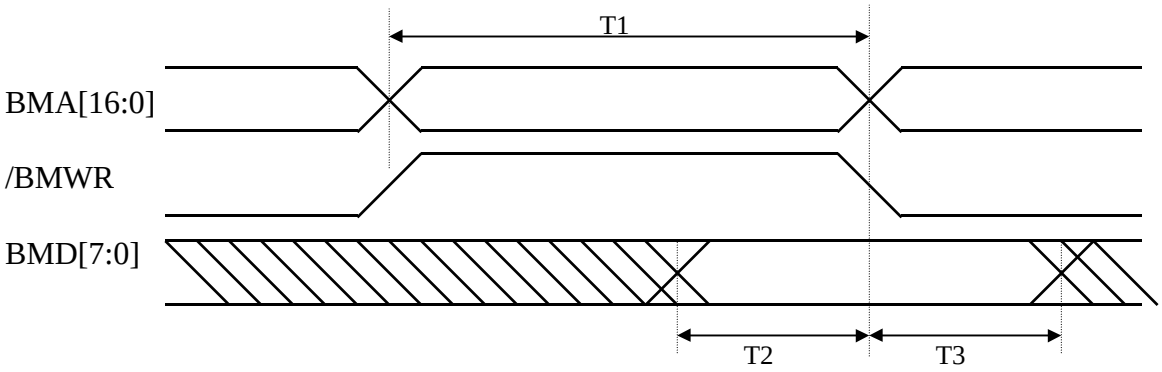


Symbol	Description	Min	Typ.	Max	Units
T0	Local Clock Cycle Time	39.996	40	40.004	ns
T1	Local Clock High Time	14	20	26	ns
T2	TX_EN Delay from LCLK High	7.440		21.760	ns
T3	TX_ER or TXD Delay from LCLK High	3.410		13.320	ns

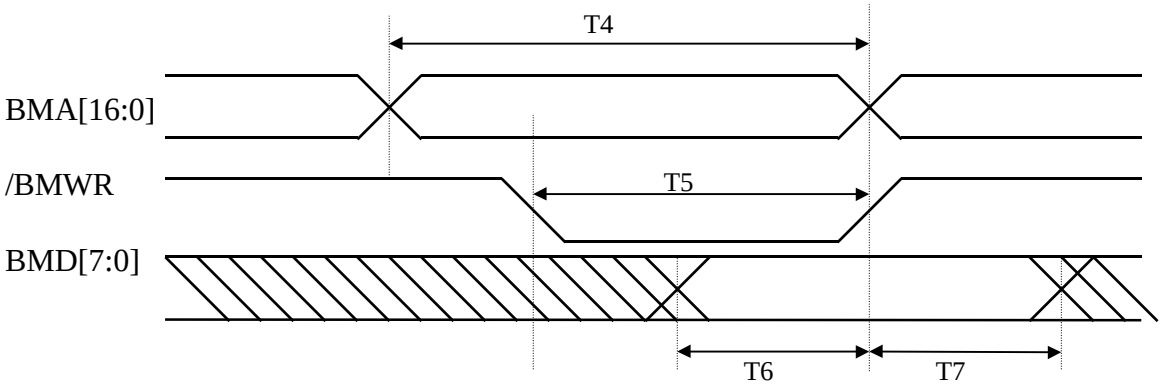


Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXE Assertion Delay			20	ns
T7	CRS to RXE De-assertion Delay	160		200	ns
T8	CRS to RXDV Delay Requirement	40		160	ns
T9	RXD or RXDV or RX_ER setup to RX_CLK rise time	10		-	ns

5.4.2 SRAM read cycle and write cycle

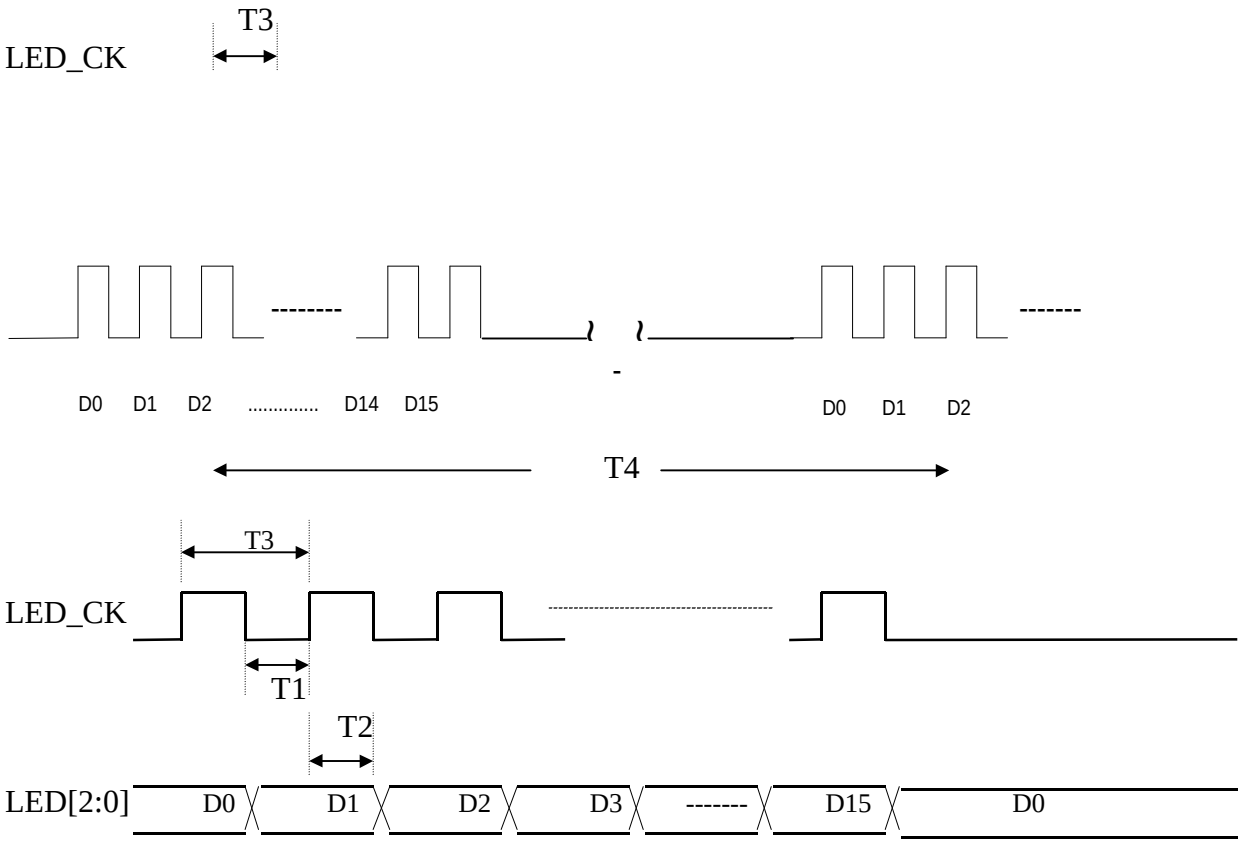


Symbol	Description	Min	Max	Units
T1	Read Cycle Time	40	-	ns
T2	BMD[7:0] Setup Time	3	-	ns
T3	BMD[7:0] Hold Time	3	-	ns



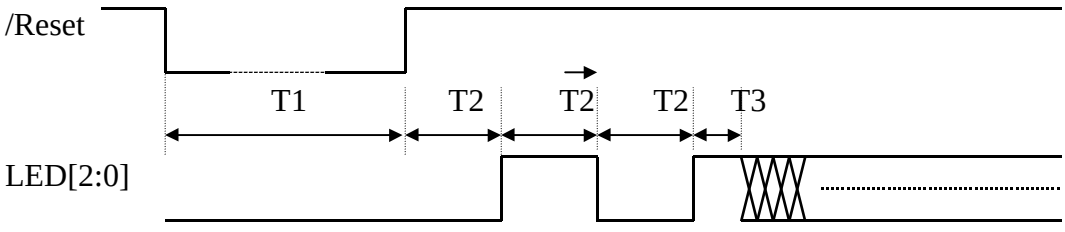
Symbol	Description	Min	Max	Units
T4	Write Cycle Time	38	-	ns
T5	Write Pulse Wtdth	20	-	ns
T6	BMD[7:0] Data Valid to End of Write	14	-	ns
T7	BMD[7:0] Data Hold from End of Write	1		ns

5.4.3 LED DISPLAY



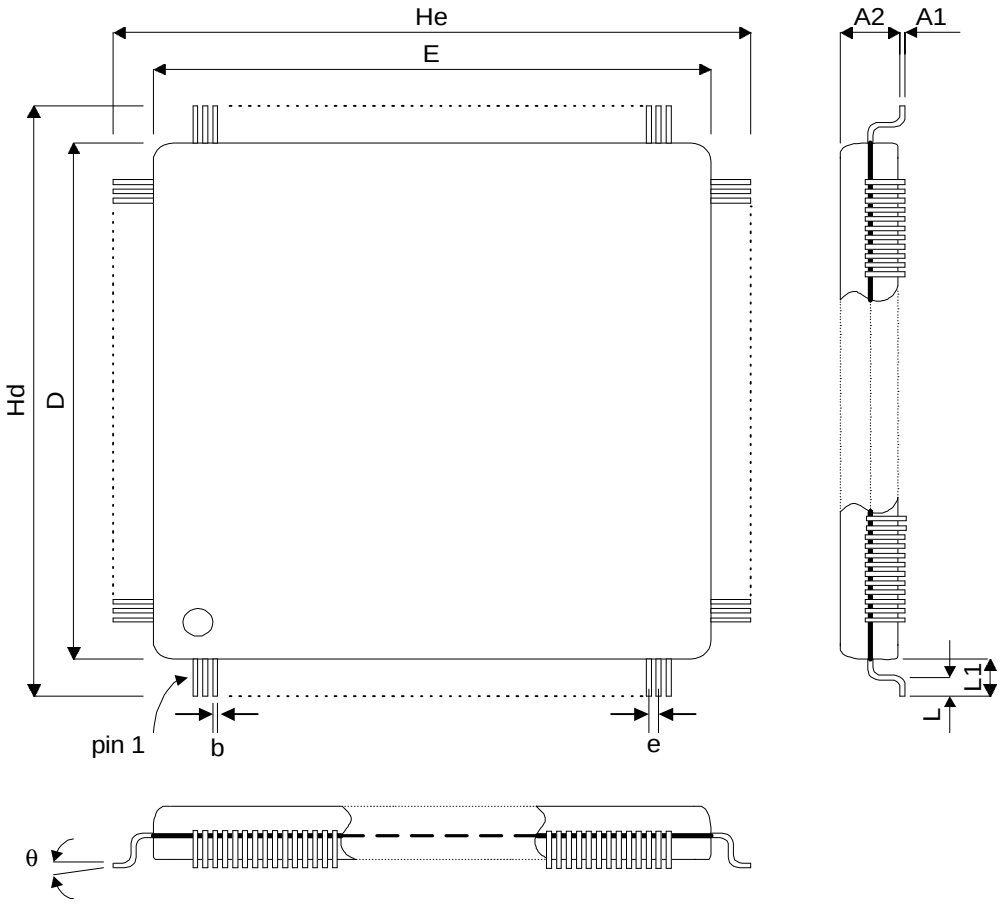
Symbol	Description	Min	Typ.	Max	Units
T1	LED setup to LED_CK High	190		200	ns
T2	LED hold from LED_CK High	200		210	ns
T3	LED_CK Period Width		400		ns
T4	continuous 16 LED_CK Cycle Time		52.4		ms

5.4.4 LED Display After Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

6.0 PACKAGE INFORMATION



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.25		
A2	3.15	3.40	3.65
b	0.22	0.30	0.38
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e		0.65	
Hd	30.95	31.20	31.45
He	30.95	31.20	31.45
L	0.73		1.03
L1		1.60	
θ	0		7°

Appendix A: Applications

Two type of applications for AX88875A are illustrated bellow.

A.1 Stand-along 5-ports 10/100Mbps HUB Application

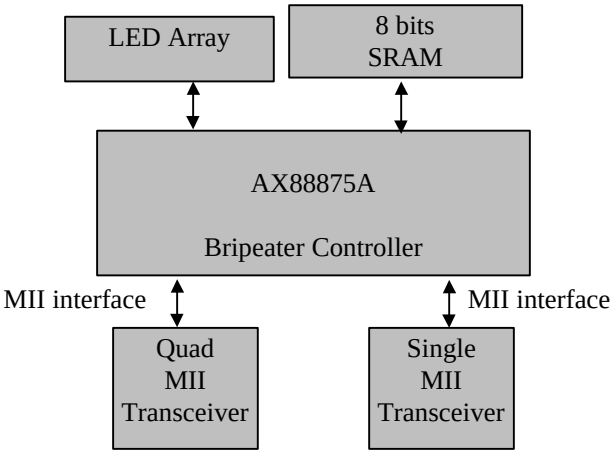


Fig - 5 Stand-along 5-ports 10/100Mbps HUB Application

A.2 Stand-along 4-ports 10/100Mbps HUB with one MAC Application

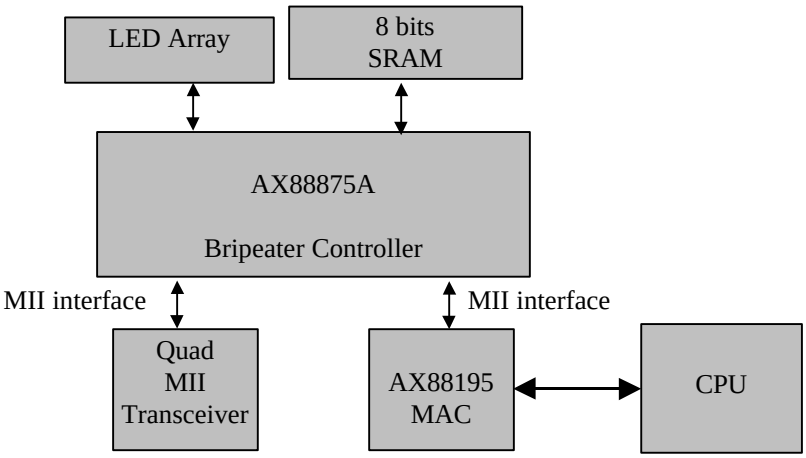
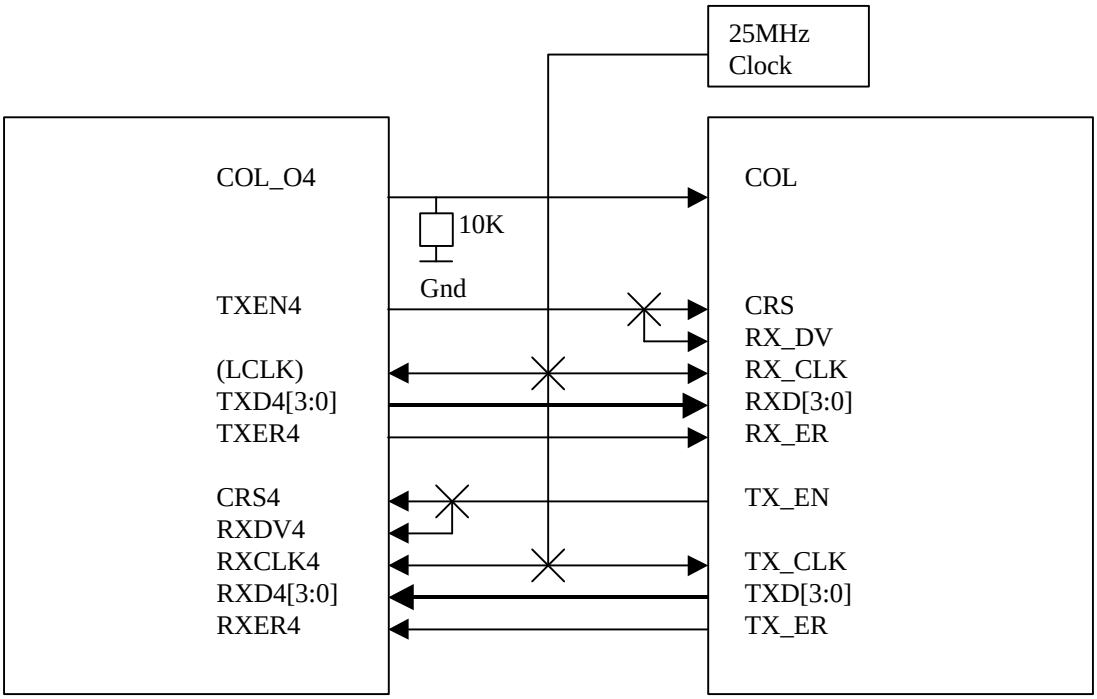


Fig - 6 Stand-along 4-ports 10/100Mbps HUB with one MAC Application

Appendix B: Using MII I/F connects to MAC

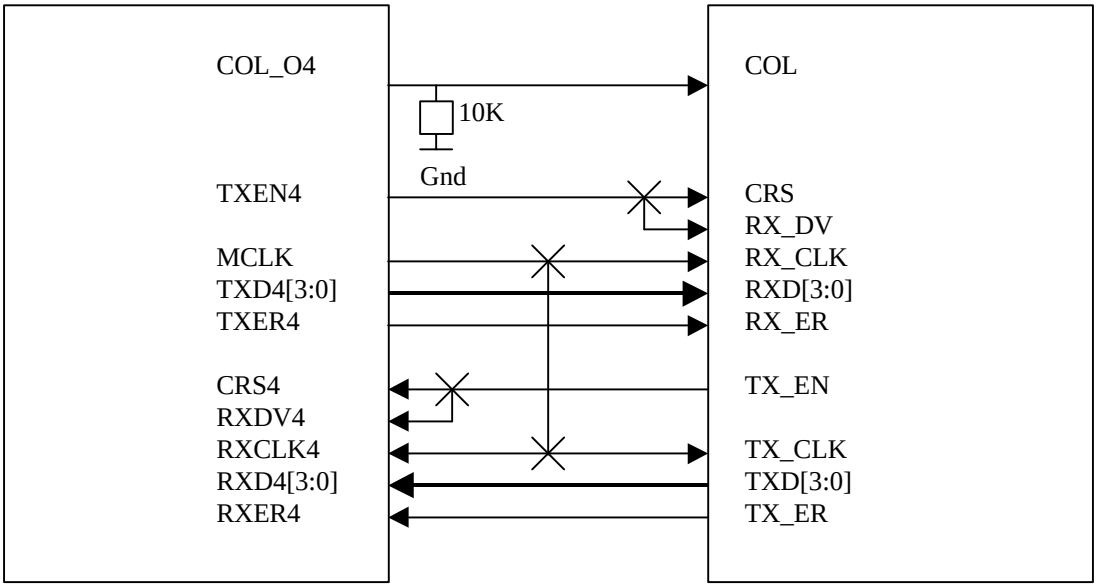
Using MII interface to connect to MAC type device application for AX88875A is illustrated bellow.



AX88875 / Repeater **AX88195 / MAC**

Note : 1. The MAC needs to run at halfduplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embbeded MAC can also refer to this example

Using MII interface to connect to 10Mbps MAC device application for AX88875A is illustrated bellow.



AX88875 / Repeater **10Mbps MAC**