ASD0500

Dual Ultra Low Power 20/40/65/80 MSPS, 12/13-bit Analog-to-Digital Converter

Features

- 13-bit resolution
- 20/40/65/80 MSPS maximum sampling rate
- Ultra-Low Power Dissipation: 30/55/85/102 mW
- 72 dB SNR at 80MSPS and 8 MHz F_{IN}
- Internal reference circuitry
- 1.8 V core supply voltage
- 1.7 – 3.6 V I/O supply voltage
- Parallel CMOS output
- 64 pin QFN and TQFP package
- Dual channel
- Pin compatible with ASD0400

Applications

- Handheld Communication, PMR, SDR
- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- Baseband / IF Communication
- Video Digitizing
- CCD Digitizing

Description

The ASD0500 is a high performance low power dual analog-to-digital converter (ADC). The ADC employs internal reference circuitry, a CMOS control interface and CMOS output data, and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Several idle modes with fast startup times exist. Each channel can independently be powered down and the entire chip can either be put in Standby Mode or Power Down mode. The different modes are optimized to allow the user to select the mode resulting in the smallest possible energy consumption during idle mode and startup.

The ASD0500 has a highly linear THA optimized for frequencies up to 70 MHz. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave and CMOS clock inputs.

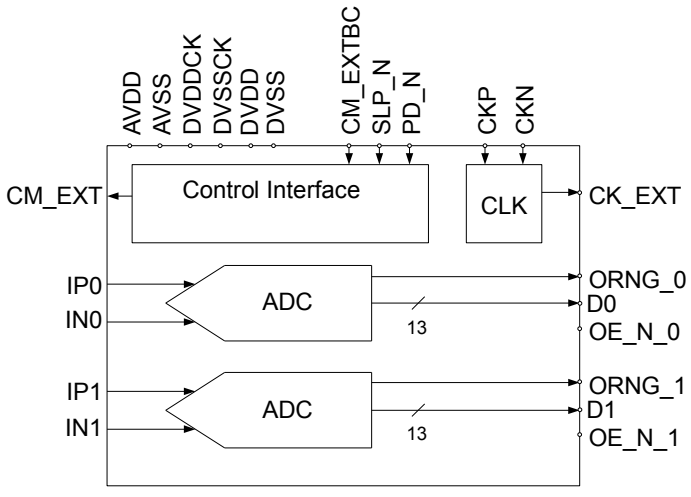

Figure 1: Functional Block Diagram

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Specifications

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, 20/40/65/80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
DC accuracy					
No missing codes			Guaranteed		
Offset error	Midscale offset		1		LSB
Gain error	Full scale range deviation from typical			+/- 6	%FS
Gain matching	Gain matching between channels. +/- 3 sigma value at worst case conditions		+/- 0.5		%FS
DNL	Differential nonlinearity (12-bit level)		+/- 0.2		LSB
INL	Integral nonlinearity (12-bit level)		+/- 0.6		LSB
V_{CM}	Common mode voltage output		$V_{AVDD}/2$		V
Analog Input					
Input common mode	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
Full scale range, Normal	Differential input voltage range,		2.0		Vpp
Full scale range, Option	Differential input voltage range, 1V (see section Reference Voltages)		1.0		Vpp
Input capacitance	Differential input capacitance		2		pF
Bandwidth	Input Bandwidth	500			MHz
Power Supply					
Core Supply Voltage	Supply voltage to all 1.8V domain pins. See Pin Configuration and Description	1.7	1.8	2.0	V
I/O Supply Voltage	Output driver supply voltage (OVDD). Should be higher than or equal to Core Supply Voltage ($V_{OVDD} \geq V_{DVDD}$)	1.7	2.5	3.6	V

ASD0500L20

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, FS=20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 2 MHz		72.5		dBFS
	F_{IN} = 8 MHz	71.5	72.2		dBFS
	$F_{IN} \cong FS/2$		72.1		dBFS
	F_{IN} = 20 MHz		71.6		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	F_{IN} = 2 MHz		72.4		dBFS
	F_{IN} = 8 MHz	71.0	72.0		dBFS
	$F_{IN} \cong FS/2$		71.7		dBFS
	F_{IN} = 20 MHz		71.3		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 2 MHz		87		dBc
	F_{IN} = 8 MHz	75	85		dBc
	$F_{IN} \cong FS/2$		80		dBc
	F_{IN} = 20 MHz		80		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 2 MHz		-90		dBc
	F_{IN} = 8 MHz	-85	-95		dBc
	$F_{IN} \cong FS/2$		-95		dBc
	F_{IN} = 20 MHz		-95		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 2 MHz		-87		dBc
	F_{IN} = 8 MHz	-75	-85		dBc
	$F_{IN} \cong FS/2$		-80		dBc
	F_{IN} = 20 MHz		-80		dBc
ENOB	Effective number of Bits				
	F_{IN} = 2 MHz		11.7		bits
	F_{IN} = 8 MHz	11.5	11.7		bits
	$F_{IN} \cong FS/2$		11.6		bits
	F_{IN} = 20 MHz		11.6		bits
Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-105		dB
Power Supply					
Analog supply current			11.6		mA
Digital supply current	Digital core supply		1.8		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT enabled		2.9		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT disabled		2.4		mA
Analog power			20.9		mW
Digital power	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		9.2		mW
Total power Dissipation	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		30.1		mW
Power Down			9.9		µW
Sleep Mode 1	Power Dissipation, Sleep mode one channel		20.5		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels		9.2		mW
Clock Inputs					
Max. Conversion Rate		20			MSPS
Min. Conversion Rate				3	MSPS

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AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, FS=40MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 2 MHz		72.5		dBFS
	F_{IN} = 8 MHz	71.9	72.7		dBFS
	$F_{IN} \cong FS/2$		72.0		dBFS
	F_{IN} = 30 MHz		70.8		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	F_{IN} = 2 MHz		71.7		dBFS
	F_{IN} = 8 MHz	71.0	72.1		dBFS
	$F_{IN} \cong FS/2$		71.5		dBFS
	F_{IN} = 30 MHz		71.2		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 2 MHz		81		dBc
	F_{IN} = 8 MHz	75	81		dBc
	$F_{IN} \cong FS/2$		80		dBc
	F_{IN} = 30 MHz		80		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 2 MHz		-90		dBc
	F_{IN} = 8 MHz	-85	-95		dBc
	$F_{IN} \cong FS/2$		-95		dBc
	F_{IN} = 30 MHz		-90		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 2 MHz		-81		dBc
	F_{IN} = 8 MHz	-75	-81		dBc
	$F_{IN} \cong FS/2$		-80		dBc
	F_{IN} = 30 MHz		-80		dBc
ENOB	Effective number of Bits				
	F_{IN} = 2 MHz		11.6		bits
	F_{IN} = 8 MHz	11.5	11.7		bits
	$F_{IN} \cong FS/2$		11.6		bits
	F_{IN} = 30 MHz		11.5		bits
Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-100		dB
Power Supply					
Analog supply current			21.1		mA
Digital supply current	Digital core supply		3.3		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT enabled		5.3		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT disabled		4.4		mA
Analog power			38.0		mW
Digital power	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		16.9		mW
Total power Dissipation	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		54.9		mW
Power Down			9.7		µW
Sleep Mode 1	Power Dissipation, Sleep mode one channel		36.1		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels		14.2		mW
Clock Inputs					
Max. Conversion Rate		40			MSPS
Min. Conversion Rate				20	MSPS

ASD0500L65

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, FS=65MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 8 MHz	71.6	72.6		dBFS
	F_{IN} = 20 MHz		71.8		dBFS
	$F_{IN} \cong FS/2$		71.5		dBFS
	F_{IN} = 40 MHz		70.4		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	F_{IN} = 8 MHz	70.5	71.7		dBFS
	F_{IN} = 20 MHz		71.7		dBFS
	$F_{IN} \cong FS/2$		71.1		dBFS
	F_{IN} = 40 MHz		70.0		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 8 MHz	75	81		dBc
	F_{IN} = 20 MHz		84		dBc
	$F_{IN} \cong FS/2$		79		dBc
	F_{IN} = 40 MHz		77		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 8 MHz	-85	-95		dBc
	F_{IN} = 20 MHz		-95		dBc
	$F_{IN} \cong FS/2$		-95		dBc
	F_{IN} = 40 MHz		-95		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 8 MHz	-75	-81		dBc
	F_{IN} = 20 MHz		-84		dBc
	$F_{IN} \cong FS/2$		-79		dBc
	F_{IN} = 40 MHz		-79		dBc
ENOB	Effective number of Bits				
	F_{IN} = 8 MHz	11.4	11.6		bits
	F_{IN} = 20 MHz		11.6		bits
	$F_{IN} \cong FS/2$		11.5		bits
	F_{IN} = 40 MHz		11.3		bits
Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-95		dB
Power Supply					
Analog supply current			32.8		mA
Digital supply current	Digital core supply		5.0		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT enabled		8.2		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT disabled		6.6		mA
Analog power			59.0		mW
Digital power	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		25.5		mW
Total power Dissipation	OVDD = 2.5V, ~5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		84.5		mW
Power Down			9.3		µW
Sleep Mode 1	Power Dissipation, Sleep mode one channel		55.3		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels		20.4		mW
Clock Inputs					
Max. Conversion Rate		65			MSPS
Min. Conversion Rate				40	MSPS

ASD0500L80

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, FS=80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13 bit output, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 8 MHz	70.4	72.0		dBFS
	F_{IN} = 20 MHz		71.7		dBFS
	F_{IN} = 30 MHz		71.2		dBFS
	$F_{IN} \cong FS/2$		70.7		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	F_{IN} = 8 MHz	69.5	70.5		dBFS
	F_{IN} = 20 MHz		70.5		dBFS
	F_{IN} = 30 MHz		70.4		dBFS
	$F_{IN} \cong FS/2$		70.3		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 8 MHz	74	77		dBc
	F_{IN} = 20 MHz		78		dBc
	F_{IN} = 30 MHz		78		dBc
	$F_{IN} \cong FS/2$		78		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 8 MHz	-80	-95		dBc
	F_{IN} = 20 MHz		-90		dBc
	F_{IN} = 30 MHz		-90		dBc
	$F_{IN} \cong FS/2$		-85		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 8 MHz	-74	-77		dBc
	F_{IN} = 20 MHz		-78		dBc
	F_{IN} = 30 MHz		-78		dBc
	$F_{IN} \cong FS/2$		-78		dBc
ENOB	Effective number of Bits				
	F_{IN} = 8 MHz	11.3	11.4		bits
	F_{IN} = 20 MHz		11.4		bits
	F_{IN} = 30 MHz		11.4		bits
	$F_{IN} \cong FS/2$		11.4		bits
Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-95		dB
Power Supply					
Analog supply current			39.7		mA
Digital supply current	Digital core supply		6.0		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT enabled		9.4		mA
Output driver supply	2.5V output driver supply, sine wave input, F_{IN} = 1 MHz, CK_EXT disabled		7.7		mA
Analog power			71.5		mW
Digital power	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		30.0		mW
Total power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1 MHz, CK_EXT disabled		101.5		mW
Power Down			9.1		µW
Sleep Mode 1	Power Dissipation, Sleep mode one channel		66.4		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels		24.1		mW
Clock Inputs					
Max. Conversion Rate		80			MSPS
Min. Conversion Rate				65	MSPS

Digital and timing Specifications

AVDD=1.8V, DVDD=1.8V, DVDDCK=1.8V, OVDD=2.5V, Conversion Rate: Max specified, 50% clock duty cycle, -1dBFS input signal, 5 pF capacitive load on data outputs, unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
Clock Inputs					
Duty Cycle		20		80	% high
Compliance			CMOS, LVDS, LVPECL, Sine Wave		
Input range	Differential input swing	0.4			Vpp
Input range	Differential input swing, sine wave clock input	1.6			Vpp
Input common mode voltage	Keep voltages within ground and voltage of OVDD	0.3		V_{OVDD} -0.3	V
Input capacitance	Differential		2		pF
Timing					
T_{PD}	Start up time from Power Down Mode to Active Mode			900	clock cycles
T_{SLP}	Start up time from Sleep Mode to Active Mode			20	clock cycles
T_{OVR}	Out of range recovery time		1		clock cycles
T_{AP}	Aperture Delay		0.8		ns
Єrms	Aperture jitter		< 0.5		ps
T_{LAT}	Pipeline Delay		12		clock cycles
T_D	Output delay (see timing diagram). 5pF load on output bits	3.0		10.0	ns
T_{DC}	Output delay relative to CK_EXT (see timing diagram)	1.0		6.0	ns
Logic Inputs					
V_{HI}	High Level Input Voltage. $V_{OVDD} \geq 3.0V$	2			V
V_{HI}	High Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0.8 ·V_{OVDD}			V
V_{LI}	Low Level Input Voltage. $V_{OVDD} \geq 3.0V$	0		0.8	V
V_{LI}	Low Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0		0.2 ·V_{OVDD}	V
I_{HI}	High Level Input leakage Current			+/-10	µA
I_{LI}	Low Level Input leakage Current			+/-10	µA
C_I	Input Capacitance		3		pF
Logic Outputs					
V_{HO}	High Level Output Voltage	V_{OVDD} -0.1			V
V_{LO}	Low Level Output Voltage			0.1	V
C_L	Max capacitive load. Post-driver supply voltage equal to digital supply voltage $V_{OVDD} = V_{DVDD}$			5	pF
C_L	Max capacitive load. Post-driver supply voltage above 2.25V (1)		10		pF

(1) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum

Timing Diagram

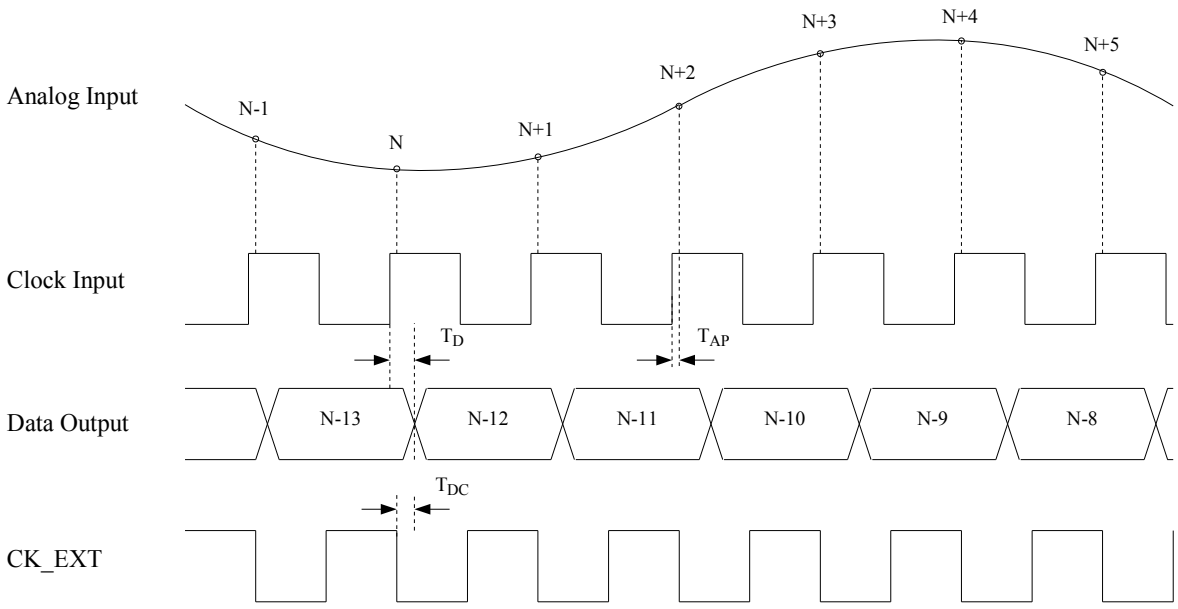

Figure 2: Timing Diagram

Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied for short periods of time. Exposure to absolute maximum rating conditions for an extended period of time may reduce device lifetime.

Table 1:

Pin	Pin	Rating
AVDD	AVSS	-0.3V to +2.3V
DVDD	DVSS	-0.3V to +2.3V
AVSS, DVSSCK, DVSS, OVSS	DVSS	-0.3V to +0.3V
OVDD	OVSS	-0.3V to +3.9V
IPx, INx, analog inputs and outputs	AVSS	-0.3V to +2.3V
Digital outputs	OVSS	-0.3V to +3.9V
CKP, CKN	DVSSCK	-0.3V to +3.9V
Digital Inputs	OVSS	-0.3V to +3.9V
Operating temperature		-40 to +85 °C
Storage temperature		-60 to +150 °C
Soldering Profile Qualification		J-STD-020

This device can be damaged by ESD. Even though this product is protected with state-of-the-art ESD protection circuitry, damage may occur if the device is not handled with appropriate precautions. ESD damage may range from device failure to performance degradation. Analog circuitry may be more susceptible to damage as very small parametric changes can result in specification incompliance.

Pin Configuration and Description

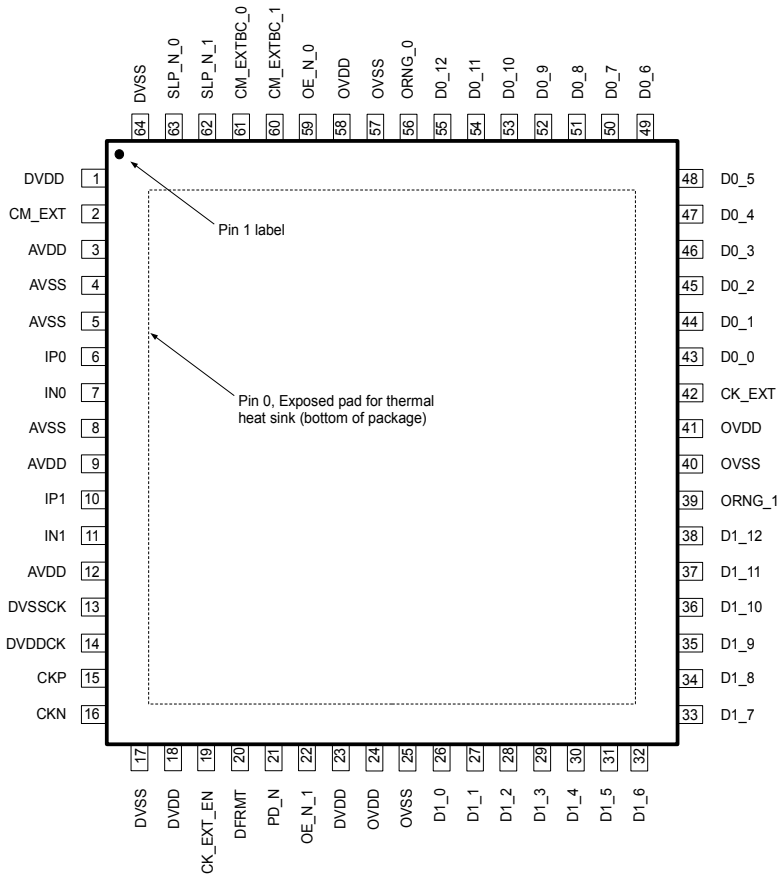

Figure 3: Package Drawing, 64-pin QFN or TQFP

Table 2: Pin function

Pin #	Name	Description
1, 18, 23	DVDD	Digital and I/O-ring pre driver supply voltage, 1.8V
2	CM_EXT	Common Mode voltage output
3, 9, 12	AVDD	Analog supply voltage, 1.8V
4, 5, 8	AVSS	Analog ground
6, 7	IP0, IN0	Analog input Channel 0 (non-inverting, inverting)
10, 11	IP1, IN1	Analog input Channel 1 (non-inverting, inverting)
13	DVSSCK	Clock circuitry ground
14	DVDDCK	Clock circuitry supply voltage, 1.8V
15	CKP	Clock input, non-inverting (Format: LVDS, LVPECL, CMOS/TTL, Sine Wave)
16	CKN	Clock input, inverting. For CMOS input on CKP, connect CKN to ground.
17, 64	DVSS	Digital circuitry ground
19	CK_EXT_EN	CK_EXT signal enabled when low (zero). Tristate when high.
20	DFRMT	Data format selection. 0: Offset Binary, 1: Two's Complement
21	PD_N	Full chip Power Down mode when Low. All digital outputs reset to zero. **After chip power up always apply Power Down mode before using Active Mode to reset chip.**
22	OE_N_1	Output Enable Channel 0. Tristate when high

24, 41, 58	OVDD	I/O ring post-driver supply voltage. Voltage range 1.7 to 3.6V
25, 40, 57	OVSS	Ground for I/O ring
26	D1_0	Output Data Channel 1 (LSB, 13 bit output or 1Vpp full scale range)
27	D1_1	Output Data Channel 1 (LSB, 12 bit output 2Vpp full scale range)
28	D1_2	Output Data Channel 1
29	D1_3	Output Data Channel 1
30	D1_4	Output Data Channel 1
31	D1_5	Output Data Channel 1
32	D1_6	Output Data Channel 1
33	D1_7	Output Data Channel 1
34	D1_8	Output Data Channel 1
35	D1_9	Output Data Channel 1
36	D1_10	Output Data Channel 1
37	D1_11	Output Data Channel 1 (MSB for 1Vpp full scale range, see Reference Voltages section)
38	D1_12	Output Data Channel 1 (MSB for 2Vpp full scale range)
39	ORNG_1	Out of Range flag Channel 1. High when input signal is out of range
42	CK_EXT	Output clock signal for data synchronization. CMOS levels
43	D0_0	Output Data Channel 0 (LSB, 13 bit output or 1Vpp full scale range)
44	D0_1	Output Data Channel 0 (LSB, 12 bit output 2Vpp full scale range)
45	D0_2	Output Data Channel 0
46	D0_3	Output Data Channel 0
47	D0_4	Output Data Channel 0
48	D0_5	Output Data Channel 0
49	D0_6	Output Data Channel 0
50	D0_7	Output Data Channel 0
51	D0_8	Output Data Channel 0
52	D0_9	Output Data Channel 0
53	D0_10	Output Data Channel 0
54	D0_11	Output Data Channel 0 (MSB for 1Vpp full scale range, see Reference Voltages section)
55	D0_12	Output Data Channel 0 (MSB for 2Vpp full scale range)
56	ORNG_0	Out of Range flag Channel 0. High when input signal is out of range
59	OE_N_0	Output Enable Channel 0. Tristate when high
60, 61	CM_EXTBC_1, CM_EXTBC_0	Bias control bits for the buffer driving pin CM_EXT 00: OFF 01: 50uA 10: 500uA 11: 1mA
62, 63	SLP_N_1, SLP_N_0	Sleep Mode 00: Sleep Mode 01: Channel 0 active 10: Channel 1 active 11: Both channels active

Recommended Usage

Analog Input

The analog inputs to the ASD0500 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The CM_EXT pin provides a voltage suitable as common mode voltage reference. The internal buffer for the CM_EXT voltage can be switched off, and driving capabilities can be changed by using the CM_EXTBC control input.

Figure 4 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22 ohm) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic

resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

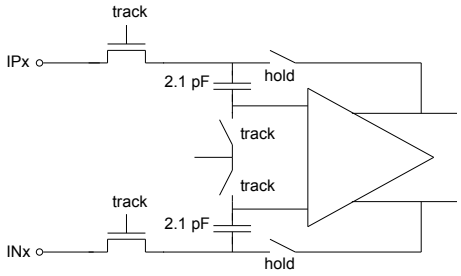

Figure 4: Input configuration

DC-coupling

Figure 5 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as reference to set the common mode voltage.

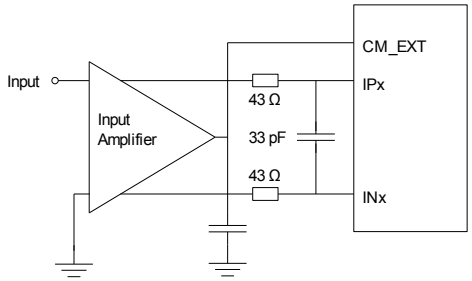

Figure 5: DC coupled input with buffer

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the ASD0500 input specifications.

Detailed configuration and usage instructions must be found in the documentation of the selected driver, and the values given in figure 5 must be varied according to the recommendations for the driver.

AC-coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 6 shows a recommended configuration using a transformer. Make

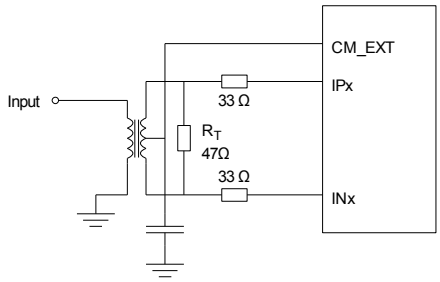

Figure 6: Transformer coupled input

sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to minimize phase mismatch between the differential ADC inputs for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout. If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in figure 8 can be used.

Figure 7 shows AC-coupling using capacitors. Resistors from the CM_EXT output, R_{CM}, should be used to bias the differential input signals to the correct voltage. The series capacitor, C_I, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

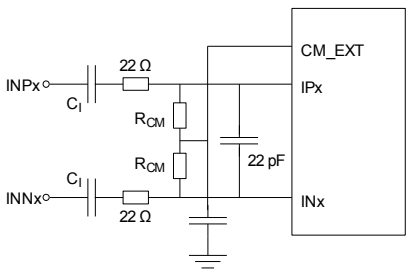

Figure 7: AC coupled input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of figure 8 can be used. The configuration in figure 8 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

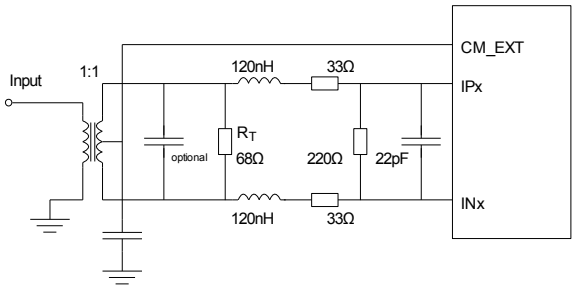

Figure 8: Alternative input network

Clock Input and Jitter considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the ASD0500 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% are acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally. Hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CKN pin should be connected to ground, and the CMOS clock signal should be connected to CKP. For differential sine wave clock, the input amplitude must be at least +/- 800 mVpp.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1,

$$SNR_{jitter} = 20 \cdot \log\left(2 \cdot \pi \cdot f_{IN} \cdot \epsilon_t\right) \qquad (1)$$

where f_{IN} is the signal frequency, and ε_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be re-timed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Digital Outputs

Digital output data are presented on parallel CMOS form. The voltage on the OVDD pin set the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OVDD above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CK_EXT always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE_N signal high.

The ASD0500 employs digital offset correction. This means that the output code will be 4096 with shorted inputs. However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of codes at the edges of the full scale range. With **no** offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for overrange and all zeros for underrange.

Note that the out of range flags (ORNG) will behave differently for 12 bit and 13 bit output. For 13 bit output ORNG will be set when digital output data are all ones or all zeros. For 12-bit output the ORNG flags will be set when all twelve bits are zeros or ones **and** when the thirteenth bit is equal to the rest of the bits.

Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connect to OVSS). Setting DFRMT high (connect to OVDD) results in 2's complement output format. Details are shown in table 3.

Table 3: Data Format Description for 2Vpp full scale range

Differential Input Voltage (IPx - INx)	**Output data: Dx_12 : Dx_0** (DFRMT = 0, offset binary)	**Output Data: Dx_12 : Dx_0** (DFRMT = 1, 2's complement)
1.0 V	1 1111 1111 1111	0 1111 1111 1111
+0.24mV	1 0000 0000 0000	0 0000 0000 0000
-0.24mV	0 1111 1111 1111	1 1111 1111 1111
-1.0V	0 0000 0000 0000	1 0000 0000 0000

The data outputs can be used in three different configurations.

- **Normal mode:**
  All 13 bits are used. MSB is Dx_12 and LSB is Dx_0. This mode gives optimum performance
- **12-bit mode:**
  The LSB is left unconnected such that only 12 bits are used. MSB is Dx_12 and LSB is Dx_1. This mode gives slightly reduced performance due to increased quantization noise.
- **Reduced full scale range mode:**
  The full scale range is reduced from 2Vpp to 1Vpp which is equivalent to 6dB gain in the ADC frontend. Note that data are only available in 2's complement format in this mode. MSB is Dx_11 and LSB is Dx_0. Note that the codes will wrap around when exceeding the full scale range, and that out of range bits should be used to clamp output data. See section Reference Voltages for details. This mode gives slightly reduced performance

Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

If a lower full scale range is required the 13-bit output word provides sufficient resolution to perform digital scaling with an equivalent impact on noise compared to adjusting the reference voltages.

A simple way to obtain 1.0Vpp input range with a 12-bit output word is shown in table 4. Note that only 2's complement output data are available in this mode and that out of range conditions must be determined based on a two bit output. The output code will wrap around when the code goes outside the full scale range. The out of range bits should be used to clamp the output data for overrange conditions.

Table 4: Data Format Description for 1Vpp full scale range

Differential Input Voltage (IPx - INx)	**Output data Dx_11:Dx_0** (DFRMT = 0) (2's complement)	**Out of Range** (Use logical AND function for &)	**Output Data Dx_11:Dx_0** (DFRMT = 1) (2's complement)	**Out of Range** (Use logical AND function for &)
> 0.5V	0111 1111 1111	Dx_12 = 1 & Dx_11 = 1	0111 1111 1111	D_12 = 0 & D_11 = 1
0.5V	0111 1111 1111		0111 1111 1111	
+0.24mV	0000 0000 0000		0000 0000 0000	
-0.24mV	1111 1111 1111		1111 1111 1111	
-0.5V	1000 0000 0000		1000 0000 0000	
< -0.5V	1000 0000 0000	Dx_12 = 0 & Dx_11 = 0	1000 0000 0000	Dx_12 = 1 & Dx_11 = 0

Operational Modes

The operational modes are controlled with the PD_N and SLP_N pins. If PD_N is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for other idle modes as all references need to settle to their final values before normal operation can resume.

The SLP_N bus can be used to power down each channel independently, or to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

Startup Initialization

The ASD0500 must be reset prior to normal operation. This is required every time the power supply voltage has been switched off. A reset is performed by applying Power Down mode. Wait until a stable supply voltage has been reached, and pull the PD_N pin for the duration of at least one clock cycle. The input clock must be running continuously during this Power Down period and until active operation is reached. Alternatively the PD pin can be kept low during power-up, and then be set high when the power supply voltage is stable.

The input clock should be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

Package Mechanical Data

TQFP64

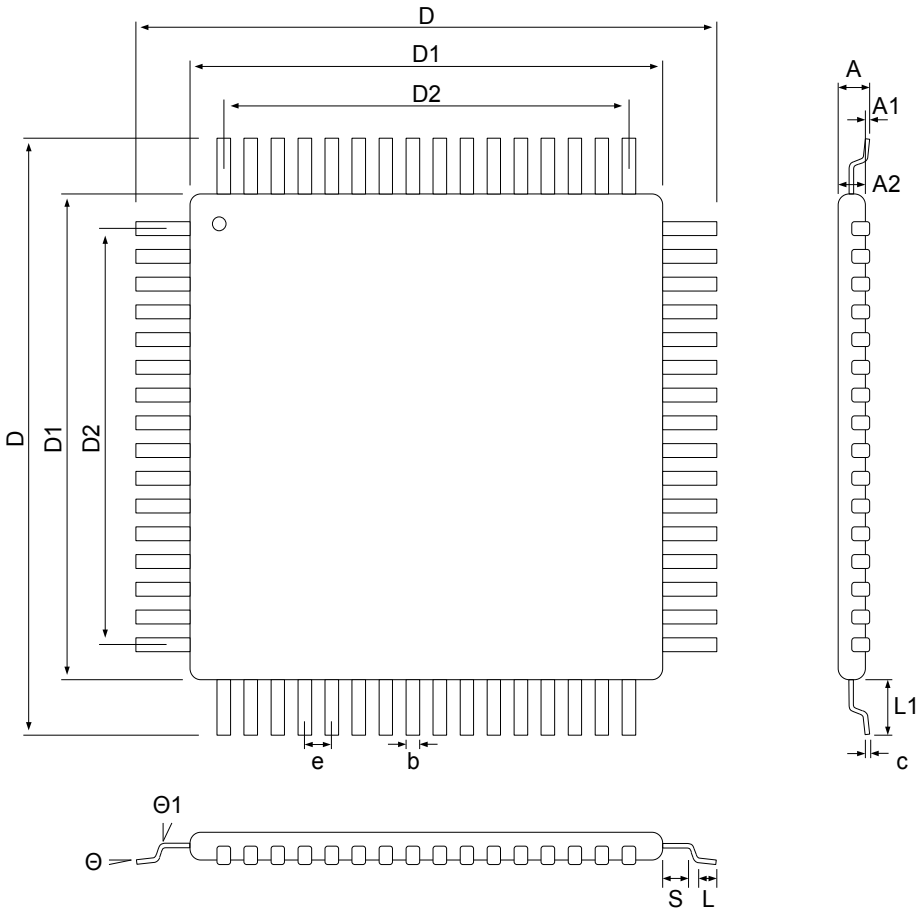

Figure 9: TQFP 64 Package dimensions (millimeter unless otherwise noted)

Table 5: TQFP 64 Dimensions

	Millimeter			Inch		
Symbol	Min	Typ	Max	Min	Typ	Max
A	-	-	1.2	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D		12.00 BSC			0.472 BSC	
D1		10.00 BSC			0.393 BSC	
D2		7.5 BSC			0.295 BSC	
Θ	0º	3.5º	7º	0º	3.5º	7º
Θ1	0º	-	-	0º	-	-
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
S	0.20	-	-	0.008	-	-
b	0.17	0.20	0.27	0.007	0.008	0011
e		0.5 BSC			0.020 BSC	

QFN64

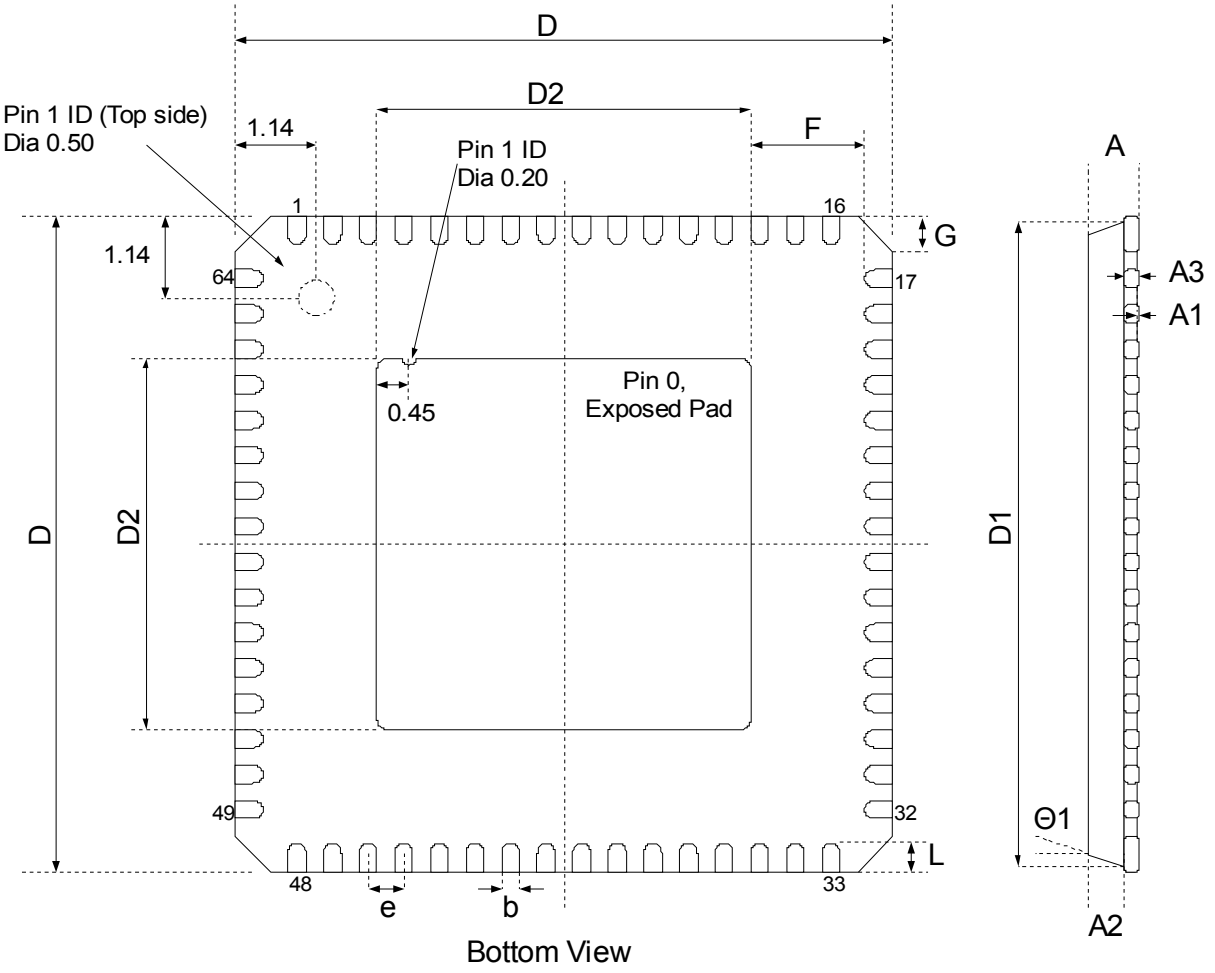

Figure 10: QFN 64 Package dimensions (millimeter unless otherwise noted)

Table 6: QFN 64 Dimensions

	Millimeter			Inch		
Symbol	Min	Typ	Max	Min	Typ	Max
A			0.9			0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2		0.65	0.7		0.026	0.028
A3		0.2 REF			0.008 REF	
b	0.2	0.25	0.3	0.008	0.010	0.012
D		9.00 bsc			0.354 bsc	
D1		8.75 bsc			0.344 bsc	
D2	3.79	3.99	4.19	0.149	0.157	0.165
L	0.3	0.4	0.5	0.012	0.016	0.020
e		0.50 bsc			0.020 bsc	
Θ1	0°		12°	0°		12°
F	1.9			0.075		
G	0.24	0.42	0.6	0.0096	0.0168	0.024

Product Information

Product	Status	Datasheet revision	Date
ASD0500	Product Specification	v3.2	2010.04.23

Ordering information

Ordering Code	Temp. range	Package type	Package drawing	MSL, Peak temp (1)	Transport Media
ASD0500L20-INR	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tape and Reel
ASD0500L40-INR	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tape and Reel
ASD0500L65-INR	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tape and Reel
ASD0500L85-INR	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tape and Reel
ASD0500L20-IPR	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tape and Reel
ASD0500L40-IPR	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tape and Reel
ASD0500L65-IPR	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tape and Reel
ASD0500L80-IPR	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tape and Reel
ASD0500L20-INT	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tray
ASD0500L40-INT	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tray
ASD0500L65-INT	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tray
ASD0500L85-INT	-40 to +85 °C	64 pin QFN	QFN64	Level 2A	Tray
ASD0500L20-IPT	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tray
ASD0500L40-IPT	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tray
ASD0500L65-IPT	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tray
ASD0500L80-IPT	-40 to +85 °C	64 pin TQFP	TQFP64	Level 3	Tray

(1) MSL, Peak Temp: The moisture sensitivity level rating classified according to the JEDEC industry standard and to peak solder temperature.

Datasheet status

Objective Product Specification:

The values and functionality describe design targets only. Specifications and functionality can be changed without notice

Preliminary Product Specification:

The specifications are based on initial design results. Specifications and functionality can be changed without notice.

Product Specification:

Information is current as of publication data. Products conform to specifications according to the terms of Arctic Silicon Devices AS standard warranty. Production does not necessarily require all parameters to be tested.

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