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SA2030

PCM FRAME ALIGNER

FEATURES

- Frame Alignment Recovery and loss in accordance with CCITT recommendations G.732 and G.737
- Jitter and phase-wander immunity exceed the requirements of CCITT recommendation G.823.
- Internal 1½ frame elastic buffer.
- Detection of incoming Alarm-Indication-Signal (AIS), and Distant Alarm
- Indication of Slip, loss of frame synchronisation, and loss of route clock conditions.
- ISO-CMOS technology, TTL Compatible.
- Pin-for-Pin replacement for Siemens PEB 2030 and SM 300
- Microprocessor Interface

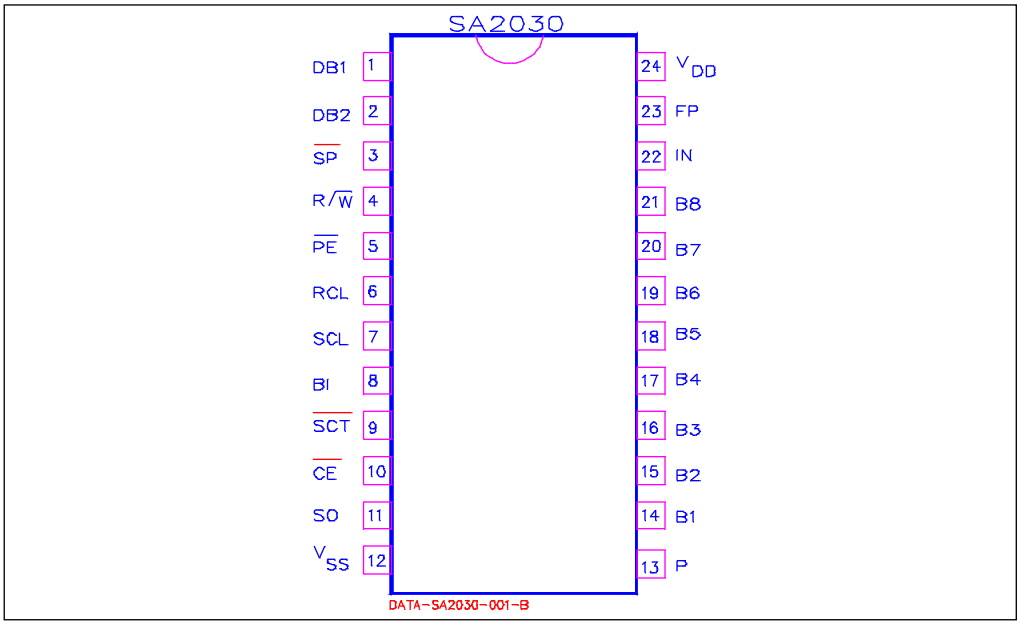
APPLICATIONS

- Delay compensation and clock alignment between 2,048MHz PCM-30 transmission lines, and terminating equipment.
- Control of Jitter and Wander within Digital Networks.
- Delay compensation between switching stages.
- Interfacing of PCM systems operating with different clocks.
- PCM concentrators and subscriber multiplexers.

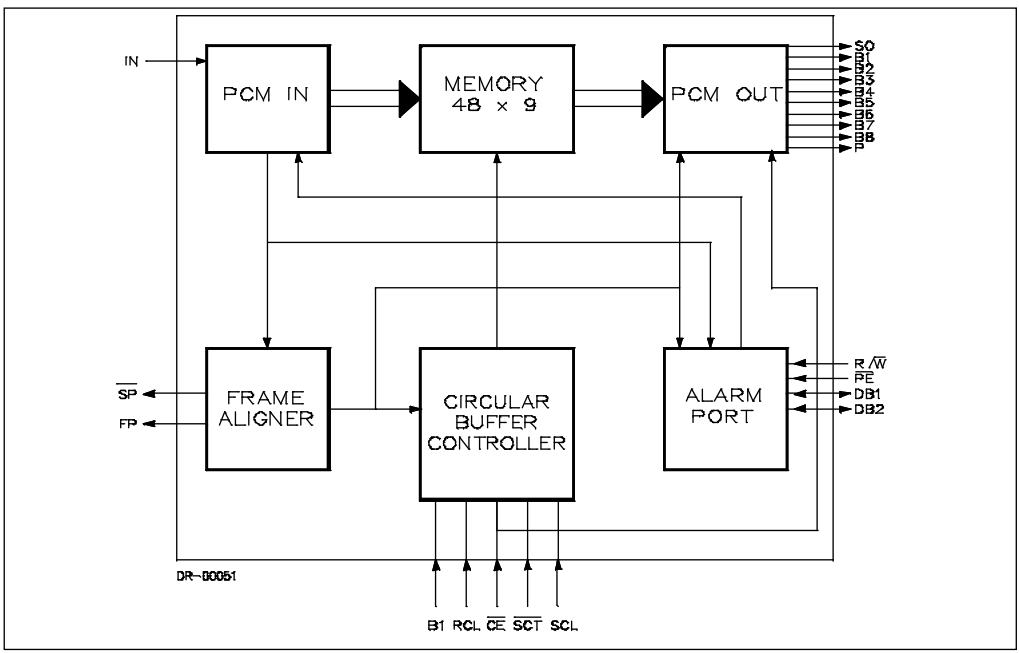
GENERAL DESCRIPTION

The SA2030 is designed to interface PCM-30 routes with switching systems. The device synchronises with the frame-format of the incoming data, and outputs this data in accordance with the bit and frame timing of the terminating equipment. The circuit is designed to tolerate delay, drift, wander and jitter of the incoming data and clock, and thus simplifies the design of data- and clock-recovery hardware. The internal 1½ frames elastic buffer provides for delay compensation and wander immunity. If the bounds of the buffer are exceeded, the SA2030 will either repeat or drop a frame. The circuit will accurately detect incoming Alarm-Indication-Signal (AIS) conditions, in accordance with CCITT recommendation G.737. Loss of frame alignment is indicated on both dedicated outputs and by outputting of AIS. The circuit includes a bidirectional alarm port for interrogation of alarm conditions.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PCM INPUT AND FRAME-ALIGNMENT

The SA2030 accepts route data on the IN input pin, on rising edges of the route clock RCL. The circuit synchronises with the frame format of the incoming data by identification of the Frame Alignment Signal (FAS) and the Service Word (SW) in time slot zero of the PCM frame. The algorithm used for recovery and loss of frame synchronisation is in accordance with CCITT recommendation G.737. After the circuit has gained synchronisation with the incoming PCM-30 data stream, it outputs a synchronisation pulse SP on alternate frames, during the bit interval prior to time-slot-zero of frames containing the FAS word. The circuit will output a fault pulse on the FP output every time errors are detected in the incoming FAS word. When the circuit is unable to synchronise with the incoming data format, the SA2030 will generate a fault pulse every alternate frame, and outgoing synchronisation pulses will be suppressed.

PCM OUTPUT

Data is clocked out on falling edges of the System Clock (SCL). PCM output is clocked out serially on the SO output, and is made available in parallel on a tristate bus with parity (B1-B8, P). The tristate outputs are enabled by asserting $\overline{CE}$. The SA2030 must be provided with a System Clock Trigger ($\overline{SCT}$) pulse to define the required output frame timing. The $\overline{SCT}$ pulse defines the bit interval immediately prior to the start of time-slot-zero, on every alternate frame. Acceptance of $\overline{SCT}$ pulses is only enabled when $\overline{CE}$ is asserted. The tristate parallel bus, with $\overline{CE}$ control, simplifies the use of the circuit in multiplex and switching applications.

ELASTIC BUFFER

Incoming PCM data is saved in dual-ported RAM. The RAM has capacity for 1½ frames of data. The SA2030 can thus accommodate any required frame delay between the incoming data timing, and the required output frame timing. When the bounds of the buffer are exceeded, whole frames are either dropped or repeated. The action of dropping or repeating a received frame is called slip. Depending on the frame-delay, the SA2030 can tolerate between ½ and 1½ frame of wander without requiring to alternately repeat and drop frames. The design of the elastic buffer controller provides for correct performance under severe clock-and-data-jitter conditions. The SA2030 exceeds the requirements of CCITT recommendation G.823, and can be used to control jitter and wander within digital networks. The 1½ frame buffer is enabled by setting BI = 0. If BI = 1, the buffer length is limited to only one frame. The frame delay through the frame-aligner is then constrained to be less than one frame. The buffer inhibit mode is useful for delay compensation within a switching system, where drift and wander do not occur.

ALARM SUBSYSTEM

The alarm system may be used by the host equipment to determine the operation status of the SA2030. The SA2030 provides a bidirectional alarm-port interface DB1 and DB2. The direction of the interface is controlled by the R/$\overline{W}$ line. Transfers to or from the interface are enabled by strobing the port-enable ($\overline{PE}$) input. The circuit includes two 2-bit alarm registers. The four flags in these registers are set when:

- Incoming Alarm-Indication-Signal is received (AIS)
- Loss of frame synchronisation occurs (SYLOSS)
- A distant alarm is received (DISAL)
- A frame slip occurs (SLIP)

* The algorithm used for detection of incoming AIS is in accordance with CCITT recommendation G.737. That is, AIS will be correctly detected, even in the presence of random errors, at a rate of 1 in 10^3.
* The loss of frame synchronisation flag is set if loss of frame-alignment occurs, if the route clock is missing or too slow, or if a system-clock-trigger ($\overline{SCT}$) pulse is not applied to the circuit once every alternate frame.
* The distant alarm flag is set if bit 3 of time-slot-zero of frames not containing FAS is true.
* The frame-slip is set if the frame aligner either drops or repeats a frame.

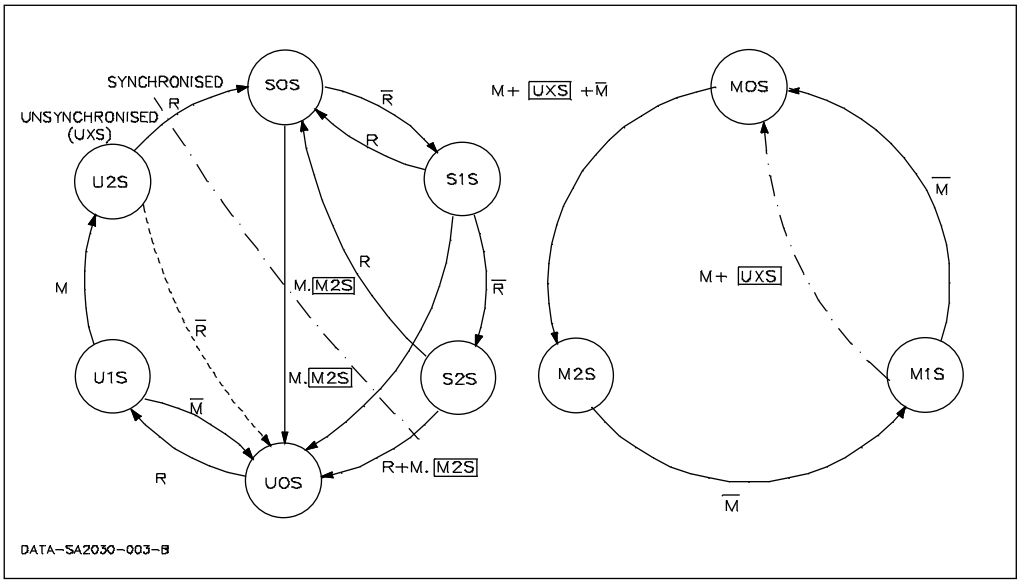
Selection of which of the two alarm registers is to be read, is carried out by first writing a command to the comand register via DB1 and DB2. Four commands are supported:

- Enable Read of Alarm Group 1
- Enable Read of Alarm Group 2
- Clear all alarm flags
- Simulate Alarms

Alarm Group 1 includes the AIS and frame synchronisation flags. Alarm Group 2 includes the Slip and distant alarm flags.

Once an alarm flag is set, it can only be cleared by writing the "clear-all-alarms" command to the alarm command register. That is, these flags remain set until explicitly cleared. The simulate-alarm command provides an alarm system self-test capability. This command simulates all alarm conditions at their sources. If the circuit is operating correctly, all alarm flags should be set after issuing this command. Alarm simulation tests the loss of synchronisation function of the frame alignment state-machine, and the AIS detection logic, and thus may require up to four-frames to complete. After all of the alarm flags are set, alarm simulation is disabled, and the circuit reverts to normal operation.

LOSS AND RECOVERY OF FRAME ALIGNMENT



CONDITIONS

R	-	Good FAS Received
$\overline{R}$	-	One or more errors in FAS
M	-	Bit 2 of service word = 1 (Good SW)
$\overline{M}$	-	Bit 2 of service word = 0 (Bad SW)
UXS	-	Unsynchronised stated U0S, U1S or U2S
M2S	-	Two service word errors received state

STATES

U0S	-	Unsynchronised, zero frames OK state
U1S	-	Unsynchronised, one frame OK state
U2S	-	Unsynchronised, two frame OK state
S0S	-	Synchronised, zero FAS errors state
S1S	-	Synchronised, one FAS error state
S2S	-	Synchronised, two FAS errors state
M0S	-	Zero service word errors state
M1S	-	One service word error state
M2S	-	Two service word errors state

Command Mnemonic	Write		Alarms Read		Description
	DB2	DB1	DB2	DB1	
RAG1	0	0	AIS	SYLOSS	Read Alarm Group 1
RAG2	0	1	SLIP	DISAL	Read Alarm Group 2
CLR	1	0	-	-	Alarm Register Clear
SIM	1	1	-	-	Simulate Alarms

Notes: 1. After the CLR or SIM commands, neither RAG1 or RAG2 are selected for reading. Thus subsequent reading will return undefined data.
2. Allow 4 frames for the SIM command to execute before issuing a RAG1 or RAG2 command.

PIN DESCRIPTION

Pin No.	Name	Function
1	DB1	Bidirectional Alarm Port
2	DB2	Bidirectional Alarm Port
3	SP	Synchronisation Pulse output. Asserted during the bit interval immediately prior to time-slot-zero of frames that contain FAS. Suppressed in the event of frame-alignment loss.
4	R/$\overline{W}$	Input for controlling direction of Alarm port data bus DB1 and DB2. Internally pulled up to V_{DD}.
5	$\overline{PE}$	Alarm port enable. Asserting this pin enables data transfers to or from DB1 and DB2. Internally pulled up to V_{DD}.
6	RCL	Route Clock Input. 2.048 MHz clock that defines PCM input data timing. The route clock is usually extracted from the route data.
7	SCL	System Clock Input. 2.048 MHz clock that defines the timing of the terminating equipment.
8	BI	Buffer Inhibit Input. When true, the 1½ frame buffer is inhibited, and the output frame timing is constrained to be within one-frame of the input frame timing. When false, the full 1½ frame buffer is enabled, and immunity to wander is maximised. Buffer Inhibit Mode of operation is intended for delay compensation between switching stages in one exhange system. Internally pulled up to V_{DD}.
9	$\overline{SCT}$	Station Clock Trigger input. Low going pulse used by the host system to define the required output frame timing. $\overline{SCT}$ should be asserted on alternate frames, during the data-bit interval immediately prior to time-slot-zero. $\overline{SCT}$ input is enabled by asserting $\overline{CE}$.
10	$\overline{CE}$	Chip Enable input. When asserted the parallel outputs, B1 to B8 and P are enabled. When CE = 1, parallel outputs are high impedance. CE must also be asserted to enable the SCT input. Internally pulled-up to V_{DD}.
11	SO	Serial PCM Data Output. PCM-30 format output of aligned and retimed data. Data clocked out under control of the System Clock SCL.
12	V_{SS}	Ground (0V) supply.
13	P	Parity Bit 3-state Ouput. Parity check for internal RAM. RAM data is saved with Parity bit. Even Parity is used.
14	B1	3-State PCM Parallel Output (PCM sign bit).
15	B2	3-State PCM Parallel Output
16	B3	3-State PCM Parallel Output
17	B4	3-State PCM Parallel Output
18	B5	3-State PCM Parallel Output
19	B6	3-State PCM Parallel Output
20	B7	3-State PCM Parallel Output
21	B8	3-State PCM Parallel Output (LSB)
22	IN	PCM data input. Data is derived from route data and is clocked into the circuit on rising edges of RCL.
23	FP	Fault Pulse Output. Fault pulses of 4 Route Clock cycles duration are delivered whenever errors are detected in FAS, or on alternate frames in the event of Frame Alignment loss.
24	V_{DD}	Supply Voltage (+5V Nominal)

Absolute Maximum Ratings

Characteristics	Sym	Min	Max	Unit	Conditions
Supply Voltage	V_{DD}	-0,3	7,0	V	-
Voltage on any pin	V_{PIN}	V_{SS} -0,3	V_{DD} +0,3	V	-
Storage Temperature	T_{STG}	-55	125	°C	-
Total power dissipation	P_{TOT}	-	100	mW	25°C
Operating ambient temperature range	T_{OP}	0	70	°C	-

Stresses beyond these limits may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DD}	4,75	5,00	5,25	V	-
Voltage on any pin	V_{PIN}	V_{SS}	-	V_{DD}	V	-
Operating temperature	T_{OP}	0	25	70	°C	-

Electrical Characteristics

T_{AMB} = 25°C, over recommended operating supply voltage range.

Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Standby Power Consumption	P_{STBY}	-	-	1,0	mW	Outputs, Unloaded, V_{DD} = 5V
Power Consumption	P_{OPER}	-	25,0	-	mW	Outputs Unloaded, at 2,048MHz, V_{DD} = 5V
Input High Voltage	V_{IH}	2,4	-		V	
Input Low Voltage	V_{IL}	-	-	0,8	V	
Input Pull-up Current	I_{PU}	-150		-5	µA	V_{IN} = 0V
Output High Voltage	V_{OH}	2,7	-	-	V	I_{OH} = -1,0mA
Output Low Voltage	V_{OL}	-	-	0,4	V	I_{OL} = 1,0mA
High Impedance Leakage Current	I_{OZ}	-	50	-	nA	

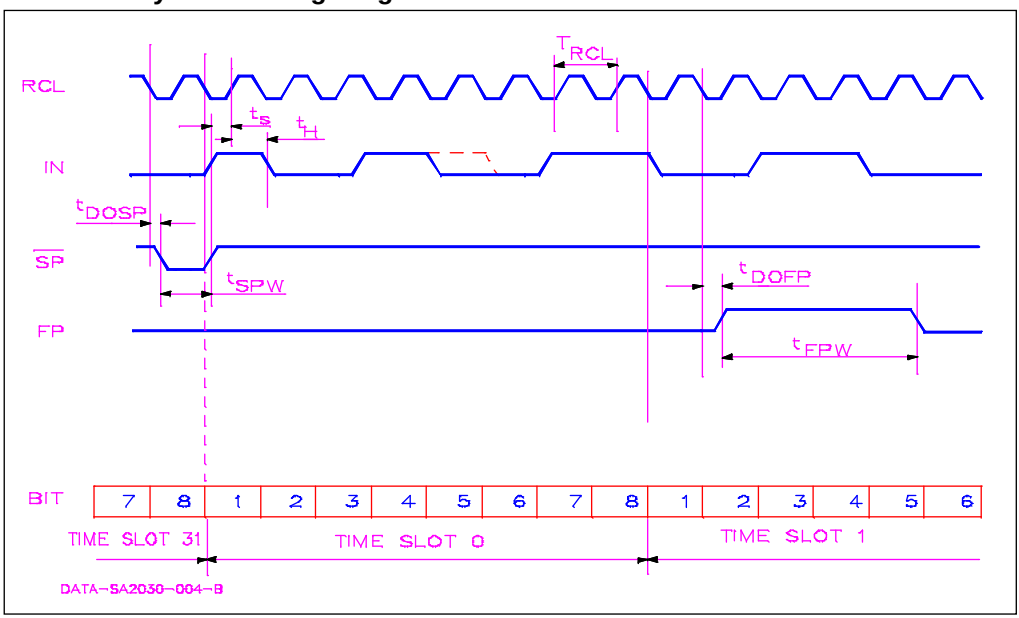
Route Subsystem Timing

(At V_{DD} = 5V, T_{AMB} = 25°C)

Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Route Clock Period	T_{RCL}	400	488	600	ns	Note 1, 2, 3
Route Clock Duty Cycle	D_{RCL}	25	50	75	%	at 2,048MHz
Input Data Setup time	t_S	150	-	-	ns	
Input Data Hold time	t_H	40	-	-	ns	
Synch Pulse Width	t_{SPW}	-	488	-	ns	In Frame Synch
Synch Pulse Delay	t_{DOSP}	-	-	200	ns	In Frame Synch
Fault Pulse Width	t_{FPW}	-	1952	-	ns	After Bad FAS
Fault Pulse Delay	t_{DOFP}	-	-	200	ns	After Bad FAS
Synch Pulse Repeat Period	T_{SP}	-	250	-	µs	In Frame Synch
Fault Pulse Repeat Period	T_{FP}	-	250	-	µs	Out of Frame Synch

Note: 1. The CCITT recommends clock frequency of 2,048MHz ±50ppm.
2. Incorrect Slip operation may occur if the Route clock and System clock differ by more than 1% (10000ppm).
3. A Synch Alarm will be issued if the Route Clock frequency is less than 75% of the Station Clock frequency.

Route Subsystem Timing Diagram



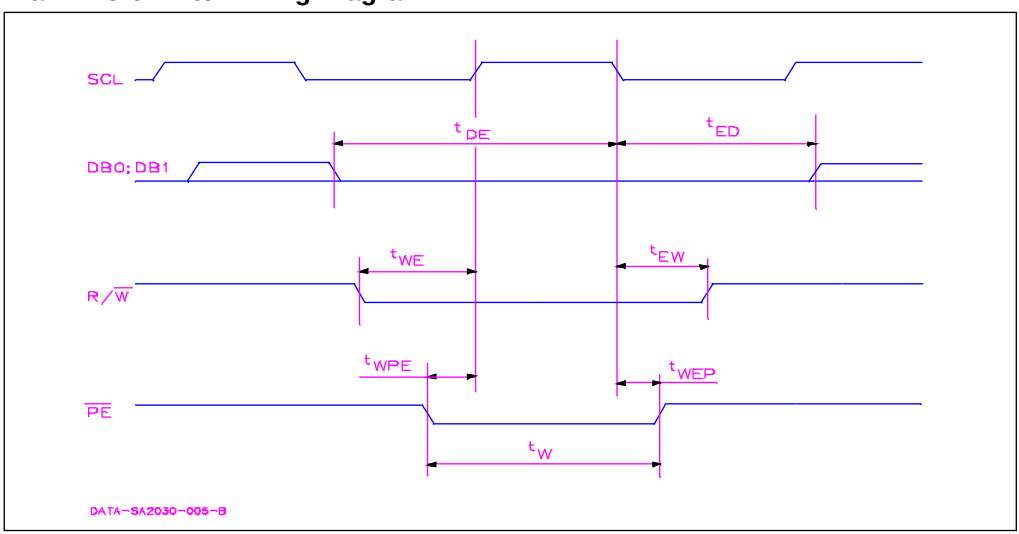
Alarm Port Read / Write Timing

(At V_{DD} = 5V, T_{AMB} = 25°C)

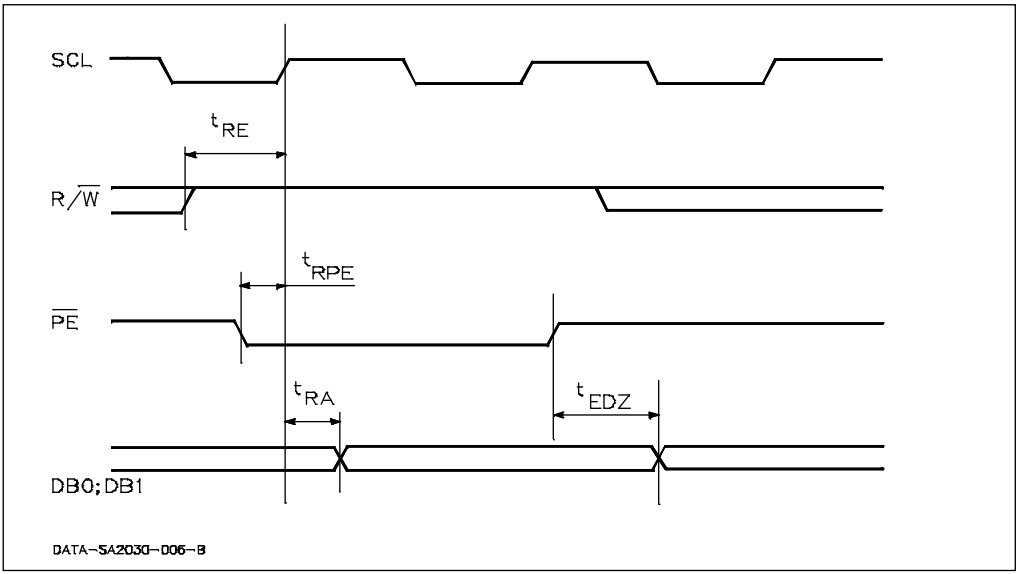
Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Data Setup Time	t_{DE}	100	-	-	ns	
Write Enable Setup Time	t_{WE}	150	-	-	ns	
Port Enable Write Setup Time	t_{WPE}	150	-	-	ns	
Data Hold Time	t_{ED}	100	-	-	ns	
Write Enable Hold Time	t_{EW}	100	-	-	ns	
Port Enable Hold Time	t_{WEP}	100	-	-	ns	
Write Duration	t_{N}	444	896	-	ns	at 2,048MHz
Read Enable Setup Time	t_{RE}	150	-	-	ns	
Port Enable Read Setup Time	t_{RPE}	150	-	-	ns	
Read Access Time	t_{RA}	-	-	350	ns	C_L=50pF, R_L=5K
High Impedance Delay	t_{EDZ}	-	-	160	ns	

Note: 1. R/$\overline{W}$ and $\overline{PE}$ are read on rising edges of SCL.
2. Data is latched on failing edges of SCL subject to R/$\overline{W}$ = 0, and $\overline{PE}$ = 0 on previous SCL rising edge.
3. Data is output after rising edge of SCL subject to R/$\overline{W}$ = 1 and $\overline{PE}$ = 0.

Alarm Port Write Timing Diagram



Alarm Port Read Timing Diagram

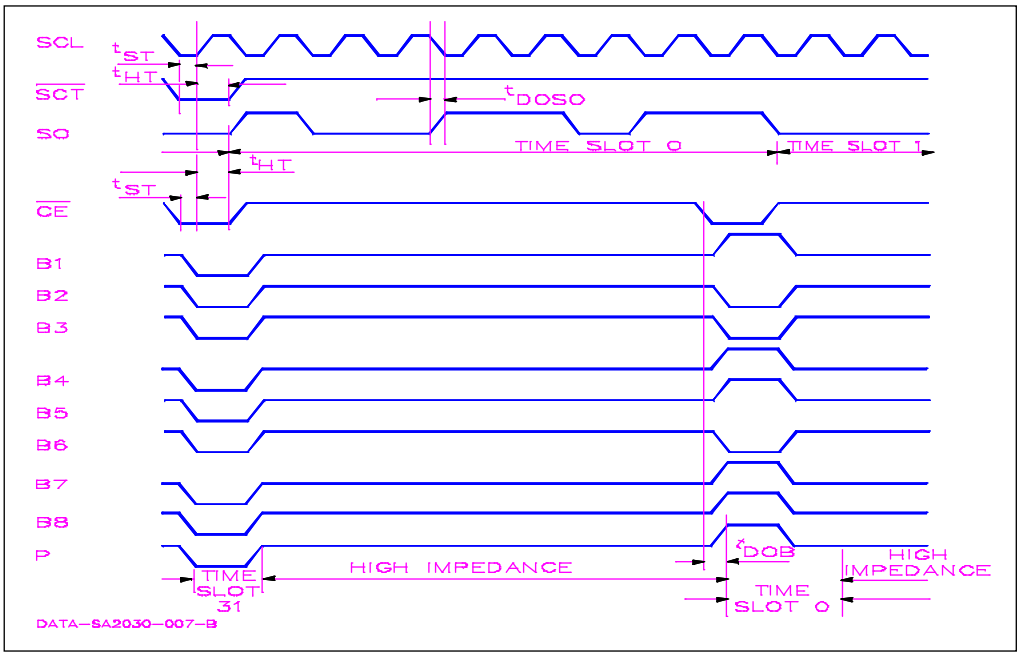


Data Output Timing

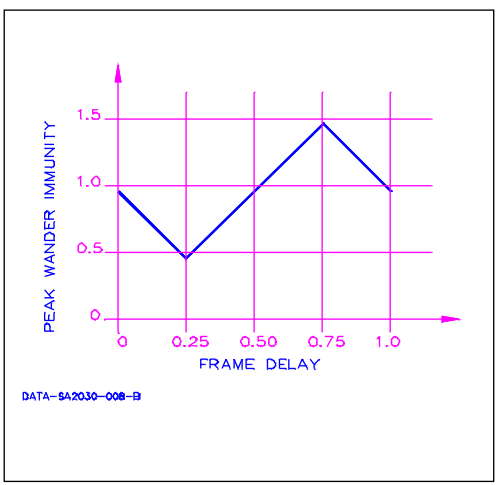
(at VDD = 5V, T_{AMB} = 25°C)

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
System Clock Period	t_{SCL}	400	488	600	ns	Note 1
System Clock Duty Cycle	D_{SCL}	25	50	75	%	
Clock Trigger Setup Time	t_{ST}	150	-	-	ns	
Clock Trigger Hold Time	t_{HT}	100	-	-	ns	
SO Output Delay	t_{DOSO}	-	-	200	ns	C_L=15pF, R_L=10K
BI.. B8, P Output Delay	t_{DOB}	-	-	200	ns	C_L=15pF, R_L=10K

Note: 1. The CCITT recommends a data rate of 2,048MHz + 50ppm.



JITTER IMMUNITY



FRAME DELAY