Process FIT Rate Report

QTR: 2013-00285 **Rev: 05**

Wafer Process: PHEMT-J

HMC190B	HMC348A	HMC784A
HMC194A	HMC349A	HMC792A
HMC197B	HMC424A	HMC849A
HMC199A	HMC425A	HMC939A
HMC221B	HMC427A	HMC941A
HMC231A	HMC435A	HMC1018A
HMC232A	HMC468A	HMC1019A
HMC233A	HMC470A	HMC1084
HMC234A	HMC472A	HMC-C011A
HMC240B	HMC539A	HMC-C018A
HMC241A	HMC540A	HMC-C019A
HMC244A	HMC542B	HMC-C025A
HMC245A	HMC544A	
HMC252A	HMC545A	
HMC253A	HMC547A	
HMC270A	HMC550A	
HMC271B	HMC574A	
HMC273A	HMC595A	
HMC274A	HMC603A	
HMC284A	HMC624A	
HMC305B	HMC625A	
HMC306A	HMC626A	
HMC321A	HMC627A	
HMC322A	HMC641A	
HMC344A	HMC681A	
HMC345A	HMC742A	
HMC347A	HMC743A	

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- *Supplying products of the highest quality*
- *Advance in state-of-the-art technology that supports our products*
- *Enhance our competitive position with superior product standards*

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- *Take the initiative to ensure product quality*
- *Create an environment where the highest standards are maintained*
- *Continue to improve quality practices*

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Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the PHEMT-J process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.hittite.com.

Glossary of Terms & Definitions:

1. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
2. **HTSL:** High Temperature Storage Life. Devices are subjected to 1000 hours at 150°C per JESD22-A103.
3. **MSL:** Moisture sensitivity level pre-conditioning is performed per JESD22-A113.
4. **Operating Junction Temp (T_{oj}):** Temperature of the die active circuitry during typical operation.
5. **Stress Junction Temp (T_{sj}):** Temperature of the die active circuitry during stress testing.
6. **UHAST:** Unbiased Highly Accelerated Stress Test. Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (18.6 PSIG). This test is performed in accordance with JESD22-A118.
7. **Temperature Cycle:** Devices are subjected to 500 cycles of -65°C to 150°C. This test is performed in accordance with JESD22-A104.
8. **THB:** Temperature Humidity Bias. Devices are subjected to 1000 hours of 85% relative humidity at a temperature of 85°C and electrical bias. This test is performed in accordance with JESD22-A101.

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Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:

HMC6488A / HMC349A (QTR2012-00017)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	80	80	Complete	
HTOL, 1000 hours	80	80	Complete	
Post HTOL Electrical Test	80	80	Pass	
HTSL, 1000 hours	46	46	Complete	
Post HTSL Electrical Test	46	46	Pass	

HMC6484 / HMC273A (QTR2012-00042)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	80	80	Complete	
HTOL, 1000 hours	80	80	Complete	
Post HTOL Electrical Test	80	80	Pass	
HTSL, 1000 hours	80	80	Complete	
Post HTSL Electrical Test	80	80	Pass	

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HMC284A (QTR2012-00461)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	478	478	Complete	
HTOL, 1000 hours	160	160	Complete	
Post HTOL Electrical Test	160	160	Pass	
HTSL, 1000 hours	80	80	Complete	
Post HTSL Electrical Test	80	80	Pass	
MSL1 Preconditioning	238	238	Complete	
MSL1 Preconditioning Final Test	238	238	Pass	
UHAST (Preconditioned)	80	80	Complete	
UHAST Final Test	80	80	Pass	
Temperature Cycle (Preconditioned)	80	80	Complete	
Temperature Cycle Final Test	80	80	Pass	
THB (Preconditioned)	78	78	Complete	
THB Final Test	78	78	Pass	

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HMC472A (QTR2013-00524)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	1134	1134	Complete	
HTOL, 168 hours	1134	1134	Complete	
Post HTOL Electrical Test	1134	1134	Pass	

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PHEMT-J Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With Device Die Junction Temp, T_j = 85°C

HMC6488A / HMC349A (QTR2012-00017)
Operating Junction Temp (T_{oj}) = 85°C(358°K)
Stress Junction Temp (T_{sj}) = 125°C(398°K)

HMC6484 / 273A (QTR2012-00042)
Operating Junction Temp (T_{oj}) = 85°C(358°K)
Stress Junction Temp (T_{sj}) = 125°C(398°K)

HMC284A (QTR2012-00461)
Operating Junction Temp (T_{oj}) = 85°C(358°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

HMC472A (QTR2013-00524)
Operating Junction Temp (T_{oj}) = 85°C(358°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

Device hours:

HMC6488A / HMC349A (QTR2012-00017) = (80 X 1000hrs) = 80,000 hours
HMC6484 / HMC273A (QTR2012-00042) = (80 X 1000hrs) = 80,000 hours
HMC284A (QTR2012-00461) = (160 X 1000hrs) = 160,000 hours
HMC472A (QTR2013-00524) = (1134 X 168hrs) = 190,512 hours

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For PHEMT-J MMIC, Activation Energy = 1.46 eV

Acceleration Factor (AF): $$AF = \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

HMC6488A / HMC349A (QTR2012-00017) Acceleration Factor = exp[1.46/8.6 e-5(1/358-1/398)] = 117.4
HMC6484 / 273A (QTR2012-00042) Acceleration Factor = exp[1.46/8.6 e-5(1/358-1/398)] = 117.4
HMC284A (QTR2012-00461) Acceleration Factor = exp[1.46/8.6 e-5(1/358-1/423)] = 1461.1
HMC472A (QTR2013-00524) Acceleration Factor = exp[1.46/8.6 e-5(1/358-1/423)] = 1461.1

Equivalent hours = Device hours x Acceleration Factor

Equivalent hours = (80,000x117.4)+(80,000x117.4)+(160,000x1461.1)+(190,512x1461.1) = 5.31×10^8 hours

Since there was no failures and we used a time terminated test, F=0, and R = 2F+2 = 2

The failure rate was calculated using Chi Square Statistic:

$\lambda_{CL} = \frac{\chi^2_{\%CL,2f+2} \cdot 10^9}{2 \cdot t \cdot ss \cdot AF}$ at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 85°C device junction temp;

Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X \quad 5.31x10^8 \quad)] = 1.8/ \quad 1.06x10^9 = \quad 1.72x10^{-9}$ failures/hour or 1.7 FIT or MTTF = $5.8x10^8$ Hours

$\lambda_{90} = [(\chi^2)_{90,2}]/(2X \quad 5.31x10^8 \quad)] = 4.6/ \quad 1.06x10^9 = \quad 4.34x10^{-9}$ failures/hour or 4.3 FIT or MTTF = $2.3x10^8$ Hours

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