ADVANCED
LINEAR
DEVICES, INC.

ALD114813/ALD114913

QUAD/DUAL N-CHANNEL DEPLETION MODE EPAD® PRECISION MATCHED PAIR MOSFET ARRAY

$V_{GS(th)}$= -1.30V

GENERAL DESCRIPTION

ALD114813/ALD114913 are high precision monolithic quad/dual depletion mode N-Channel MOSFETS matched at the factory using ALD's proven EPAD CMOS technology. These devices are intended for low voltage, small signal applications. They are excellent functional replacements for normally-closed relay applications, as they are normally on (conducting) without any power applied, but could be turned off or modulated when system power supply is turned on. These MOSFETS have the unique characteristics of, when the gate is grounded, operating in the resistance mode for low drain voltage levels and in the current source mode for higher voltage levels and providing a constant drain current.

These MOSFETS are designed for exceptional device electrical characteristics matching. As these devices are on the same monolithic chip, they also exhibit excellent temperature tracking characteristics. They are versatile as design components for a broad range of analog applications, and they are basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications. Besides matched pair electrical characteristics, each individual MOSFET also exhibits well controlled parameters, enabling the user to depend on tight design limits. Even units from different batches and different date of manufacture have correspondingly well matched characteristics.

These depletion mode devices are built for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in single 1.5V to +/-5V systems where low input bias current, low input capacitance and fast switching speed are desired. These devices exhibit well controlled turn-off and sub-threshold charactersitics and therefore can be used in designs that depend on sub-threshold characteristics.

The ALD114813/ALD114913 are suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. A sample calculation of the DC current gain at a drain current of 3mA and gate input leakage current of 30pA = 100,000,000. It is recommended that the user, for most applications, connect the V+ pin to the most positive voltage and the V- and IC pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times.

FEATURES

- Depletion mode (normally ON)
- Precision Gate Threshold Voltages: -1.30V +/- 0.04V
- Nominal $R_{DS(ON)}$ @V_{GS}=0.0V of 1.3KΩ
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- Low input capacitance
- $V_{GS(th)}$ match (V_{OS}) — 20mV
- High input impedance — 10^{12}Ω typical
- Positive, zero, and negative $V_{GS(th)}$ temperature coefficient
- DC current gain >10^8
- Low input and output leakage currents

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range* 0°C to +70°C		0°C to +70°C	
16-Pin SOIC Package	16-Pin Plastic Dip Package	8-Pin SOIC Package	8-Pin Plastic Dip Package
ALD114813SCL	ALD114813PCL	ALD114913SAL	ALD114913PAL

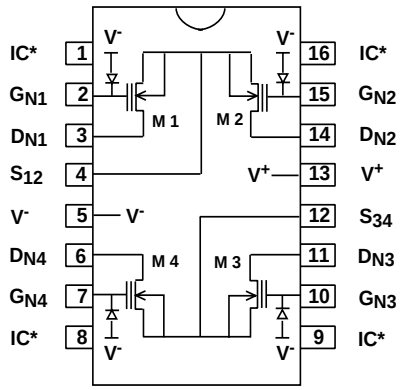
* Contact factory for industrial temp. range or user-specified threshold voltage values

APPLICATIONS

- Functional replacement of Form B (NC) relays
- Ultra low power (nanowatt) analog and digital circuits
- Ultra low operating voltage (<0.2V) analog and digital circuits
- Sub-threshold biased and operated circuits
- Zero power fail safe circuits in alarm systems
- Backup battery circuits
- Power failure and fail safe detector
- Source followers and high impedance buffers
- Precision current mirrors and current sources
- Capacitives probes and sensor interfaces
- Charge detectors and charge integrators
- Differential amplifier input stage
- High side switches
- Peak detectors and level shifters
- Sample and Hold
- Current multipliers
- Discrete analog switches and multiplexers
- Discrete voltage comparators

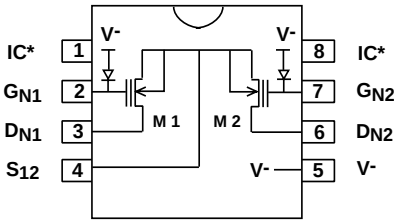
PIN CONFIGURATIONS

ALD114813



SCL, PCL PACKAGES

ALD114913



SAL, PAL PACKAGES

*IC pins are internally connected, connect to V-

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} ____ 10.6V
Gate-Source voltage, V_{GS} ____ 10.6V
Power dissipation ____ 500 mW
Operating temperature range SCL, PCL, SAL, PAL package ____ 0°C to +70°C
Storage temperature range ____ -65°C to +150°C
Lead temperature, 10 seconds ____ +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = -5V T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD114813/ALD114913 Min	Typ	Max	Unit	Test Conditions
Gate Threshold Voltage	$V_{GS(th)}$	-1.34	-1.30	-1.26	V	I_{DS} = 1μA, V_{DS} = 0.1V
Offset Voltage $V_{GS(th)1}$-$V_{GS(th)2}$	V_{OS}		7	20	mV	I_{DS} = 1μA
Offset VoltageTempco	TC_{VOS}		5		μV/ °C	V_{DS1} = V_{DS2}
GateThreshold Voltage Tempco	$TC_{VGS(th)}$		-1.7 0.0 +1.6		mV/ °C	I_D = 1μA, V_{DS} = 0.1V I_D = 20μA, V_{DS} = 0.1V I_D = 40μA, V_{DS} = 0.1V
On Drain Current	$I_{DS\ (ON)}$		12.0 3.0		mA	V_{GS} = +8.2V, V_{DS} = +5V V_{GS} = +2.7V, V_{DS} = +5V
Forward Transconductance	G_{FS}		1.4		mmho	V_{GS} = +2.7V V_{DS} = +7.7V
Transconductance Mismatch	ΔG_{FS}		1.8		%	
Output Conductance	G_{OS}		68		μmho	V_{GS} = +2.7V V_{DS} = +7.7V
Drain Source On Resistance	$R_{DS\ (ON)}$		500		Ω	V_{DS} = 0.1V V_{GS} = +2.7V
Drain Source On Resistance	$R_{DS\ (ON)}$		1.3		KΩ	V_{DS} = 0.1V V_{GS} = +0.0V
Drain Source On Resistance Tolerance	$\Delta R_{DS\ (ON)}$		7		%	
Drain Source On Resistance Mismatch	$\Delta R_{DS\ (ON)}$		0.5		%	
Drain Source Breakdown Voltage	BV_{DSX}	10			V	I_{DS} = 1.0μA V_{GS} = -2.3V
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} = -2.3V, V_{DS} =+5V T_A = 125°C
Gate Leakage Current[1]	I_{GSS}		3	200 1	pA nA	V_{DS} = 0V, V_{GS} = 5V T_A =125°C
Input Capacitance	C_{ISS}		2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1		pF	
Turn-on Delay Time	t_{on}		10		ns	V^+ = 5V, R_L= 5KΩ
Turn-off Delay Time	t_{off}		10		ns	V^+ = 5V, R_L= 5KΩ
Crosstalk			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents

PERFORMANCE CHARACTERISTICS OF EPAD® PRECISION MATCHED PAIR MOSFET FAMILY

ALD1108xx/ALD1109xx/ALD1148xx/ALD1149xx are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD® CMOS technology. These devices are intended for low voltage, small signal applications.

ALD's Electrically Programmable Analog Device (EPAD) technology provides the industry's only family of matched transistors with a range of precision threshold values. All members of this family are designed and actively programmed for exceptional matching of device electrical characteristics. Threshold values range from -3.50V Depletion to +3.50V Enhancement devices, including standard products specified at -3.50V, -1.30V, -0.40V, +0.00V, +0.20V, +0.40V, +0.80V, +1.40V, and +3.30V. ALD can also provide any customer desired value between -3.50V and +3.50V. For all these devices, even the depletion and zero threshold transistors, ALD EPAD technology enables the same well controlled turn-off, subthreshold, and low leakage characteristics as standard enhancement mode MOSFETs. With the design and active programming, even units from different batches and different date of manufacture have well matched characteristics. As these devices are on the same monolithic chip, they also exhibit excellent tempco tracking.

This EPAD MOSFET Array product family (EPAD MOSFET) is available in the three separate categories, each providing a distinctly different set of electrical specifications and characteristics. The first category is the ALD110800/ALD110900 Zero-Threshold™ mode EPAD MOSFETs. The second category is the ALD1108xx/ALD1109xx enhancement mode EPAD MOSFETs. The third category is the ALD1148xx/ALD1149xx depletion mode EPAD MOSFETs. (The suffix "xx" denotes threshold voltage in 0.1 V steps, for example, xx=08 denotes 0.80V).

The ALD110800/ALD110900 (quad/dual) are EPAD MOSFETs in which the individual threshold voltage of each MOSFET is fixed at zero. The threshold voltage is defined as I_{DS} = 1uA @ V_{DS} = 0.1V when the gate voltage V_{GS} = 0.00V. Zero threshold devices operate in the enhancement region when operated above threshold voltage and current level (V_{GS} > 0.00V and I_{DS} > 1uA) and subthreshold region when operated at or below threshold voltage and current level (V_{GS} <= 0.00V and I_{DS} < 1uA). This device, along with other very low threshold voltage members of the product family, constitute a class of EPAD MOSFETs that enable ultra low supply voltage operation and nanopower type of circuit designs, applicable in either analog or digital circuits.

The ALD1108xx/ALD1109xx (quad/dual) product family features precision matched enhancement mode EPAD MOSFET devices, which require a positive bias voltage to turn on. Precision threshold values such as +1.40V, +0.80V, +0.20V are offered. No conductive channel exists between the source and drain at zero applied gate voltage for these devices, except that the +0.20V version has a subthreshold current at about 20nA.

The ALD1148xx/ALD1149xx (quad/dual) features depletion mode EPAD MOSFETs, which are normally-on devices when the gate bias voltage is at zero volt. The depletion mode threshold voltage is at a negative voltage level at which the EPAD MOSFET turns off. Without a supply voltage and/or with V_{GS} = 0.0V the EPAD MOSFET device is already turned on and exhibits a defined and controlled on-resistance between the source and drain terminals.

The ALD1148xx/ALD1149xx depletion mode EPAD MOSFETs are different from most other types of depletion mode MOSFETs and certain types of JFETs in that they do not exhibit high gate leakage currents and channel/junction leakage currents. When negative signal voltages are applied to the gate terminal, the designer/user can depend on the EPAD MOSFET device to be controlled, modulated and turned off precisely. The device can be modulated and turned-off under the control of the gate voltage in the same manner as the enhancement mode EPAD MOSFET and the same device equations apply.

EPAD MOSFETs are ideal for minimum offset voltage and differential thermal response, and they are used for switching and amplifying applications in low voltage (1V to 10V or +/-0.5V to +/-5V) or ultra low voltage (less than 1V or +/- 0.5V) systems. They feature low input bias current (less than 30pA max.), ultra low power (microWatt) or Nanopower (power measured in nanoWatt) operation, low input capacitance and fast switching speed. These devices can be used where a combination of these characteristics are desired.

KEY APPLICATION ENVIRONMENT

EPAD(MOSFET Array products are for circuit applications in one or more of the following operating environments:

* Low voltage: 1V to 10V or +/- 0.5V to +/- 5V
* Ultra low voltage: less than 1V or +/- 0.5V
* Low power: voltage x current = power measured in microwatt
* Nanopower: voltage x current = power measured in nanowatt
* Precision matching and tracking of two or more MOSFETs

ELECTRICAL CHARACTERISTICS

The turn-on and turn-off electrical characteristics of the EPAD MOSFET products are shown in the Drain-Source On Current vs Drain-Source On Voltage and Drain-Source On Current vs Gate-Source Voltage graphs. Each graph show the Drain-Source On Current versus Drain-Source On Voltage characteristics as a function of Gate-Source voltage in a different operating region under different bias conditions. As the threshold voltage is tightly specified, the Drain-Source On Current at a given gate input voltage is better controlled and more predictable when compared to many other types of MOSFETs.

EPAD MOSFETs behave similarly to a standard MOSFET, therefore classic equations for a n-channel MOSFET applies to EPAD MOSFET as well. The Drain current in the linear region (V_{DS} < V_{GS} - $V_{GS(th)}$) is given by:

$$I_D = u \cdot C_{OX} \cdot W/L \cdot [V_{GS} - V_{GS(th)} - V_{DS}/2] \cdot V_{DS}$$

where:
u = Mobility
C_{OX} = Capacitance / unit area of Gate electrode
V_{GS} = Gate to Source voltage
$V_{GS(th)}$ = Turn-on threshold voltage
V_{DS} = Drain to Source voltage
W = Channel width
L = Channel length

In this region of operation the I_{DS} value is proportional to V_{DS} value and the device can be used as gate-voltage controlled resistor.

For higher values of V_{DS} where V_{DS} >= V_{GS} - $V_{GS(th)}$, the saturation current I_{DS} is now given by (approx.):

$$I_{DS} = u \cdot C_{OX} \cdot W/L \cdot [V_{GS} - V_{GS(th)}]^2$$

PERFORMANCE CHARACTERISTICS OF EPAD® PRECISION MATCHED PAIR MOSFET FAMILY (cont.)

SUB-THRESHOLD REGION OF OPERATION

Low voltage systems, namely those operating at 5V, 3.3V or less, typically require MOSFETs that have threshold voltage of 1V or less. The threshold, or turn-on, voltage of the MOSFET is a voltage below which the MOSFET conduction channel rapidly turns off. For analog designs, this threshold voltage directly affects the operating signal voltage range and the operating bias current levels.

At or below threshold voltage, an EPAD MOSFET exhibits a turn-off characteristic in an operating region called the subthreshold region. This is when the EPAD MOSFET conduction channel rapidly turns off as a function of decreasing applied gate voltage. The conduction channel induced by the gate voltage on the gate electrode decreases exponentially and causes the drain current to decrease exponentially. However, the conduction channel does not shut off abruptly with decreasing gate voltage, but decreases at a fixed rate of approximately 116mV per decade of drain current decrease. Thus if the threshold voltage is +0.20V, for example, the drain current is 1uA at V_{GS} = +0.20V. At V_{GS} = +0.09V, the drain current would decrease to 0.1uA. Extrapolating from this, the drain current is 0.01uA (10nA) at V_{GS} = -0.03V, 1nA at V_{GS} = -0.14V, and so forth. This subthreshold characteristic extends all the way down to current levels below 1nA and is limited by other currents such as junction leakage currents.

At a drain current to be declared “zero current” by the user, the Vgs voltage at that zero current can now be estimated. Note that using the above example, with $V_{GS(th)}$ = +0.20V, the drain current still hovers around 20nA when the gate is at zero volt, or ground.

LOW POWER AND NANOPOWER

When supply voltages decrease, the power consumption of a given load resistor decreases as the square of the supply voltage. So one of the benefits in reducing supply voltage is to reduce power consumption. While decreasing power supply voltages and power consumption go hand-in-hand with decreasing useful AC bandwidth and at the same time increases noise effects in the circuit, a circuit designer can make the necessary tradeoffs and adjustments in any given circuit design and bias the circuit accordingly.

With EPAD MOSFETs, a circuit that performs a specific function can be designed so that power consumption can be minimized. In some cases, these circuits operate in low power mode where the power consumed is measure in micro-watts. In other cases, power dissipation can be reduced to nano-watt region and still provide a useful and controlled circuit function operation.

ZERO TEMPERATURE COEFFICIENT (ZTC) OPERATION

For an EPAD MOSFET in this product family, there exist operating points where the various factors that cause the current to increase as a function of temperature balance out those that cause the current to decrease, thereby canceling each other, and resulting in net temperature coefficient of near zero. One of this temperature stable operating point is obtained by a ZTC voltage bias condition, which is 0.55V above a threshold voltage when V_{GS} = V_{DS}, resulting in a temperature stable current level of about 68uA. For other ZTC operating points, see ZTC characteristics.

PERFORMANCE CHARACTERISTICS

Performance characteristics of the EPAD MOSFET product family are shown in the following graphs. In general, the threshold voltage shift for each member of the product family causes other affected electrical characteristics to shift with an equivalent linear shift in $V_{GS(th)}$ bias voltage. This linear shift in V_{GS} causes the subthreshold I-V curves to shift linearly as well. Accordingly, the subthreshold operating current can be determined by calculating the gate voltage drop relative from its threshold voltage, $V_{GS(th)}$.

RDS(ON) AT VGS=GROUND

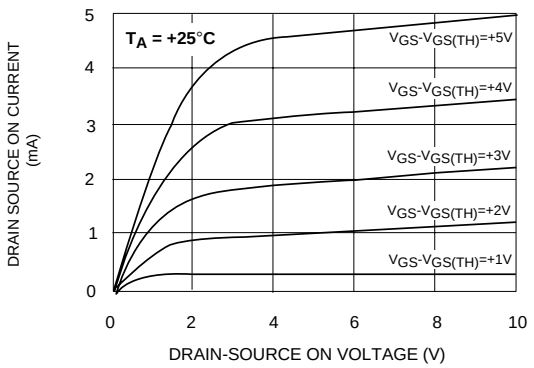
Several of the EPAD MOSFETs produce a fixed resistance when their gate is grounded. For ALD110800, the drain current at V_{DS} = 0.1V is at 1uA at V_{GS} = 0.0V. Thus just by grounding the gate of the ALD110800, a resistor with $R_{DS(ON)}$ = ~100KOhm is produced. When an ALD114804 gate is grounded, the drain current I_{DS} = 18.5 uA@ V_{DS} = 0.1V, producing $R_{DS(ON)}$ = 5.4KOhm. Similarly, ALD114813 and ALD114835 produces 77uA and 185uA, respectively, at V_{GS} = 0.0V, producing $R_{DS(ON)}$ values of 1.3KOhm and 540Ohm, respectively.

MATCHING CHARACTERISTICS

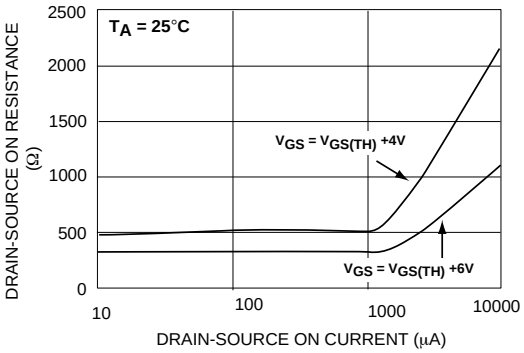
A key benefit of using matched-pair EPAD MOSFET is to maintain temperature tracking. In general, for EPAD MOSFET matched pair devices, one device of the matched pair has gate leakage currents, junction temperature effects, and drain current temperature coefficient as a function of bias voltage that cancel out similar effects of the other device, resulting in a temperature stable circuit. As mentioned earlier, this temperature stability can be further enhanced by biasing the matched-pairs at Zero Tempco (ZTC) point, even though that could require special circuit configuration and power consumption design consideration.

TYPICAL PERFORMANCE CHARACTERISTICS

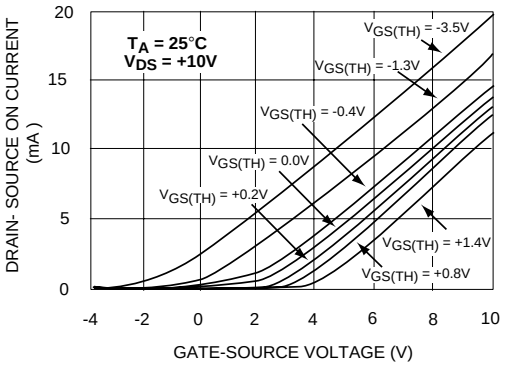
OUTPUT CHARACTERISTICS



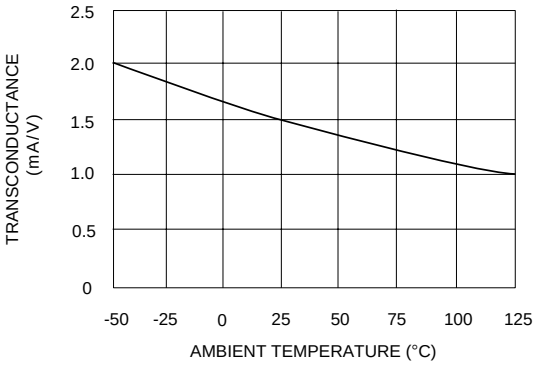
DRAIN-SOURCE ON RESISTANCE vs. DRAIN-SOURCE ON CURRENT



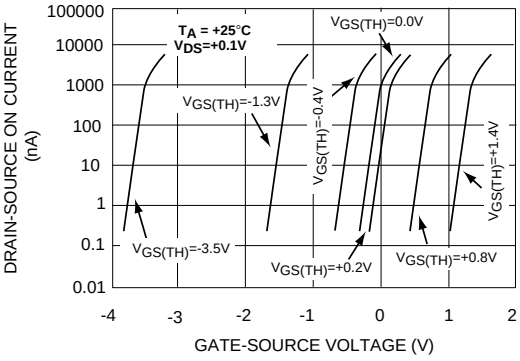
FORWARD TRANSFER CHARACTERISTICS



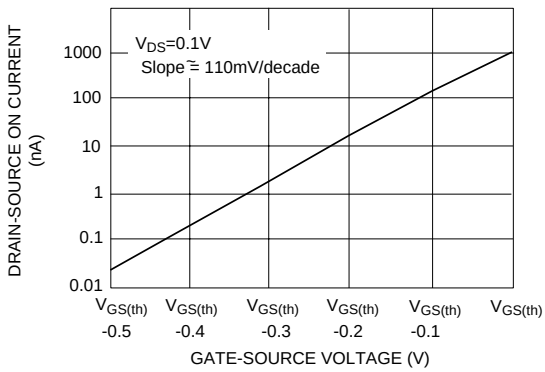
TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE



SUBTHRESHOLD FORWARD TRANSFER CHARACTERISTICS

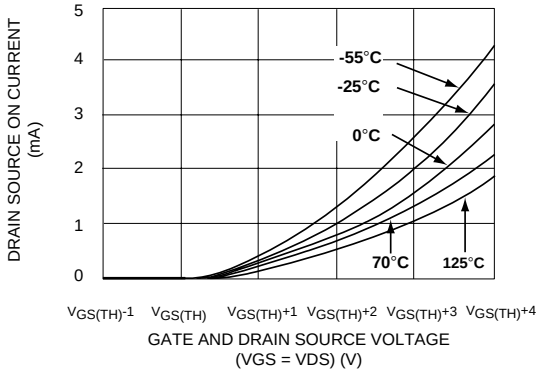


SUBTHRESHOLD FORWARD TRANSFER CHARACTERISTICS

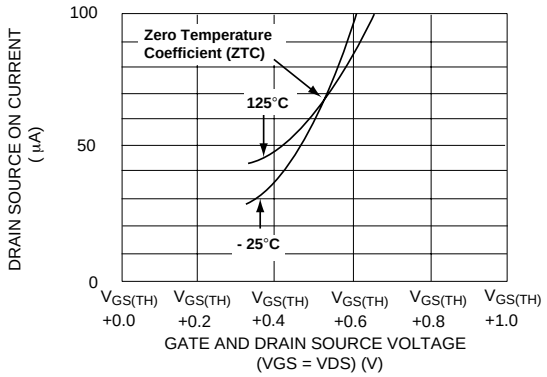


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

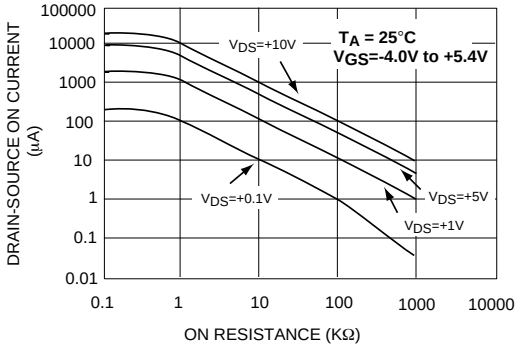
DRAIN SOURCE ON CURRENT, BIAS CURRENT vs. AMBIENT TEMPERATURE



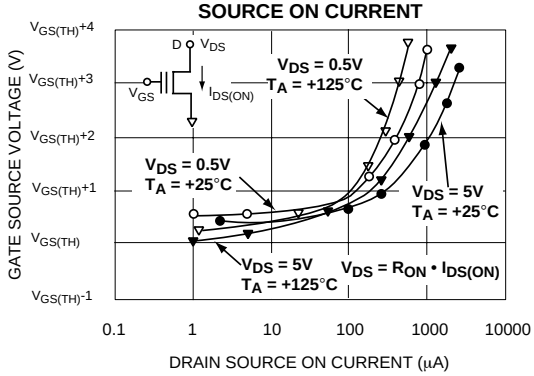
DRAIN SOURCE ON CURRENT, BIAS CURRENT vs. AMBIENT TEMPERATURE



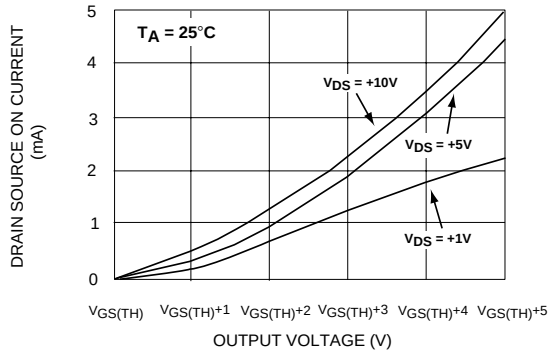
DRAIN-SOURCE ON CURRENT vs. ON RESISTANCE



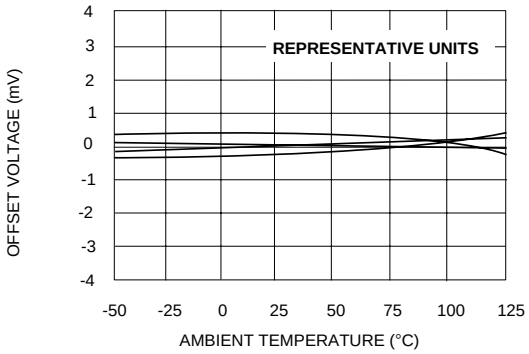
GATE SOURCE VOLTAGE vs. DRAIN SOURCE ON CURRENT



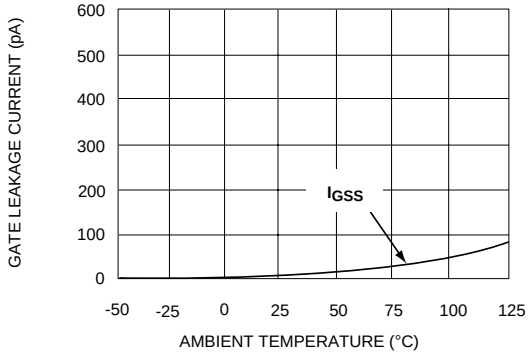
DRAIN SOURCE ON CURRENT vs. OUTPUT VOLTAGE



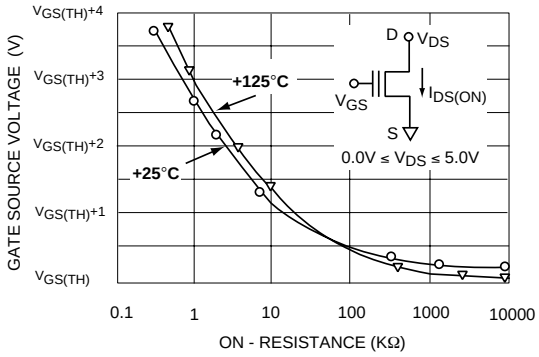
OFFSET VOLTAGE vs. AMBIENT TEMPERATURE



GATE LEAKAGE CURRENT vs. AMBIENT TEMPERATURE

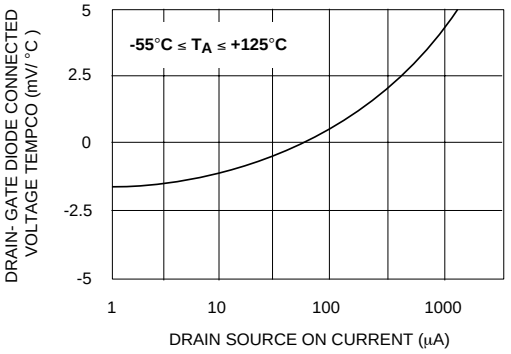


GATE SOURCE VOLTAGE vs. ON - RESISTANCE

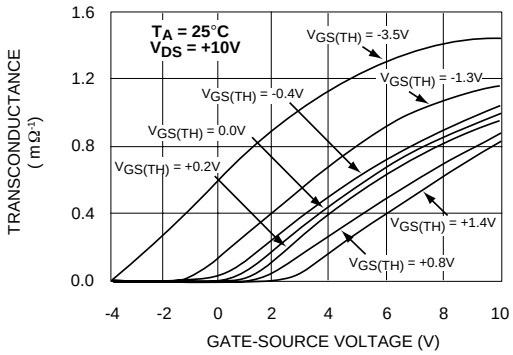


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

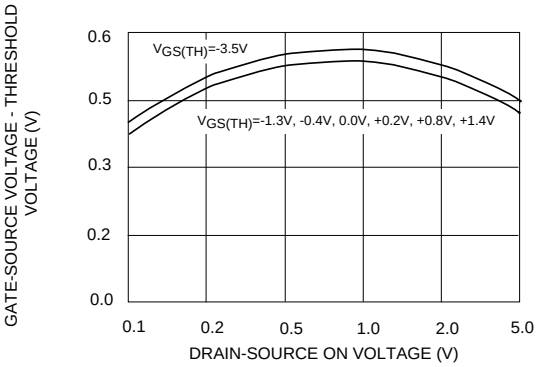
DRAIN - GATE DIODE CONNECTED VOLTAGE TEMPCO vs. DRAIN SOURCE ON CURRENT



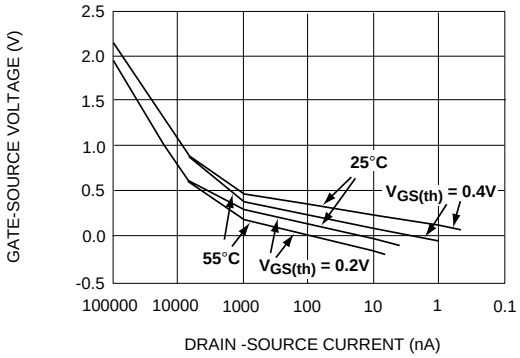
TRANSFER CHARACTERISTICS



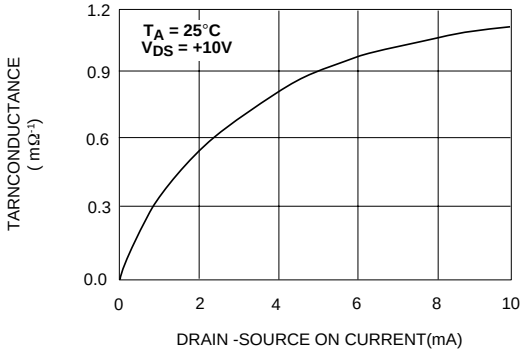
ZERO TEMPERETURE COEFFICIENT CHARACTERISTIC



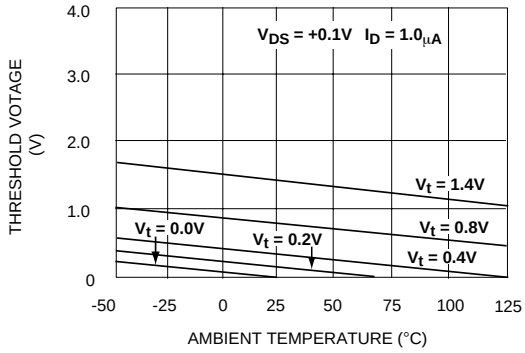
SUBTHRESHOLD CHARACTERISTICS



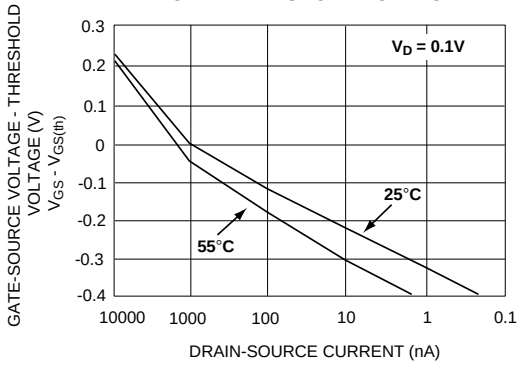
TRANCONDUCTANCE vs. DRAIN-SOURCE ON CURRENT



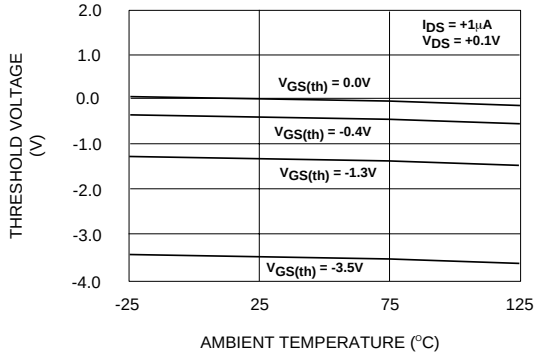
THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE



NORMALIZED SUBTHRESHOLD CHARACTERISTICS RELATIVE GATE THRESHOLD VOLTAGE

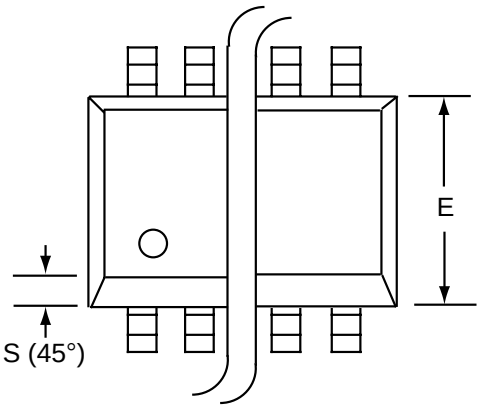


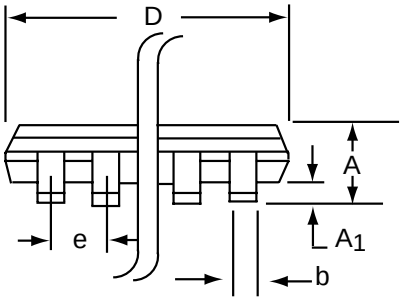
THRESHOLD VOLTAGES vs. AMBIENT TEMPERATURES



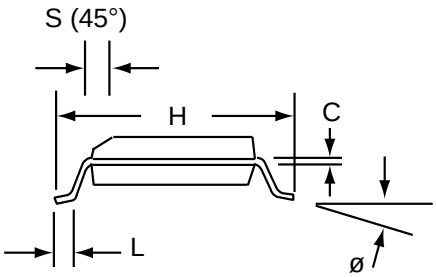
SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package



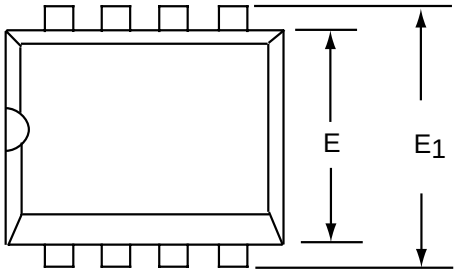


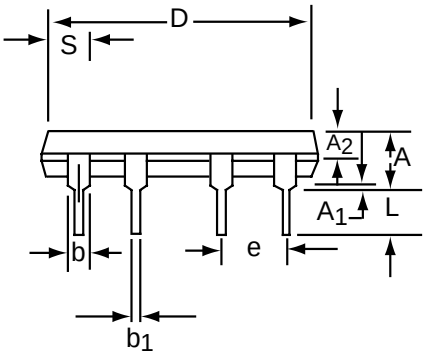
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-16	9.80	10.00	0.385	0.394
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020



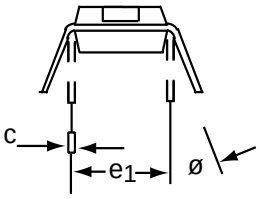
PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



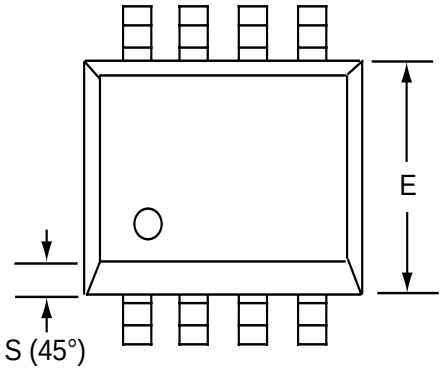


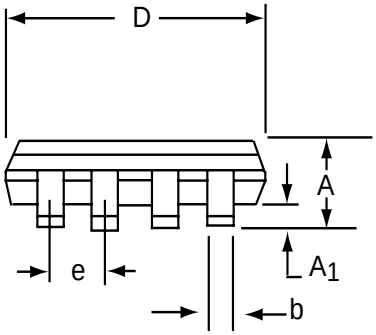
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°



SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package





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b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
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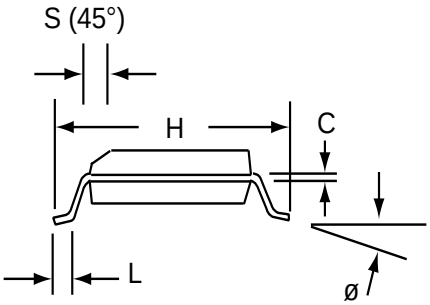
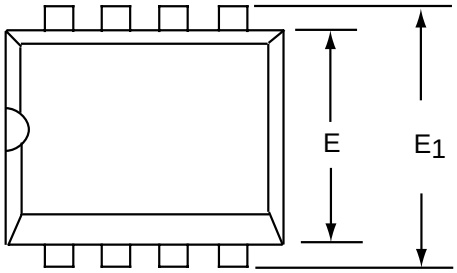
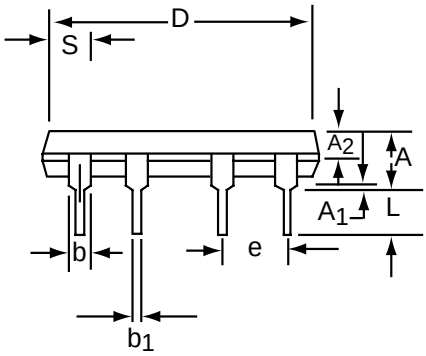


PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package





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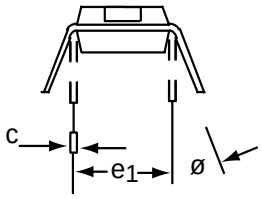

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