

Document Title**1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM****Revision History**

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Aug. 25 th , 2009	Preliminary
0.1	Revised ISB1 (110uA → 100uA)	Nov. 25 th , 2009	Preliminary
0.2	Removed Page Write Operation	Jul. 21 st , 2010	Final

1M x 16 bit Super Low Power and Low Voltage Full CMOS RAM

FEATURES

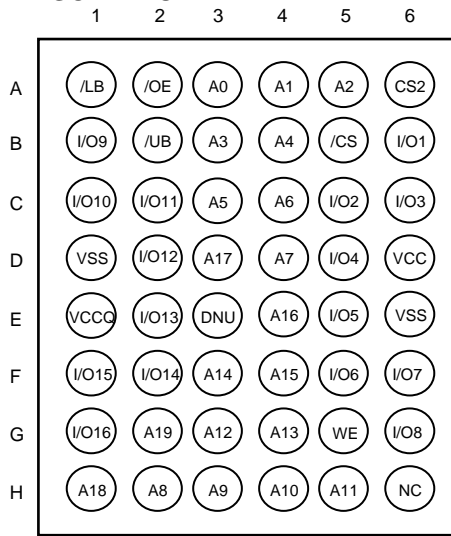
- Process Technology : Full CMOS
- Organization : 1M x 16
- Power Supply Voltage : 2.7~3.3V
- Three state output and TTL Compatible
- Separated I/O power(VCCQ) & Core power(VCC)
- Operating Temperature Ranges:
 - Special (-10°C to +60°C)
 - Commercial (0°C to +70°C)
 - Extended (-25°C to +85°C)
 - Industrial (-40°C to +85°C)
- Package Type : 48-FBGA-6.00x8.00 mm²
 FMP1617DA0(7)-HxxX : Pb-Free & Halogen Free
- Dual CS & Page Mode
 FMP1617DA0 : Dual CS
 FMP1617DA7 : Page mode with Dual CS
- Page read/write operation by 16 words

PRODUCT FAMILY

Product Family	Operating Voltage (V)			Speed	Power Dissipation					
	Min.	Typ.	Max.		ICC1		ICC2		ISB1 (CMOS Standby Current)	
					f = 1MHz		f = fmax			
					Typ.	Max.	Typ.	Max.	Typ.	Max.
FMP1617DA0(7)-H60E FMP1617DA0(7)-H70E	2.7	3.0	3.3	60ns 70ns	1.5mA	3mA	15mA 12mA	20mA	70uA	100uA

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{cc} = V_{cc} (typ) and T_A = 25°C.
2. H=FBGA(Pb-Free & Halogen Free), W=WAFER
3. Operating Temperature Range: S (-10°C~60°C), C(0°C~70°C), E(-25°C~85°C), I (-40°C~85°C)

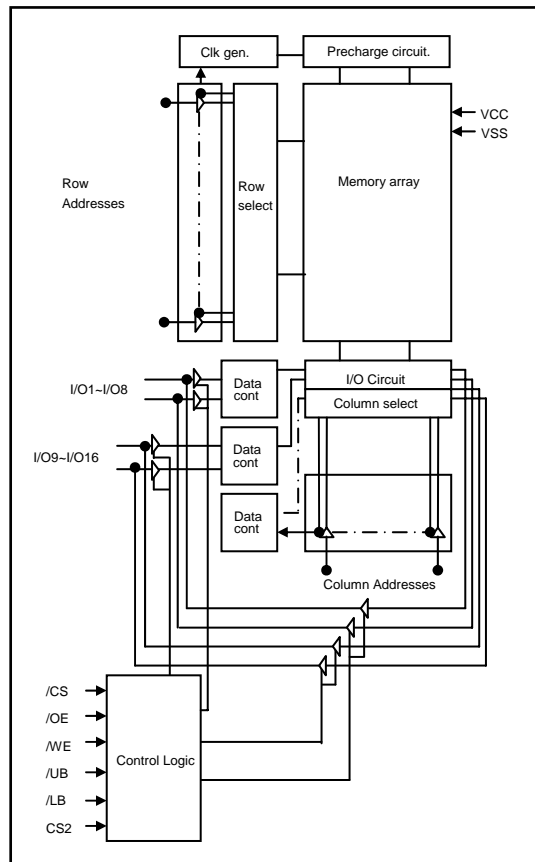
PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
CS2	Low Power Modes	VCC	Core Power
/CS	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A19	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



FMP1617DA0(7)

CMOS LPRAM

PRODUCT LIST

Part Name	Function
FMP1617DA0(7)-H60E FMP1617DA0(7)-H70E	60ns, VCC=3.0V, VCCQ=3.0V 70ns, VCC=3.0V, VCCQ=3.0V

1. H=FBGA(Pb-Free & Halogen Free), W=WAFER

2. Operating Temperature Range: S (-10°C-60°C), C(0°C-70°C), E(-25°C-85°C), I (-40°C-85°C)

FUNCTIONAL DESCRIPTION

/CS1	CS2	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselect/Power-down	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselect/Power-down	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselect/Power-down	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to VSS	VIN, VOUT	-0.5 to VCC+0.3V	V
Voltage on VCC supply relative to VSS	VCC	-0.2 to 3.6	V
Power Dissipation	PD	1.0	W
Storage temperature	TSTG	-65 to 150	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	FMP1617DA0(7)			Unit
		Min	Typ	Max	
Supply voltage	VCC	2.7	3.0V	3.3	V
I/O operating voltage (VCCQ ≤ VCC)	VCCQ	2.7	3.0V	3.3	V
Ground	VSS	0	0	0	V
Input high voltage	VIH	0.8VCCQ	VCCQ	VCC+0.2 ¹⁾	V
Input low voltage	VIL	-0.2 ²⁾	0	0.2VCCQ	V

Note :

1. Overshoot : Vcc+1.0V in case of pulse width ≤ 20ns.

2. Undershoot : -1.0V in case of pulse width ≤ 20ns.

3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

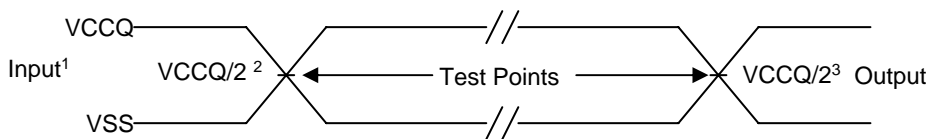
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	1	uA
Output leakage current	I _{LO}	/CS=V _{IH} , CS2=V _{IH} , /OE=V _{IH} or /WE=V _L , V _{IO} =V _{SS} to V _{CC}	-1	1	uA
Average operating current	I _{CC1}	Cycle time=1us, 100%duty, I _{IO} =0mA, /CS≤0.2V, CS2=V _{IH} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	3	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, /CS=V _L , CS2=V _{IH} , V _{IN} =V _L or V _{IH}	-	20	mA
Output low voltage	V _{OL}	I _{OL} =0.5mA		0.2V _{CCQ}	V
Output high voltage	V _{OH}	I _{OH} =-0.5mA	0.8V _{CCQ}		V
Standby Current(TTL)	I _{SB}	/CS=V _{IH} , CS2=V _{IH} , Other inputs=V _{IH} or V _L	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	/CS≥V _{CC} -0.2V, CS2≥V _{CC} -0.2V, Other inputs=0~V _{CC}	-	100	uA

Operating Range

Device	Range	Ambient Temperature	V _{CC}	V _{CCQ}
FMP1617DA0(7)-XxxS	Special	-10°C to +60°C	2.7V to 3.3V	2.7V to V _{CC}
FMP1617DA0(7)-XxxC	Commercial	0°C to +70°C		
FMP1617DA0(7)-XxxE	Extended	-25°C to +85°C		
FMP1617DA0(7)-XxxI	Industrial	-40°C to +85°C		

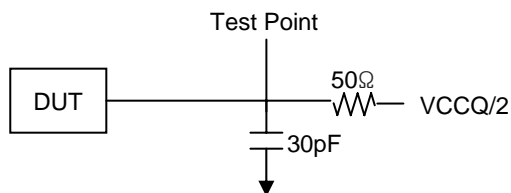
AC Input/Output Reference Waveform



NOTE:

1. AC test inputs are driven at V_{CCQ} for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at V_{CCQ}/2.
3. Output timing ends at V_{CCQ}/2.

AC Output Load Circuit



AC CHARACTERISTICS(VCC=2.7V~3.3V)

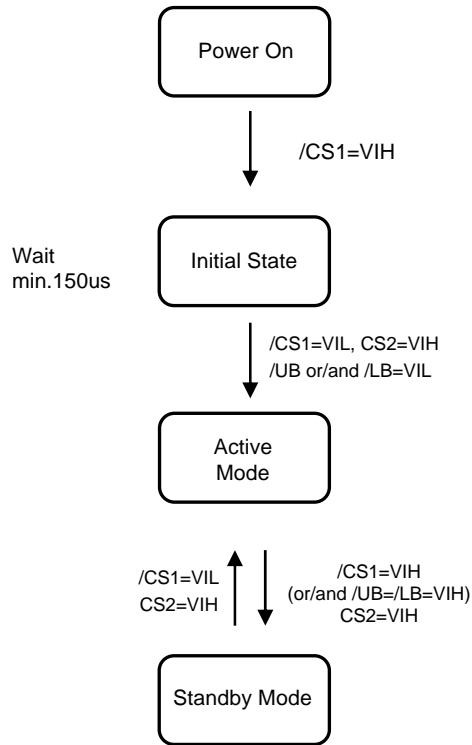
Parameter List		Symbol	Speed Bins				Units
			60ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	60	20k	70	20k	ns
	Address Access Time	tAA	-	60	-	70	ns
	Chip Select to Output	tCO	-	60	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	25	ns
	/UB, /LB Access Time	tBA	-	60	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	0	5	ns
	Output Hold from Address Change	tOH	5	-	5	-	ns
Write	Write Cycle Time	tWC	60	20k	70	20k	ns
	Chip Select to End of Write	tCW	50	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	50	-	60	-	ns
	/UB, /LB Valid to End of Write	tBW	50	-	60	-	ns
	Write Pulse Width	tWP	50	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	5	0	5	ns
	Data to Write Time Overlap	tDW	20	-	20	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	5	-	5	-	ns	
Page	Page Mode Cycle Time	tPC	20	-	25	-	ns
	Page Mode Address Access Time	tPAA	-	20	-	25	ns
	Maximum Cycle Time	tMRC	-	20k	-	20k	ns
/CS High Pulse Width		tCP	10	-	10	-	ns

1. /CS High Pulse Width is defined by /CS or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 150us with /CS=CS2=VIH

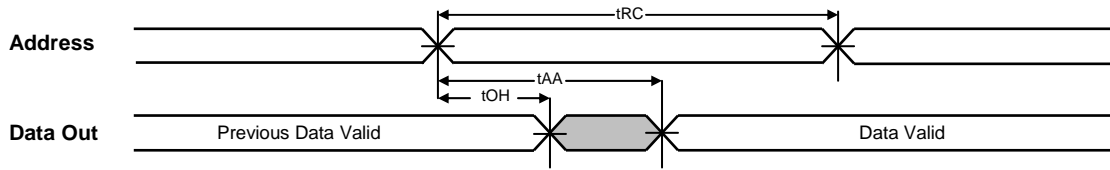
Standby Mode State machines



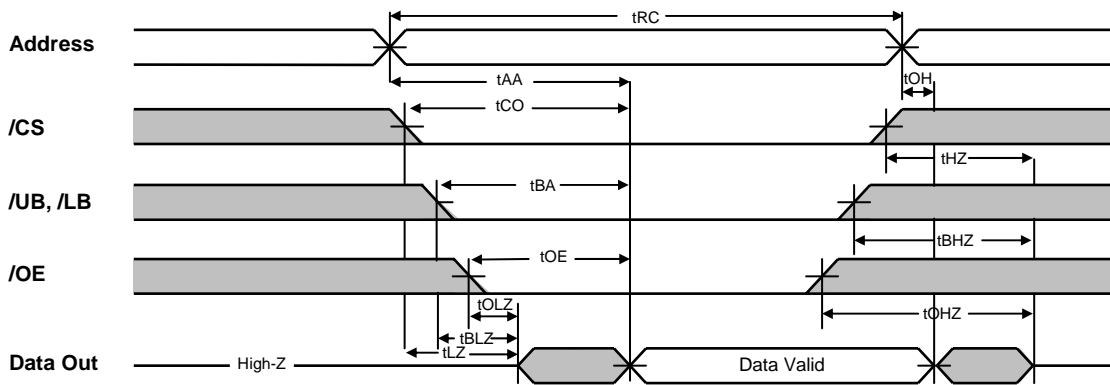
Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	100 (ISB1)	0

READ CYCLE (1) (Address controlled, /CS=/OE=VIL, CS2=/WE=VIH, /UB or/and /LB=VIL)

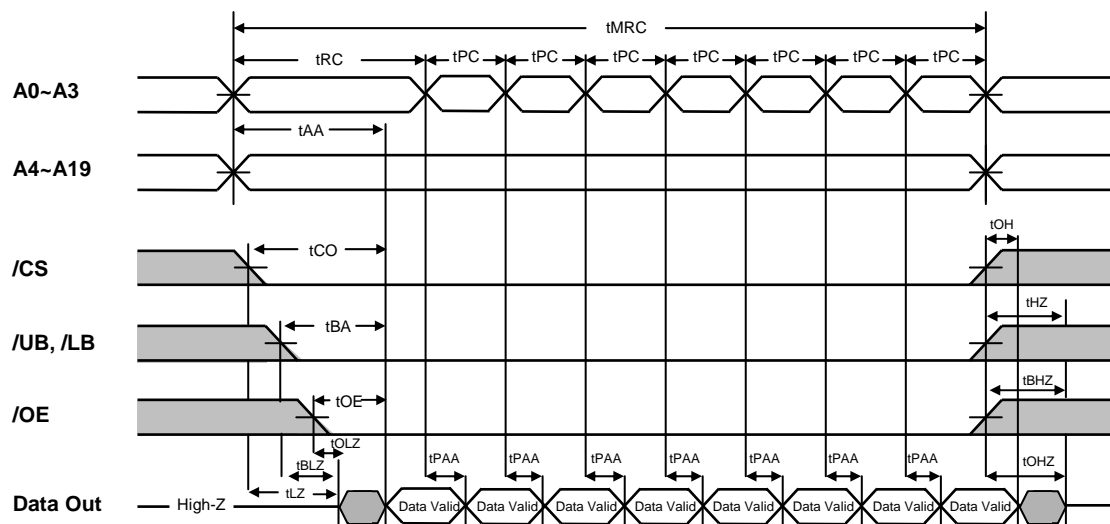


READ CYCLE (2) (CS2=/WE=VIH)



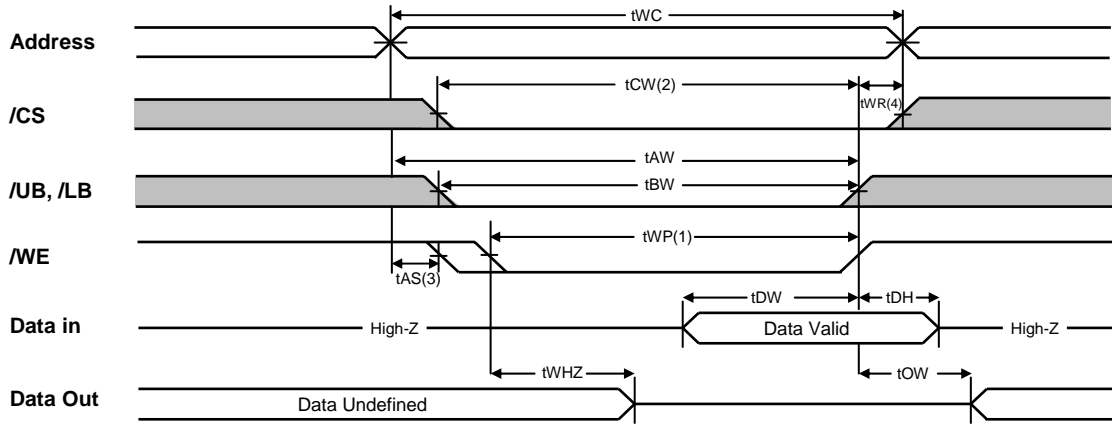
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 20 μ s.

PAGE READ CYCLE (CS2=/WE=VIH, 16 words access)

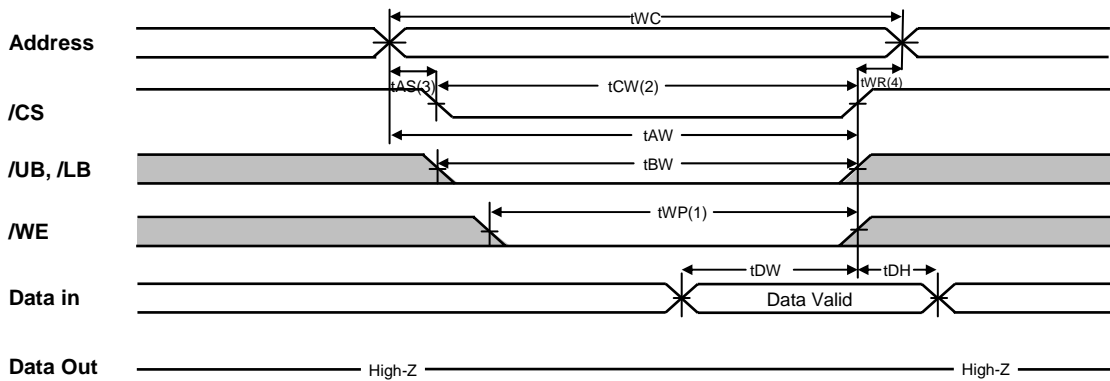


1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 20 μ s.
4. In case page address skew is over 3ns, t_{PAA} will be out of spec.

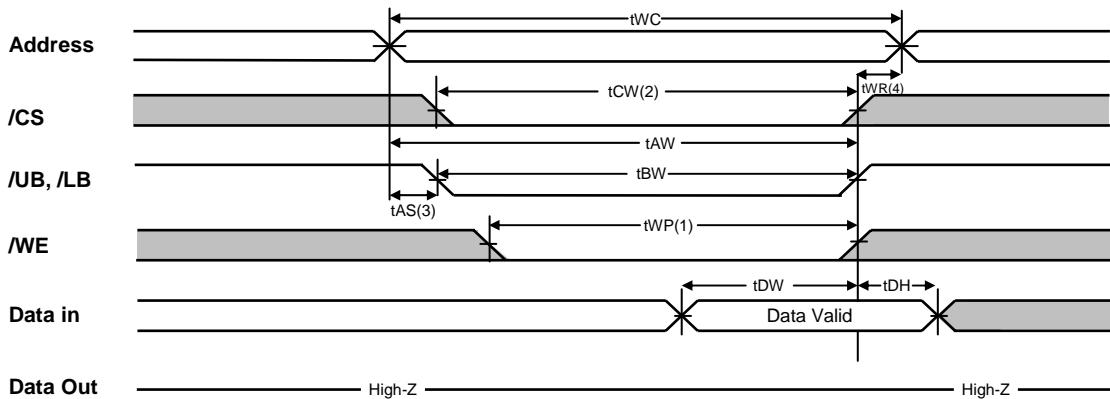
WRITE CYCLE (1) (*/WE* controlled, CS2=VIH)



WRITE CYCLE (2) (*/CS* controlled, CS2=VIH)



WRITE CYCLE (3) (*/UB*, */LB* controlled, CS2=VIH)



1. A write occurs during the overlap (t_{WP}) of low */CS* and */WE*. A write begins when */CS* goes low and */WE* goes low with asserting */UB* or */LB* for single byte operation or simultaneously asserting */UB* and */LB* for double byte operation. A write ends at the earliest transition when */CS* goes high and */WE* goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the */CS* going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as */CS* or */WE* going high.
5. Do not access device with cycle timing shorter than $t_{RC}(t_{WC})$ for continuous periods > 20 μ s.

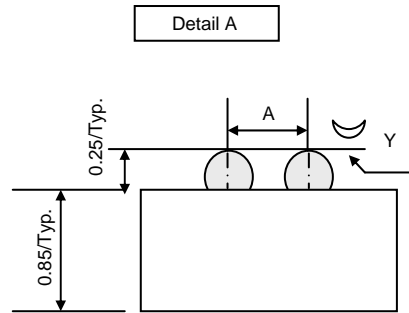
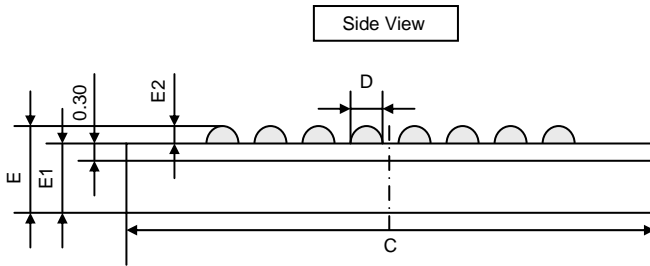
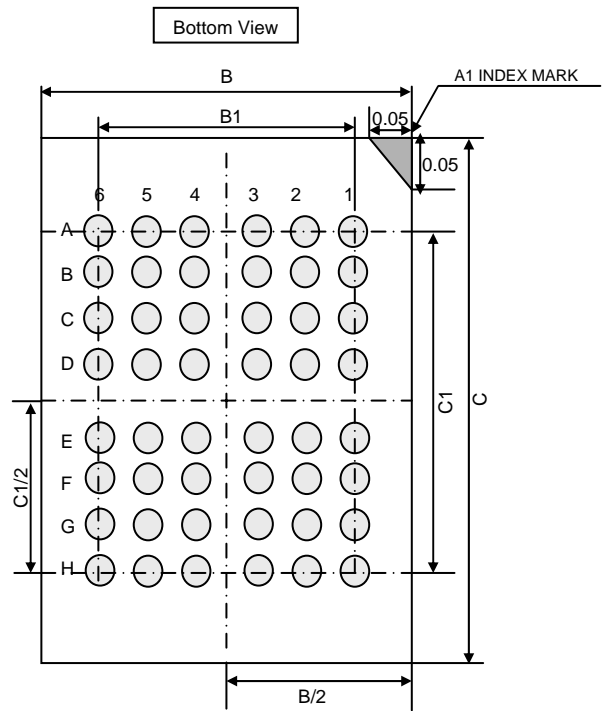
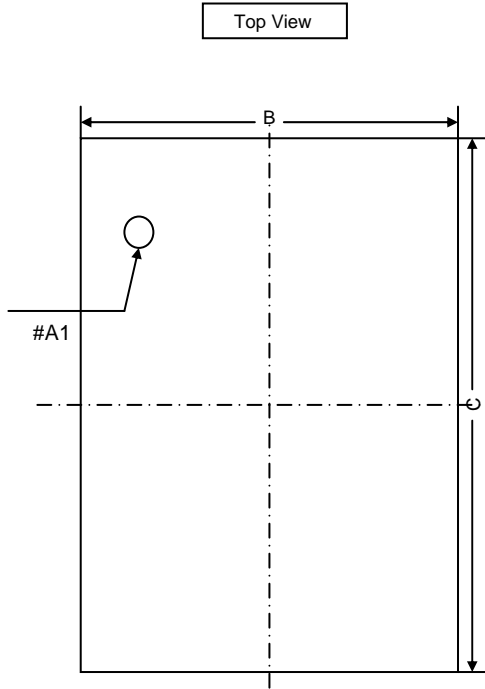
FMP1617DA0(7)

CMOS LPRAM

PACKAGE DIMENSION

Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)



	Min	Typ	Max
-			
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)