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S1R72V27
Data Sheet

SEIKO EPSON CORPORATION

Rev.1.00

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Scope

This document applies to the S1R72V27 USB 2.0 device/host controller LSI.

Contents

1. Overview

The S1R72V27 is a USB host/device controller LSI that supports the USB 2.0 high-speed mode. A single USB port can be operated as a USB host or USB device depending on how control is switched.

This LSI maintains high compatibility with the S1R72V17 but includes additional functions such as support for USB host isochronous transfers.

2. Features

<<USB 2.0 host functions>>

- Supports HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) transfer
- Built-in pull-down resistor for downstream ports (no external circuit required)
- Built-in HS termination (no external circuit required)
- Supports control, bulk, interrupt, and isochronous transfers

  Proven channel system designed specifically for embedded host

  Dedicated control transfer channel x1

  Dedicated bulk transfer channel x1

  Bulk, interrupt, and isochronous transfer channels x4
- USB power switching interface

<<USB 2.0 device functions>>

- Supports HS (480 Mbps) and FS (12 Mbps) transfer
- Built-in FS/HS termination (no external circuit required)
- VBUS 5V I/F (requires external protective circuit)
- Supports control, bulk, interrupt, and isochronous transfers
- Supports five bulk, interrupt, and isochronous transfers and Endpoint 0

<<MCU I/F>>

- Supports 16-bit width standard CPU bus I/F
- Includes DMA 1ch for each port (multi-word sequence)
- Big Endian (Includes bus-swapping function to support Little Endian CPUs)
- I/F variable voltage (3.3 V to 1.8 V)

<<Miscellaneous>>

- Clock input: Supports 12 MHz/24 MHz crystal oscillator. (built-in oscillator circuit and 1 MΩ feedback resistor)
- Dedicated terminals for 12/24/48 MHz clock input
- Power supply voltage: 3-voltage system including 3.3 V, 1.8 V, and CPU I/F power supply (3.3 V to 1.8 V)
- Package type QFP14-80, PFBGA5UX60, PFBGA8UX81
- Guaranteed operating temperature range: -40°C to 85°C

3. Block Diagram

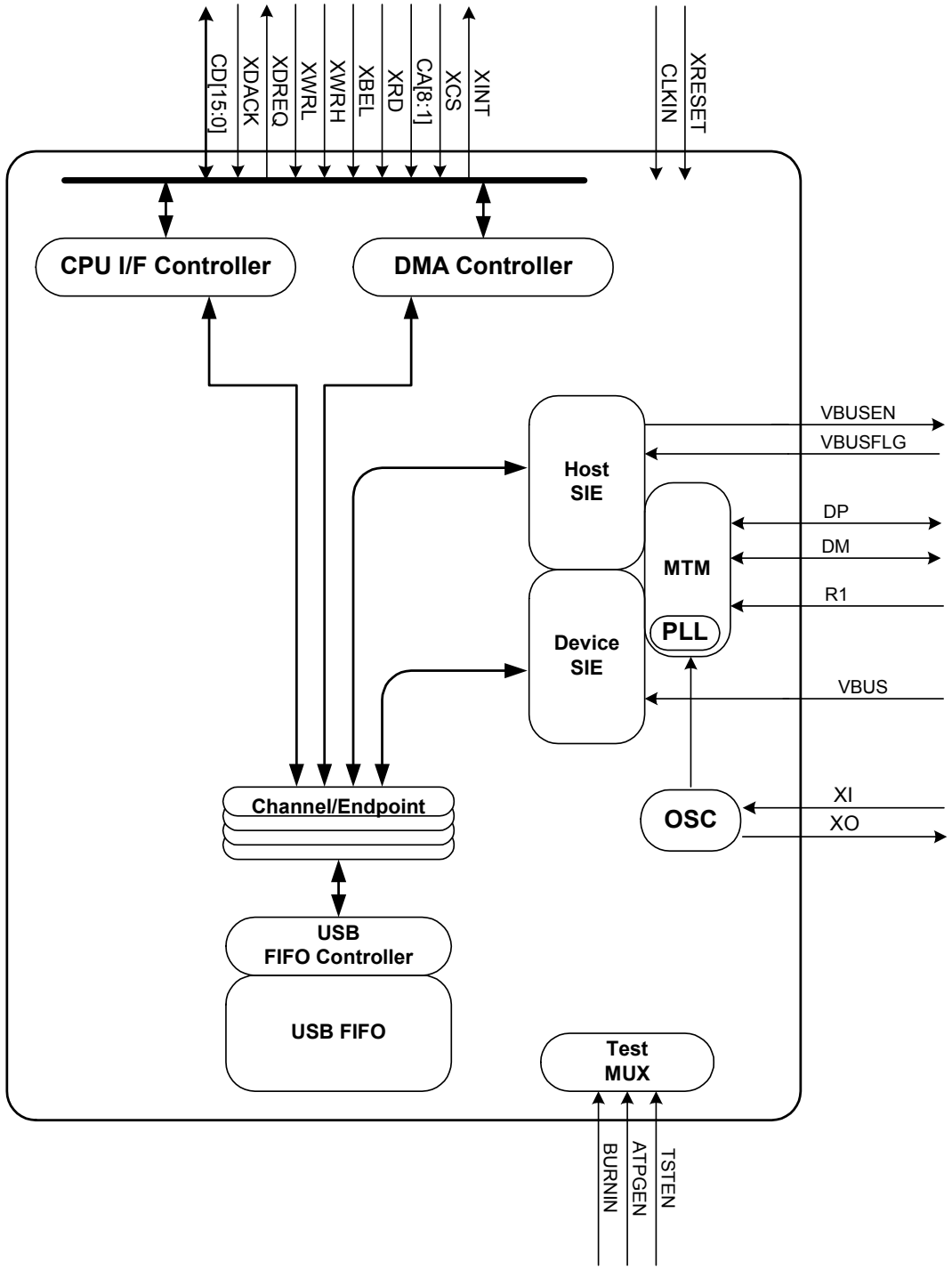


Figure 3-1 Overall block diagram

4. Explanation of Functions

For details of the register names used in the following discussion, refer to the Technical Manual for this LSI.

4.1 Power Supply

This LSI has three power supply systems and a common GND. The power supply systems consist of HVDD (3.3 V) for the USB I/O power supply, CVDD (3.3 V to 1.8 V) for the CPU I/F power supply, and LVDD (1.8 V) for internal circuits and TEST I/O. (See Figure 4-1.)

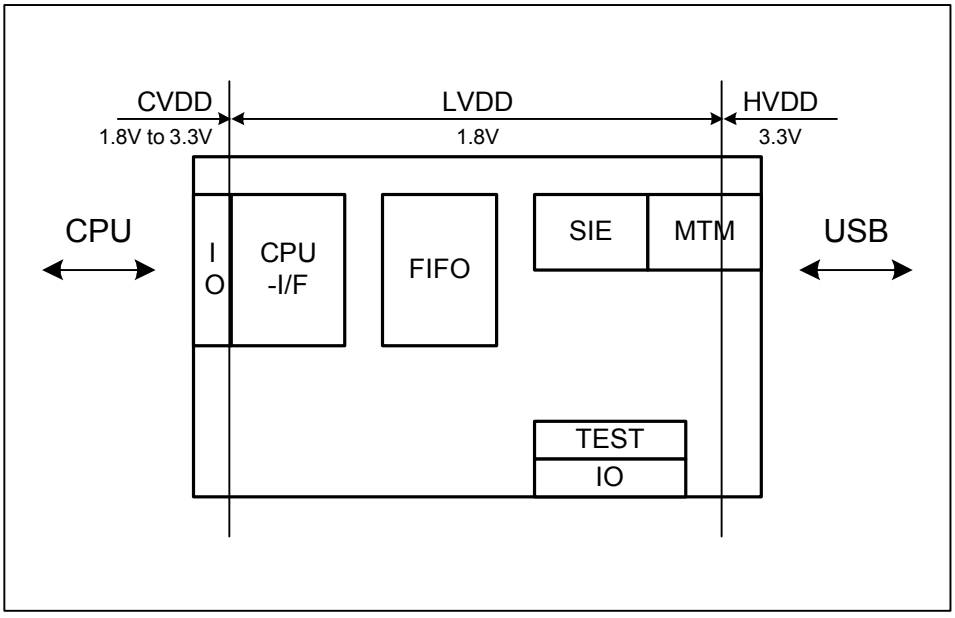


Figure 4-1 S1R72V27 power supply circuit diagram

The sequence of steps for turning the power supplies on and off are described below.

This LSI cannot be operated with only the LVDD or CVDD power supplies turned on or off. The HVDD can be turned off if the LVDD or CVDD power supplies are on. The synchronous register cannot be accessed while HVDD is off, since the PLL does not operate.

Also, the following restrictions apply to the sequence for turning the CVDD/HVDD I/O power supplies and LVDD internal power supply on or off. There are no restrictions on the sequence for turning the CVDD and HVDD power supplies on or off.

- The LVDD must be turned on before turning on the CVDD and HVDD power supplies.
- In the powering off sequence, the CVDD and HVDD must be turned off before turning off the LVDD.

If power supply circuit characteristics or the power supply load make this sequence impossible to follow, the CVDD or HVDD must not be on for more than 1 second while the LVDD is off.

4.2 Reset

This LSI includes a hard reset function using the external XRESET terminal and a soft reset function using register settings.

4.2.1 Hard Reset

Start up from reset status when power is turned on, then cancel the reset after confirming power on.

4.2.2 Soft Reset

Circuits related to the USB port or individual internal USB analog macros can be reset via software. This LSI can be soft reset using the ChipReset.AllReset bit. The ChipReset.ResetMTM bit is used to reset USB analog macros. Note, however, that analog macros should only be reset in the sleep state.

4.3 Clock

This LSI contains an internal oscillator and feedback resistor (1 MΩ) and supports clock generation using an external oscillator. External clock input is supported via the CLKIN terminal.

The oscillator frequency supports 12 MHz or 24 MHz using the internal oscillator. Frequencies of 12, 24, or 48 MHz are supported via the external input.

Figure 4-2 shows a typical connection arrangement for an oscillation circuit. Contact the oscillator manufacturer to determine circuit constants, as Cd, Cg, and Rd in the oscillator circuit must be matched, based on the oscillator.

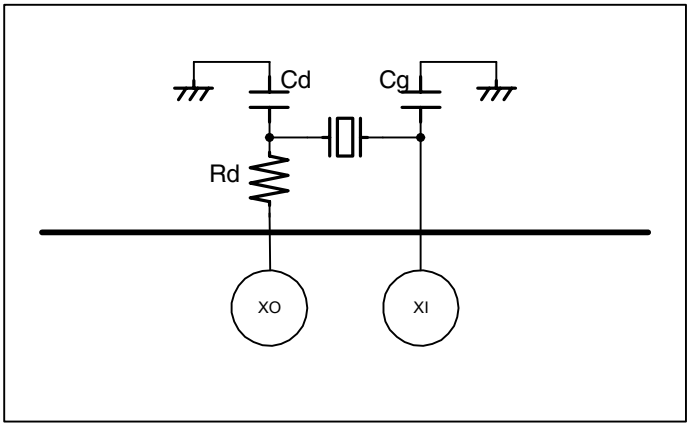


Figure 4-2 Clock generation using the internal oscillator and external oscillator

4.4 Power Management

This LSI includes a power management function featuring two power management states, SLEEP and ACTIVE, together with the CPU_Cut power management state. (See Figure 4-3.)

All function blocks are active in the ACTIVE state, whereas only the bare minimum circuits necessary for restarting from standby mode are active in SLEEP state. CPU_Cut mode minimizes power consumption attributable to the CPU-I/F input buffer.

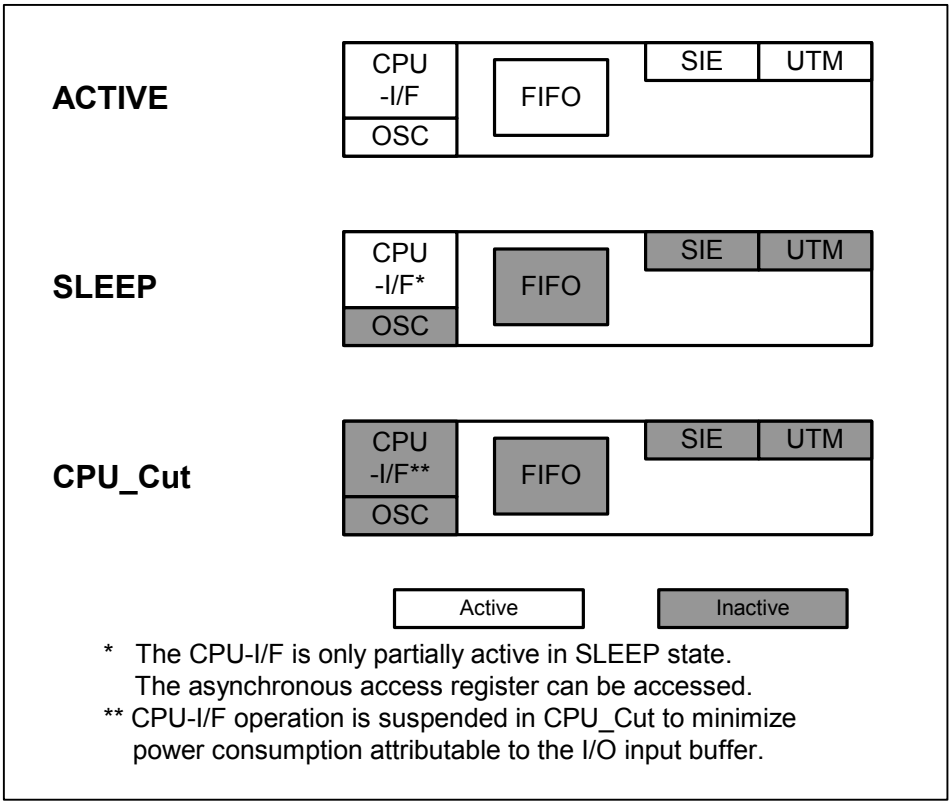


Figure 4-3 Power management states

4.5 CPU-I/F

This LSI is connected to the CPU via a 16-bit interface. Endian settings can be set as Big Endian or Little Endian in 16-bit steps. For Big Endian, registers with even addresses can be accessed above the bus (CD[15:8]), while registers with odd addresses can be accessed below the bus (CD[7:0]). For Little Endian, registers with even addresses can be accessed below the bus (CD[7:0]), while registers with odd addresses can be accessed above the bus (CD[15:8]).

The bus mode can be set to either Strobe mode for access using high/low strobe (XWRH/XWRL) or Byte Enable mode for access using high/low byte enable (XBEH/XBEL) for writing the first or last 8 bits. Endian and bus mode is set by the CPUIF_MODE register immediately cancelling of hard reset.

The CPU-I/F on this LSI includes 1-ch DMA (slave).

The registers that can be accessed will depend on the power management state. For details, refer to the LSI Technical Manual.

4.6 USB Device I/F

This LSI supports High-Speed specification USB device functions complying with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.6.1 Speed Mode and Transfer Type

This LSI's USB device function supports HS (480 Mbps) and FS (12 Mbps) speed modes. The speed mode is set automatically by the speed negotiation performed when resetting the bus. For example, HS transfer mode is selected automatically by speed negotiation if connected to a USB host that supports HS speed mode. In addition, the register can be set so that FS speed mode is always selected in speed negotiations.

All transfer types stipulated under the USB 2.0 standard are supported, including control transfers (endpoint 0), bulk transfers, interrupt transfers, and isochronous transfers.

4.6.2 Resources

4.6.2.1 Endpoint

This LSI's USB device function includes endpoint 0 and five standard endpoints. Endpoint 0 supports control transfers. The standard endpoints support bulk transfers, interrupt transfers, and isochronous transfers. The standard endpoint numbers, maximum packet size, and transfer direction (in/out) can be set as desired.

4.6.2.2 FIFO

The LSI ports include 4.5 kB of FIFO for use with USB data transfers. This forms the data transfer route with USB. The FIFO capacity of each endpoint can be assigned as desired by the software. For example, performance can be improved by assigning a sufficient size FIFO area to the endpoints for bulk transfers.

4.6.3 Data Flow

Endpoints are assigned to USB FIFO areas on a one-to-one basis, and responses are returned to USB transactions automatically, depending on effective USB FIFO free capacity (for OUT transfers) or effective data quantity (for IN transfers). This means the software does not need to be directly involved in individual transactions, allowing USB data transfers to be controlled as data flows at the USB FIFO.

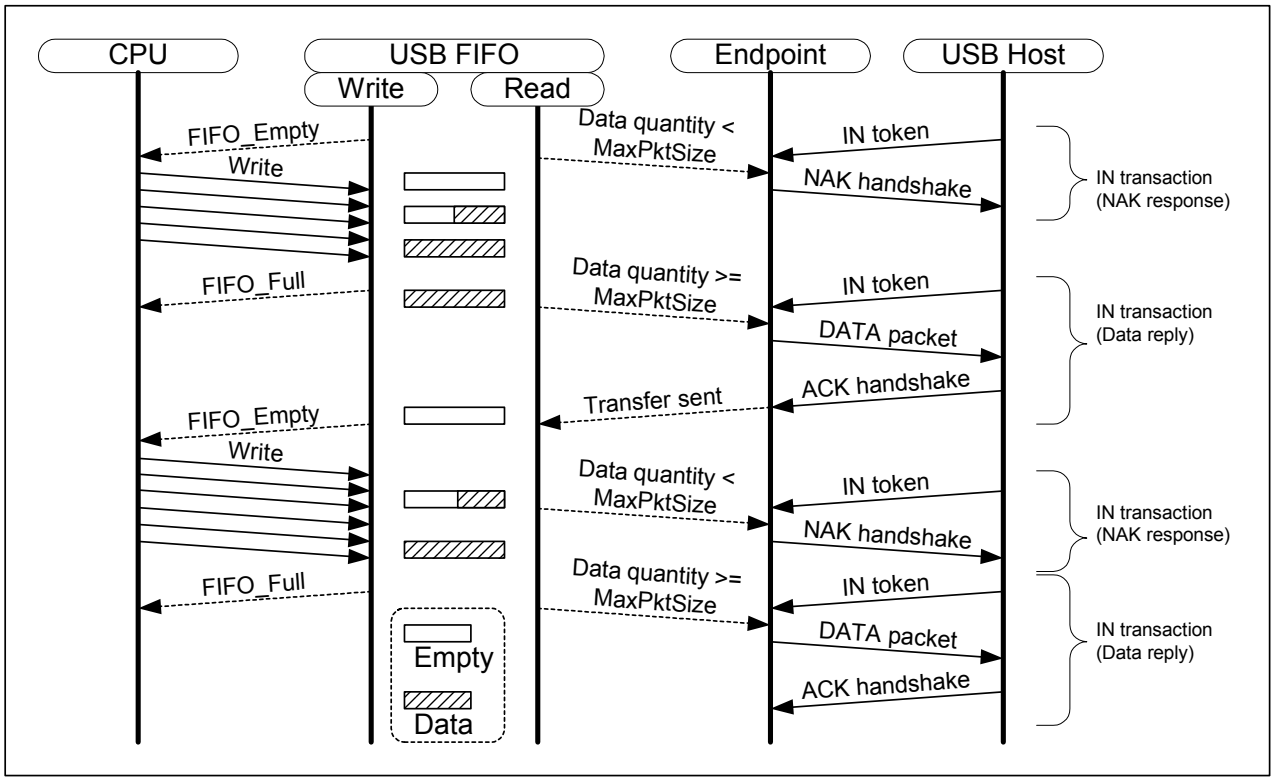


Figure 4-4 Typical data flow (with FIFO assigned for MaxPktSize and IN transfer)

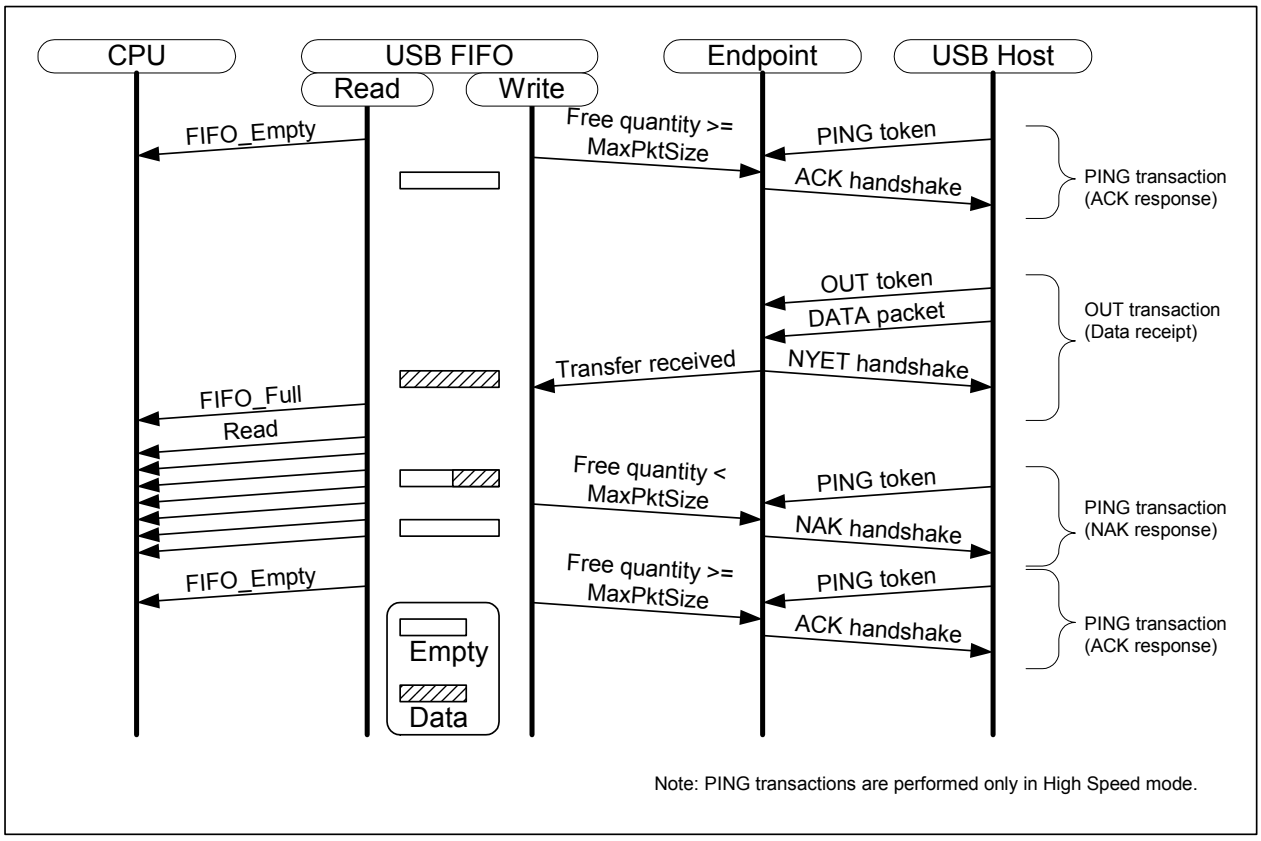


Figure 4-5 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfer)

4.6.4 USB Device Port External Circuits

The LSI USB Port 0 has internal FS and HS device termination resistors, eliminating the need for the components normally used to adjust impedance. This allows a DP/DM line to be connected directly between the LSI terminal and the connector. Note that the appropriate components must be used to ensure static electricity protection and to implement EMI precautions.

The VBUS terminal uses a 5 V input and does not require external voltage conversion. A protection circuit is recommended, since certain commercially-available USB host and hub products may apply surge voltages exceeding VBUS ratings.

Refer to the separately provided PCB Design Guidelines for S1R72V Series USB 2.0 Hi-Speed.

4.7 USB Host I/F

The LSI USB Port 0 and Port 1 support high-speed specification USB host functions complying with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.7.1 Speed Mode and Transfer Type

This LSI's USB host function supports HS (480 Mbps), FS (12 Mbps) and LS (1.5 Mbps) speed modes. The speed mode is automatically set by speed negotiations performed on resetting the bus.

All transfer types stipulated in the USB 2.0 standard are supported, including control transfers, bulk transfers, interrupt transfers, and isochronous transfers.

4.7.2 Resources

4.7.2.1 Channels

In the LSI USB host functions, sets of register settings for transfers with end points on a one-to-one basis are called channels. The LSI USB host function features one dedicated channel for control transfers, one dedicated channel for bulk transfers, and four general channels that support bulk transfers, interrupt transfers, and isochronous transfers. The endpoint number, maximum packet size, and transfer direction (IN/OUT) can be set as desired for all channels. Transfers are also possible for a number of endpoints exceeding the channel number using software-based time-multiplexing for the channels.

4.7.2.2 FIFO

Each port on the LSI includes 4.5 kB of FIFO for use with USB data transfers. This forms the data transfer route with USB. The FIFO capacity for each channel can be assigned as desired by the software. For example, to improve performance, assign a FIFO area of adequate size to the endpoints for bulk transfers.

4.7.3 Data Flow

The channels are assigned to FIFO areas on a one-to-one basis. Transactions are sent automatically to USB, depending on the FIFO effective free capacity (for IN transfers) or effective data quantity (for OUT transfers). The software does not need to be directly involved in individual transactions, allowing USB data transfers to be controlled as data flow at the FIFO.

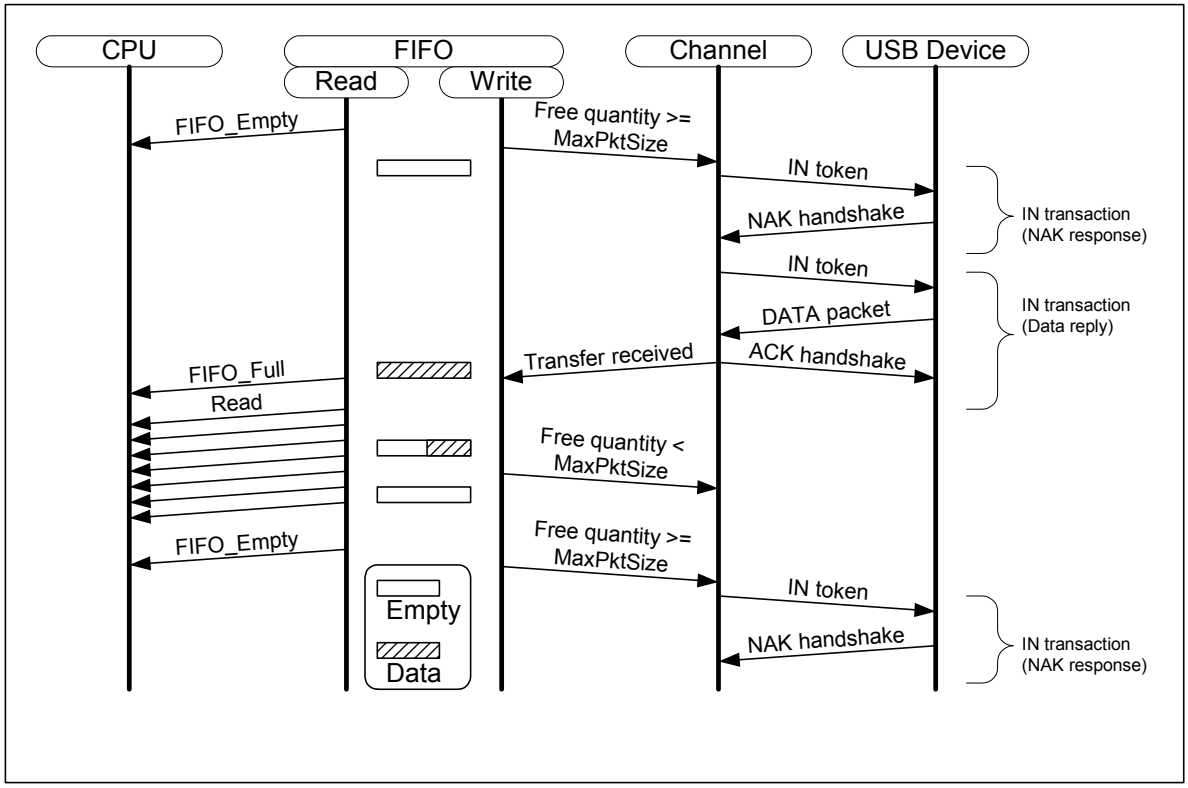


Figure 4-6 Typical data flow (with FIFO assigned for MaxPktSize and IN transfer)

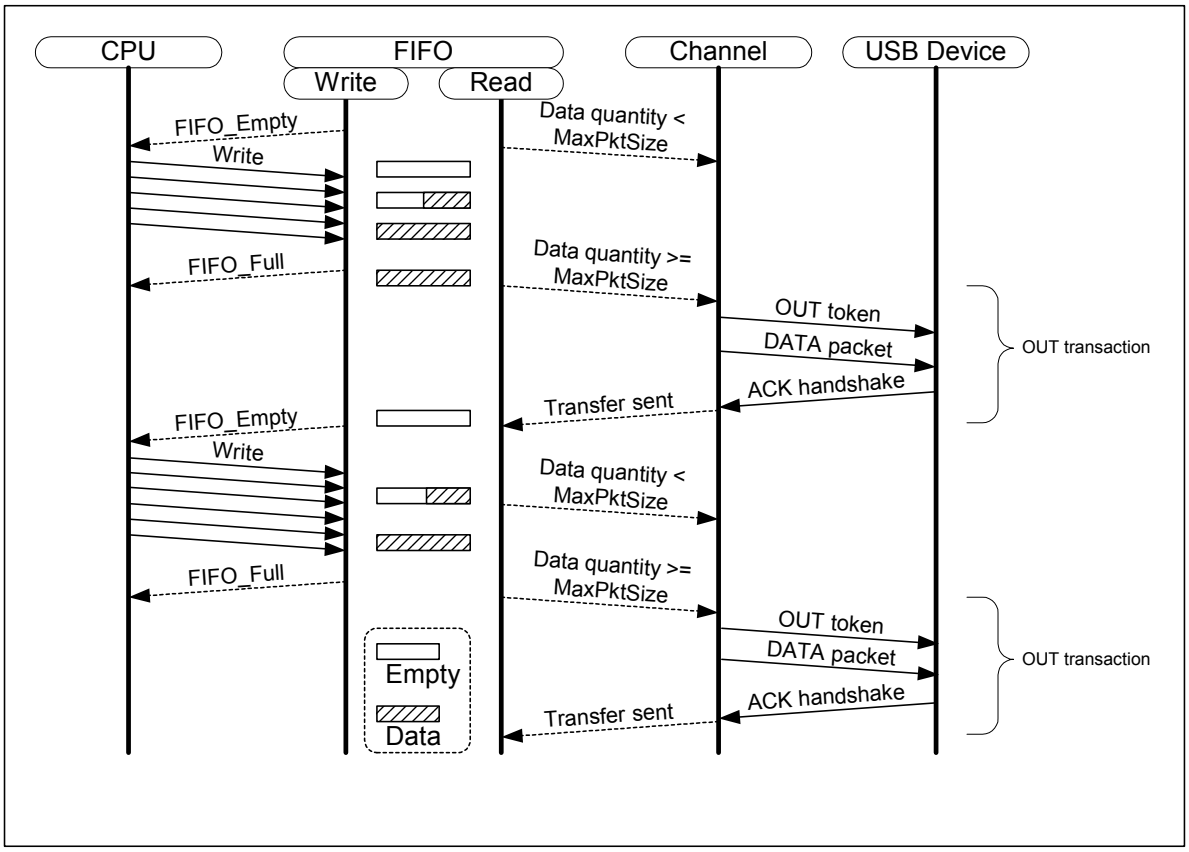


Figure 4-7 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfer)

4.7.4 USB Host Port External Circuits

The LSI ports have internal USB host termination resistors, including an HS termination resistor, eliminating the need for the external components normally used to adjust impedance. This allows a DP/DM line to be connected between the LSI terminal and the connector. Note that the appropriate components must be used to ensure static electricity protection and to implement EMI precautions.

An external VBUS control component is required for the VBUS.

4.8 FIFO

The LSI includes 4.5 kB of USB FIFO for use with USB data transfers. The USB FIFO capacity for each endpoint or channel can be assigned as desired using the register settings.

Transfers are possible between the USB-I/F and CPU-I/F via the USB FIFO.

5. Terminal Layout Diagrams

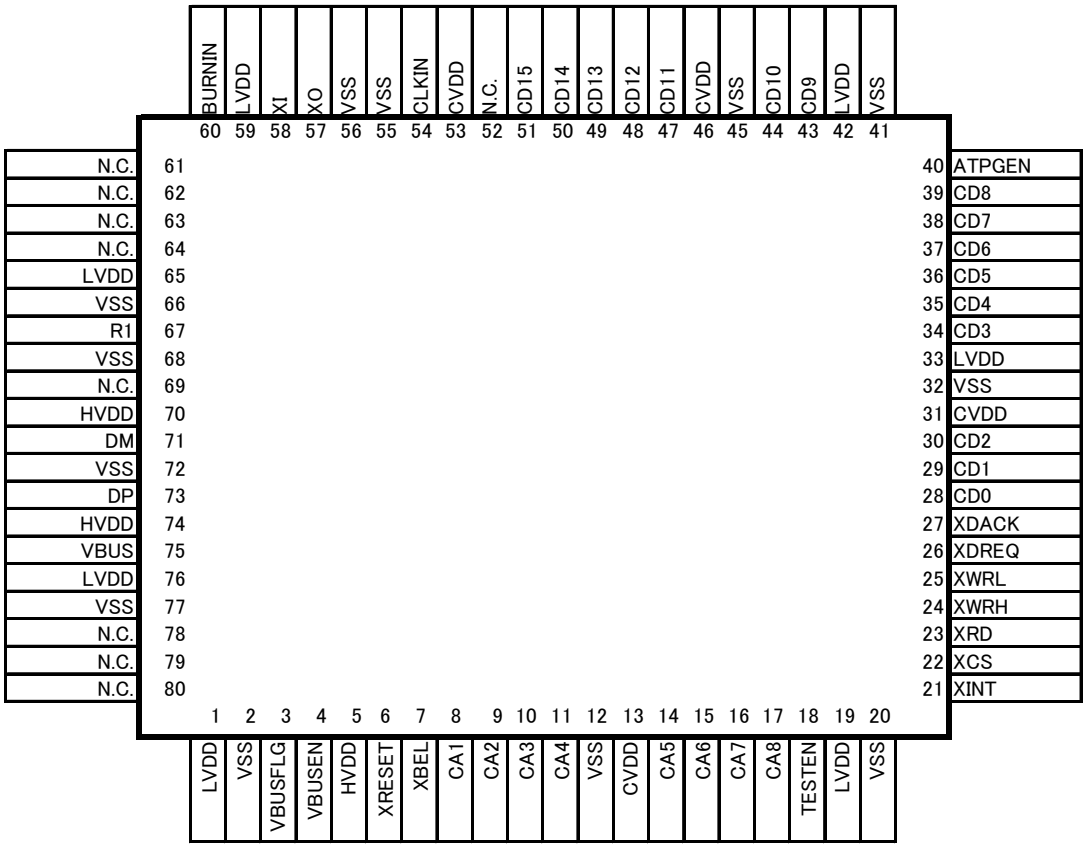


Figure 5-1 QFP package terminal layout diagram (QFP14-80)

	1	2	3	4	5	6	7	8	
A	NC	LVDD	DP	DM	HVDD	R1	LVDD	BURNIN	A
B	VBUSFLG	VSS	HVDD	VSS	VSS	VSS	VSS	XI	B
C	VBUSEN	HVDD	VBUS	CA1	CA3	CD15	LVDD	XO	C
D	XRESET	XBEL	CA5			CD13	CVDD	CLKIN	D
E	CA2	CA4	XINT			CD4	CD11	CD14	E
F	CA7	CA8	XWRH	XDACK	CD3	CD7	CD10	CD12	F
G	CA6	LVDD	XRD	XDREQ	CD1	CD6	VSS	CD9	G
H	TESTEN	XCS	XWRL	CD0	CD2	CD5	CD8	ATPGEN	H
	1	2	3	4	5	6	7	8	

Top View

Figure 5-2 BGA package terminal layout diagram (PFBGA5UX60)

	1	2	3	4	5	6	7	8	9	
A	NC	LVDD	HVDD	DP	DM	HVDD	R1	LVDD	NC	A
B	VSS	VSS	VBUS	VSS	VSS	VSS	VSS	VSS	XI	B
C	VBUSFLG	HVDD	LVDD	XBEL	CA1	CVDD	BURNIN	LVDD	XO	C
D	XRESET	VBUSEN	CA3	NC	NC	NC	CD12	CD15	CLKIN	D
E	CA2	VSS	CA4	NC	NC	NC	VSS	CD13	CD14	E
F	CVDD	CA5	CA8	NC	NC	NC	CD7	CD9	CD11	F
G	CA7	CA6	TESTEN	XCS	XDACK	CD0	CD4	CD8	CD10	G
H	LVDD	XINT	XWRL	XRD	CD1	CVDD	CD6	ATPGEN	LVDD	H
J	NC	VSS	XWRH	XDREQ	CD2	CD3	CD5	VSS	NC	J
	1	2	3	4	5	6	7	8	9	

Top View

Figure 5-3 BGA package terminal layout diagram (PFBGA8UX81)

6. Terminal Functions

OSC

QFP Pin	BGA5 Ball	BGA8 Ball	Name	I/O	RESET	Terminal type	Terminal description
58	B8	B9	XI	IN	-	Analog	Internal oscillator circuit input (12 MHz, 24 MHz)
57	C8	C9	XO	OUT	-	Analog	Internal oscillator circuit output

The clock inputs from the crystal oscillator and CLKIN for XI and XO are used exclusively by the register settings. Fix XI at Low when using CLKIN.

TEST

QFP Pin	BGA5 Ball	BGA8 Ball	Name	I/O	RESET	Terminal type	Terminal description
18	H1	G3	TESTEN	IN	(PD)	(PD)	Test terminal (Set to Low)
40	H8	H8	ATPGEN	IN	(PD)	(PD)	Test terminal (Set to Low)
60	A8	C7	BURNIN	IN	(PD)	(PD)	Test terminal (Set to Low)

USB

QFP Pin	BGA5 Ball	BGA8 Ball	Name	I/O	RESET	Terminal type	Terminal description
67	A6	A7	R1	IN	-	Analog	Internal operation reference current setting terminal Connect 6.2 kW ±1% resistance between terminal and VSS
73	A3	A4	DP	BI	Hi-Z	Analog	USB port 0, data line (Data +)
71	A4	A5	DM	BI	Hi-Z	Analog	USB port 0, data line (Data -)
3	B1	C1	VBUSFLG	IN	(PU)	Schmitt (PU)	USB power switch fault detection signal (1: Normal, 0: Error)
4	C1	D2	VBUSEN	OUT	Lo	2mA	USB power switch control signal
75	C3	B3	VBUS	IN	(PD)	(PD)	USB device bus detection signal

PD: Pull Down

PU: Pull Up

CPU I/F

QFP Pin	BGA5 Ball	BGA8 Ball	Name	I/O	RESET	Terminal type	Terminal description	
						Bus Mode ⇒	Strobe Mode	BE Mode
6	D1	D1	XRESET	IN	-	Schmitt	Reset signal	
54	D8	D9	CLKIN	IN	-	-	External clock input	
23	G3	H4	XRD	IN	-	-	Read/strobe	
25	H3	H3	XWRL (XWR)	IN	-	-	Write/strobe (lower)	Write/strobe
24	F3	J3	XWRH (XBEH)	IN	-	-	Write/strobe (upper)	High-byte enable
22	H2	G4	XCS	IN	-	Schmitt	Chip select signal	
21	E3	H2	XINT	OUT	High	2mA (Tri-state)	Interrupt output signal	
26	G4	J4	XDREQ	OUT	High	2mA	DMA request	
27	F4	G5	XDACK	IN	-	-	DMA acknowledge	
7	D2	C4	XBEL	IN	-	-	Set to High or Low	Low-byte enable
8	C4	C5	CA1	IN	-	-	CPU bus address	
9	E1	E1	CA2	IN	-	-		
10	C5	D3	CA3	IN	-	-		
11	E2	E3	CA4	IN	-	-		
14	D3	F2	CA5	IN	-	-		
15	G1	G2	CA6	IN	-	-		
16	F1	G1	CA7	IN	-	-		
17	F2	F3	CA8	IN	-	-		
28	H4	G6	CD0	BI	Hi-Z	2mA	CPU data bus	
29	G5	H5	CD1	BI	Hi-Z	2mA		
30	H5	J5	CD2	BI	Hi-Z	2mA		
34	F5	J6	CD3	BI	Hi-Z	2mA		
35	E6	G7	CD4	BI	Hi-Z	2mA		
36	H6	J7	CD5	BI	Hi-Z	2mA		
37	G6	H7	CD6	BI	Hi-Z	2mA		
38	F6	F7	CD7	BI	Hi-Z	2mA		
39	H7	G8	CD8	BI	Hi-Z	2mA		
43	G8	F8	CD9	BI	Hi-Z	2mA		
44	F7	G9	CD10	BI	Hi-Z	2mA		
47	E7	F9	CD11	BI	Hi-Z	2mA		
48	F8	D7	CD12	BI	Hi-Z	2mA		
49	D6	E8	CD13	BI	Hi-Z	2mA		
50	E8	E9	CD14	BI	Hi-Z	2mA		
51	C6	D8	CD15	BI	Hi-Z	2mA		

The XINT terminal can be set to 1/0 or Hi-Z/0 mode, depending on register settings. Note, however, that it cannot be pulled up with a voltage exceeding the rated value even in Hi-Z/0 mode, since it is not an open drain.

The clock inputs from the crystal oscillator and CLKIN for XI and XO are used exclusively by the register settings. Fix CLKIN at Low when using XI and XO.

PD: Pull Down

PU: Pull Up

POWER

QFP Pin	BGA5 Ball	BGA8 Ball	Name	Voltage	Terminal description
5, 70, 74	A5, B3, C2	A3, A6, C2	HVDD	3.3V	USB I/O power supply
13, 31, 46, 53	D7	C6, F1, H6	CVDD	1.8 to 3.3V	CPU I/F I/O power supply
1, 19, 33, 42, 59, 65, 76	A2, A7, C7, G2	A2, A8, C3, C8, H1, H9	LVDD	1.8V	OSC I/O, TEST I/O, and internal power supply
2, 12, 20, 32, 41, 45, 55, 56, 66, 68, 72, 77	B2, B4, B5, B6, B7, G7	B1, B2, B4, B5, B6, B7, B8, E2, E7, J2, J8	VSS	0V	GND
52, 61, 62, 63, 64, 69, 78, 79, 80	A1	A1, A9, D4, D5, D6, E4, E5, E6, F4, F5, F6, J1, J9	N.C.	0V	NC terminal (connect to GND)

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	HVDD	VSS - 0.3 to 4.0	V
	CVDD	VSS - 0.3 to 4.0	V
	LVDD	VSS - 0.3 to 2.5	V
Input voltage	HVI	VSS - 0.3 to HVDD + 0.5	V
	CVI*1	VSS - 0.3 to CVDD + 0.5	V
	VVI*2	VSS - 0.3 to 6.0	V
	LVI*3	VSS - 0.3 to LVDD + 0.5	V
Output voltage	HVO	VSS - 0.3 to HVDD + 0.5	V
	CVO*1	VSS - 0.3 to CVDD + 0.5	V
Output current/terminal	IOUT	±10	mA
Storage temperature	Tstg	-65 to 150	°C

*1 CPU-IF

*2 VBUS

*3 XI, TESTEN, ATPGEN, BURNIN

7.2 Recommended Operating Conditions

Item	Symbol	MIN	TYP	MAX	Units
Power supply voltage	HVDD	3.00	3.30	3.60	V
	CVDD	1.65	-	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage	HVI	-0.3	-	HVDD+0.3	V
	CVI*1	-0.3	-	CVDD+0.3	V
	VVI*2	-0.3	-	6.0	V
	LVI*3	-0.3	-	LVDD+0.3	V
Ambient temperature	Ta	-40	25	85	°C

*1 CPU-I/F

*2 VBUS

*3 XI, TESTEN, ATPGEN, BURNIN

Turn on power to the IC in the sequence shown below.

LVDD (internal) → HVDD, CVDD (IO section)

Likewise, turn off power to the IC in the sequence shown below.

HVDD, CVDD (IO section) → LVDD (internal)

Note:
Avoid leaving the HVDD or CVDD on continuously (for more than 1 second) when the LVDD is off, as doing so may affect chip reliability.

7.3 DC Characteristics

7.3.1 Current Consumption

Item	Symbol	Condition	MIN	TYP	MAX	Units
Power supply feed current	*1					
Power supply current	IDDH	HVDD = 3.3V(typ)	-	7.9	12.0	mA
	IDDCH	CVDD = 3.3V(typ)	-	1.6	5.0	mA
	IDDCL	CVDD = 1.8V(typ)	-	0.7	2.0	mA
	IDDL	LVDD = 1.8V(typ)	-	40.2	62.0	mA
Stationary current	*2					
Power supply current	IDDS	VIN = HVDD,CVDD,LVDD or VSS HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V	-	-	25	μA
Input leakage						
Input leakage current	IL	HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V HVIH = HVDD CVIH = CVDD LVIH = LVDD VIL = VSS	-5	-	5	μA
Input leakage						
Input leakage current (5 V tolerant)	ILIF	HVDD = 3.0V CVDD = 1.65V LVDD = 1.65V HVOH = 5.5V	-10	-	10	μA

*1: TYP is the measured value when transferring data with the USB-HDD connected as the USB host. MAX is the value estimated from this value.

*2: Stationary current with Ta = 25°C and both terminals in input mode.

Current consumption measurements for individual power management states using Seiko Epson operating conditions (Ta = 25°C)

Item	Condition	TYP	Units
CPU_Cut	CPU bus operation *1		
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	4.2	uW
SLEEP	CPU bus operation *1		
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	8.8	uW
ACTIVE (when operating as USB device) (USB ⇔ CPU-I/F)	*2		
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	98	mW
ACTIVE (when operating as USB host) (USB ⇔ CPU-I/F)	*3		
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	118	mW

*1: Excluding current consumption due to DP pull-up resistance inside S1R72V27 (approx. 200 µA).

*2: When transferring data connected to a PC as a USB device (actual transfer rate 13.5 MB/s).

*3: When transferring data with the USB-HDD connected as the USB host (actual transfer rate 13 MB/s).

7.3.2 Input Characteristics

Item	Symbol	Condition	MIN	TYP	MAX	Units
Input characteristics (LVCMOS)	Terminal names:	TESTEN, ATPGEN, BURNIN				
H level input voltage	VIH1	LVDD = 1.95V	1.27	-	-	V
L level input voltage	VIL1	LVDD = 1.65V	-	-	0.57	V
Input characteristics (LVCMOS)	Terminal names:	CA[8:1], CD[15:0], XRD, XWRL, XWRH, XBEL, XDACK, CLKIN				
H level input voltage	VIH2	CVDD=3.6V	2.2	-	-	V
L level input voltage	VIL2	CVDD=3.0	-	-	0.8	V
H level input voltage	VIH3	CVDD=1.95V	1.27	-	-	V
L level input voltage	VIL3	CVDD=1.65V	-	-	0.57	V
Schmitt input characteristics (USB FS)	Terminal names:	DP, DM				
H level trigger voltage	VT+ (USB)	HVDD = 3.6V	1.1	-	1.8	V
L level trigger voltage	VT- (USB)	HVDD = 3.0V	1.0	-	1.5	V
Hysteresis voltage	ΔV (USB)	HVDD= 3.0V	0.1	-	-	V
Input characteristics (USB FS differential)	Terminal names:	DP, DM pair				
Differential input sensitivity	VDS (USB)	HVDD = 3.0V Differential input voltage 0.8V to 2.5V	-	-	0.2	V
Input characteristics (VBUS)	Terminal names:	VBUS				
H level trigger voltage	VT+(VBUS)	HVDD = 3.6V	1.86	-	2.85	V
L level trigger voltage	VT- (VBUS)	HVDD = 3.0V	1.48	-	2.23	V
Hysteresis voltage	ΔV (VBUS)	HVDD= 3.0V	0.31	-	0.64	V
Input characteristics (Schmitt)	Terminal names:	VBUSFLG				
H level trigger voltage	VT1+	HVDD = 3.6V	1.4	-	2.7	V
L level trigger voltage	VT1-	HVDD = 3.0V	0.6	-	1.8	V
Hysteresis voltage	ΔV	HVDD= 3.0V	0.3	-	-	V
Input characteristics (Schmitt)	Terminal names:	XCS, XRESET				
H level trigger voltage	VT1+	CVDD=3.6V	1.4	-	2.7	V
L level trigger voltage	VT1-	CVDD=3.0V	0.6	-	1.8	V
Hysteresis voltage	ΔV1	CVDD=3.0V	0.3	-	-	V
H level trigger voltage	VT2+	CVDD=1.95V	0.6	-	1.4	V
L level trigger voltage	VT2-	CVDD=1.65V	0.3	-	1.1	V
Hysteresis voltage	ΔV2	CVDD=1.65V	0.2	-	-	V
Input characteristics	Terminal names:	VBUSFLG				
Pull-up resistor	RPLU2H	VI=VSS	50	100	240	kΩ
Input characteristics	Terminal names:	VBUS				
Pull-down resistor	RPLD3L	VI=5.0V	110	125	150	kΩ
Input characteristics	Terminal names:	ATPGEN, BURNIN				
Pull-down resistor	RPLD1L	VI=LVDD	24	60	150	kΩ
Input characteristics	Terminal names:	TESTEN				
Pull-down resistor	RPLD2L	VI=LVDD	48	120	300	kΩ

7.3.3 Output Characteristics

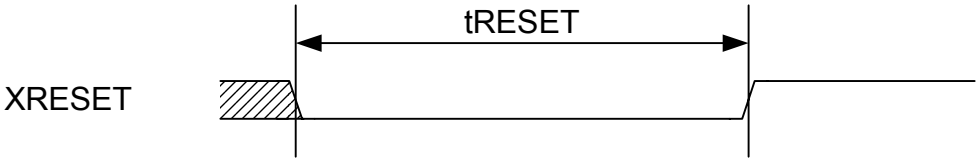
Item	Symbol	Condition	MIN	TYP	MAX	Units
Output characteristics	Terminal names: CD[15:0], XDREQ, XINT					
H level output voltage	VOH1	CVDD = 3.0V IOH = -2mA	CVDD-0.4	-	-	V
L level output voltage	VOL1	CVDD = 3.0V IOL = 2mA	-	-	VSS+0.4	V
H level output voltage	VOH2	CVDD = 1.65V IOH = -1mA	CVDD-0.4	-	-	V
L level output voltage	VOL2	CVDD = 1.65V IOL = 1mA	-	-	VSS+0.4	V
L level output voltage	VOL2(2)	CVDD = 1.65V IOL = 0.8mA	-	-	VSS+0.3	V
Output characteristics	Terminal names:VBUSEN					
H level output voltage	VOH4	HVDD = 3.0V IOH = -2mA	HVDD-0.4	-	-	V
L level output voltage	VOL4	HVDD = 3.0V IOL = 2mA	-	-	VSS+0.4	V
Output characteristics (USB FS)	Terminal names: DP, DM					
H level output voltage	VOH(USB)	HVDD=3.0V	2.8	-	-	V
L level output voltage	VOL(USB)	HVDD=3.6V	-	-	0.3	V
Output characteristics (USB HS)	Terminal names: DP, DM					
H level output voltage	VHSOH (USB)	HVDD = 3.0V	360	-	-	mV
L level output voltage	VHSOL (USB)	HVDD = 3.6V	-	-	10.0	mV
Output characteristics	Terminal names: CD[15:0], XINT					
OFF-STATE leakage current	IOZ	CVDD = 3.6V CVOH = CVDD VOL = VSS	-5	-	5	μA

7.3.4 Terminal Capacitance

Item	Symbol	Condition	MIN	TYP	MAX	Units
Terminal capacitance	Terminal name: All input terminals					
Input terminal capacitance	CI	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8	pF
Terminal capacitance	Terminal name: All output terminals					
Output terminal capacitance	CO	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8	pF
Terminal capacitance	Terminal name: All input/output terminals (except DP, DM)					
Input/output terminal capacitance 1	CIO1	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8	pF
Terminal capacitance	Terminal names: DP, DM					
Input/output terminal capacitance 2	CIO2	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	11	pF

7.4 AC Characteristics

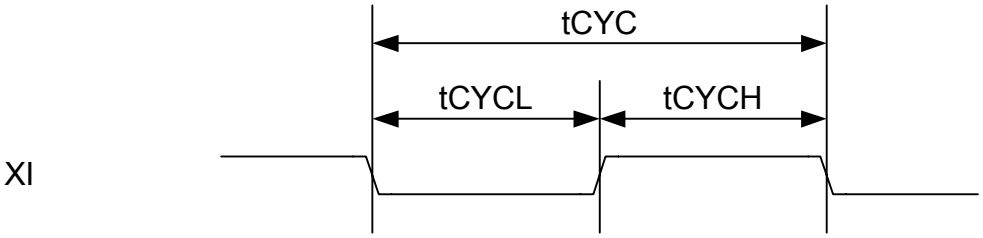
7.4.1 Reset Timing



Code	Description	min	typ	max	Units
tRESET	Reset pulse width	40	-	-	ns

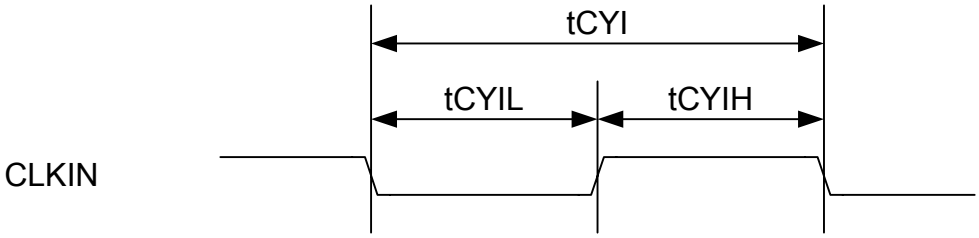
7.4.2 Clock Timing

<Internal oscillator>



Code	Description	min	typ	max	Units
tCYC	Clock cycle (ClkFreq=0b00)	11.9988	12	12.0012	MHz
tCYC	Clock cycle (ClkFreq=0b01)	23.9976	24	24.0024	MHz
tCYCH tCYCL	Clock duty	45	-	55	%

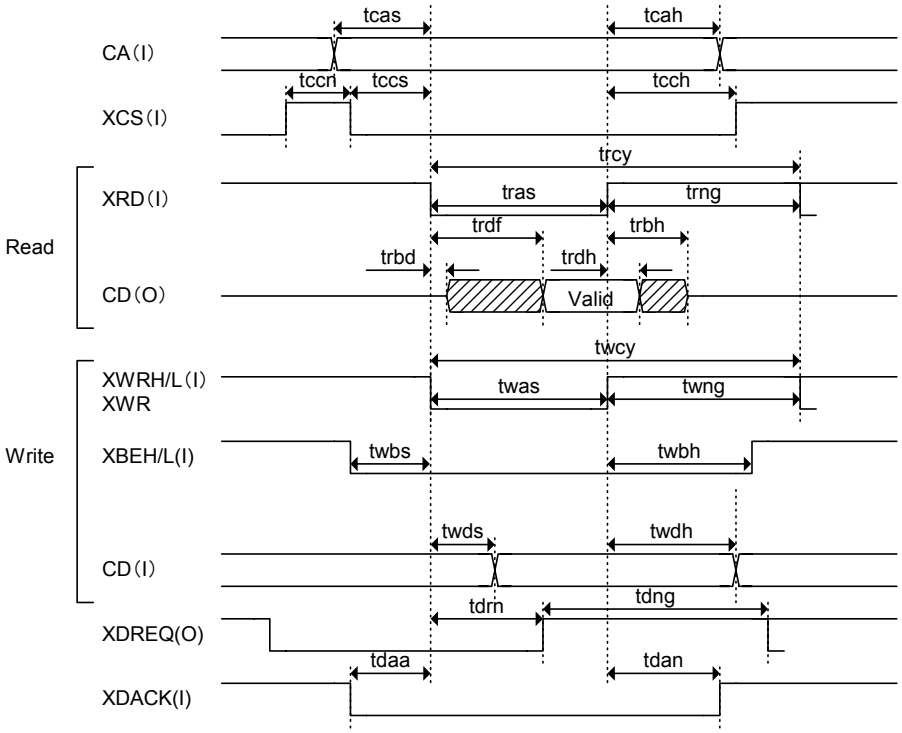
<External input>



Code	Description	min	typ	max	Units
tCYI	Clock cycle (ClkFreq=0b00)	11.9988	12	12.0012	MHz
tCYI	Clock cycle (ClkFreq=0b01)	23.9976	24	24.0024	MHz
tCYI	Clock cycle (ClkFreq=0b11)	47.9952	48	48.0048	MHz
tCYIH tCYIL	Clock duty	45	-	55	%

7.4.3 CPU/DMA I/F Access Timing

7.4.3.1 Specifications for CVDD = 1.65 V to 3.6 V

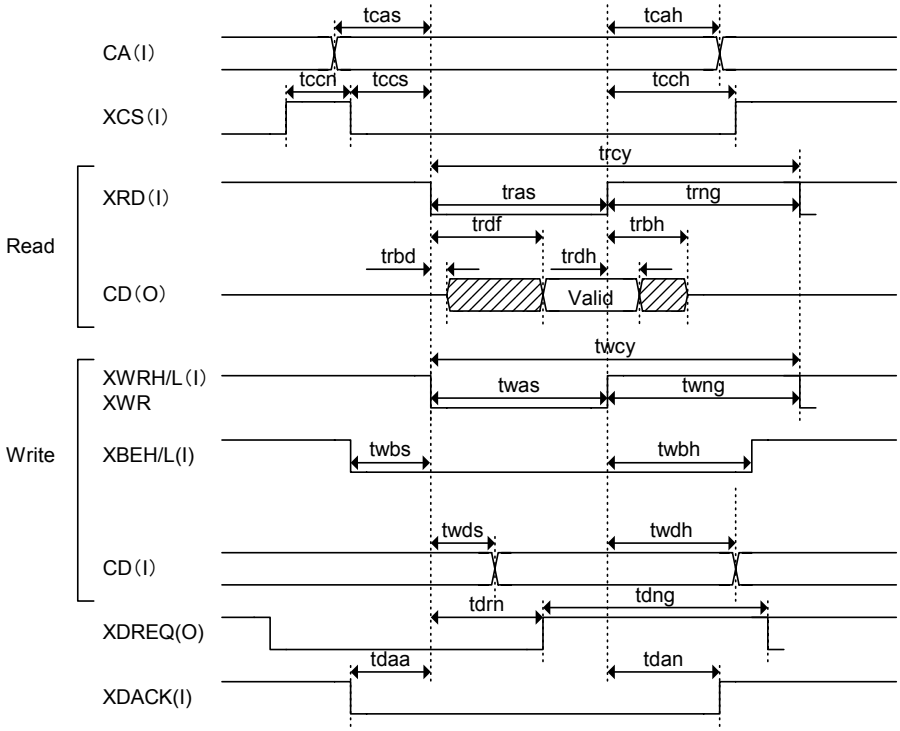


(CL=30pF)

Code	Item	min	typ	max	unit
tcas	Address setup time	6	-	-	ns
tcah	Address hold time	6	-	-	ns
tccs	XCS setup time	6	-	-	ns
tcch	XCS hold time	6	-	-	ns
tccn	XCS negate time (Only when CPUIF mode is set*)	15	-	-	ns
trcy	Read cycle	55	-	-	ns
tras	Read strobe assert time	35	-	-	ns
trng	Read strobe negate time	20	-	-	ns
trbd	Read data output start time	1	-	-	ns
trdf	Read data confirmation time	-	-	33	ns
trdh	Read data hold time	2	-	-	ns
trbh	Read data output delay time	-	-	6	ns
twcy	Write cycle	55	-	-	ns
twas	Write strobe assert time	35	-	-	ns
twng	Write strobe negate time	20	-	-	ns
twbs	Write byte enable setup time	6	-	-	ns
twbh	Write byte enable hold time	6	-	-	ns
twds	Write data delay acknowledge time	-	-	10	ns
twdh	Write data hold time (after strobe negation)	6	-	-	ns
tdrn	XDREQ negate delay time	-	-	35	ns
tdaa	XDACK setup time	6	-	-	ns
tdan	XDACK hold time	6	-	-	ns
tdng	XDREQ minimum negate time	Nn *16.6	-	-	ns

*Nn is determined by the DMA_EdgeMode.NegControl[3:0] setting. Nn = (NegControl + 3)

7.4.3.2 Specifications when limited to CVDD = 3.0 V to 3.6 V (relaxed specifications)



(C_L=30pF)

Code	Item	min	typ	max	unit
tcas	Address setup time	6	-	-	ns
tcah	Address hold time	6	-	-	ns
tccs	XCS setup time	6	-	-	ns
tcch	XCS hold time	6	-	-	ns
tccn	XCS negate time (Only when CPU IF mode is set*)	15	-	-	ns
trcy	Read cycle	55	-	-	ns
tras	Read strobe assert time	33	-	-	ns
trng	Read strobe negate time	20	-	-	ns
trbd	Read data output start time	1	-	-	ns
trdf	Read data confirmation time	-	-	30	ns
trdh	Read data hold time	2	-	-	ns
trbh	Read data output delay time	-	-	6	ns
twcy	Write cycle	55	-	-	ns
twas	Write strobe assert time	33	-	-	ns
twng	Write strobe negate time	20	-	-	ns
twbs	Write byte enable setup time	6	-	-	ns
twbh	Write byte enable hold time	6	-	-	ns
twds	Write data delay acknowledge time	-	-	10	ns
twdh	Write data hold time (after strobe negation)	6	-	-	ns
tdrn	XDREQ negate delay time	-	-	30	ns
tdaa	XDACK setup time	6	-	-	ns
tdan	XDACK hold time	6	-	-	ns
tdng	XDREQ minimum negate time	Nn *16.6	-	-	ns

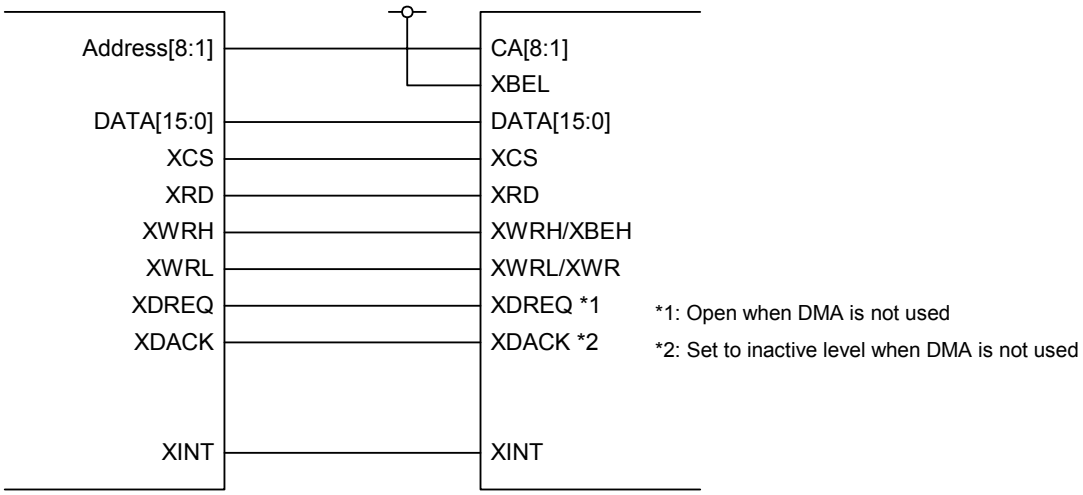
*Nn is determined by the DMA_EdgeMode.NegControl[3:0] setting. Nn = (NegControl + 3)

7.4.4 USB I/F Timing

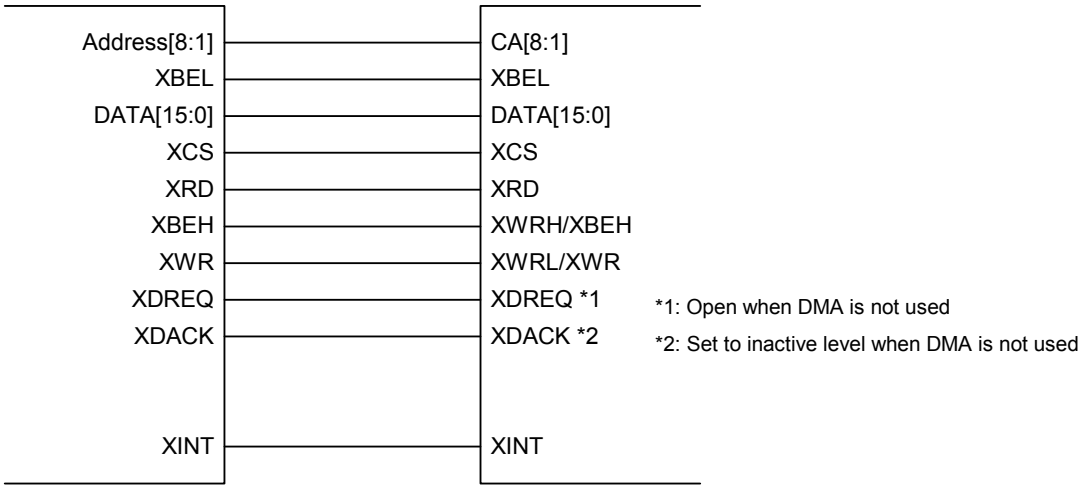
Complies with the USB 2.0 standard (Universal Serial Bus Specification Revision 2.0 Released on April 27, 2000).

8. Connection Examples

8.1 CPU I/F Connection Example



16-bit CPU (XWRH/XWRL) connection example



16-bit CPU (XBEH/XBEL) connection example

8.2 USB I/F Connection Example

Refer to the separately provided S1R72V Series USB 2.0 Hi-Speed PCB Design Guidelines.

9. Product Codes

Table 9-1 Product codes

Product code	Product type
S1R72V27B05****	PFBGA5UX60 package
S1R72V27B08****	PFBGA8UX81 package
S1R72V27F14****	QFP14-80 package

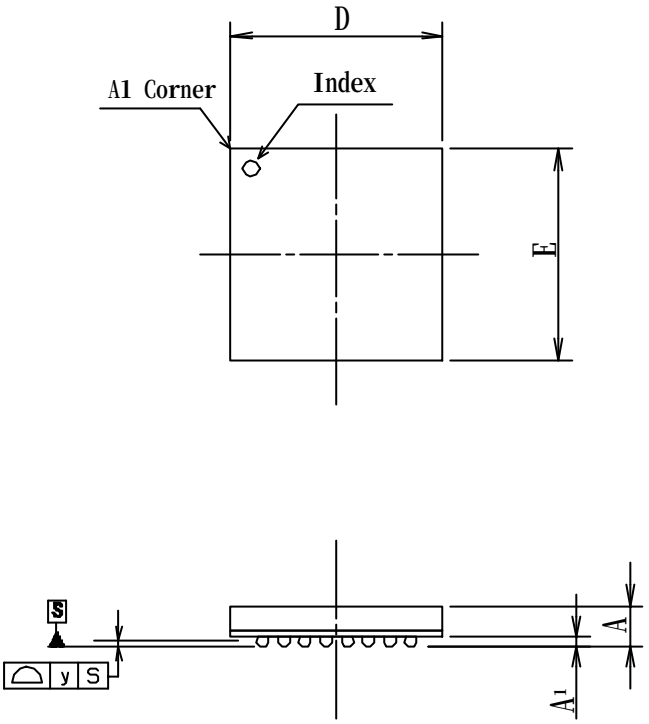
10. External Dimension Diagrams

Refer to the PFBGA5UX60, PFBGA8UX81 and QFP14-80 package drawings at the end of this document.

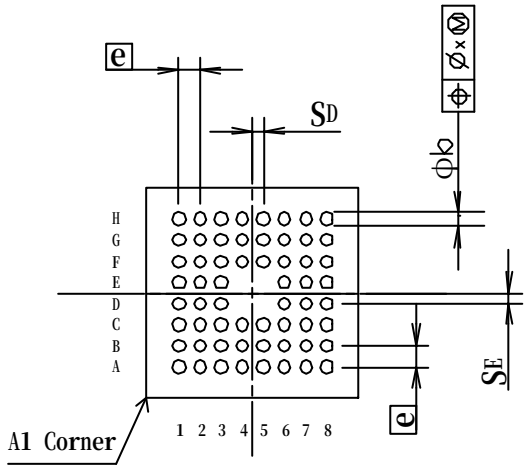
Revision History

Date	Revision details			
	Rev.	Page (old issue)	Type	Details
11/20/2007	1.0	All	New	Newly established

Top View



Bottom View

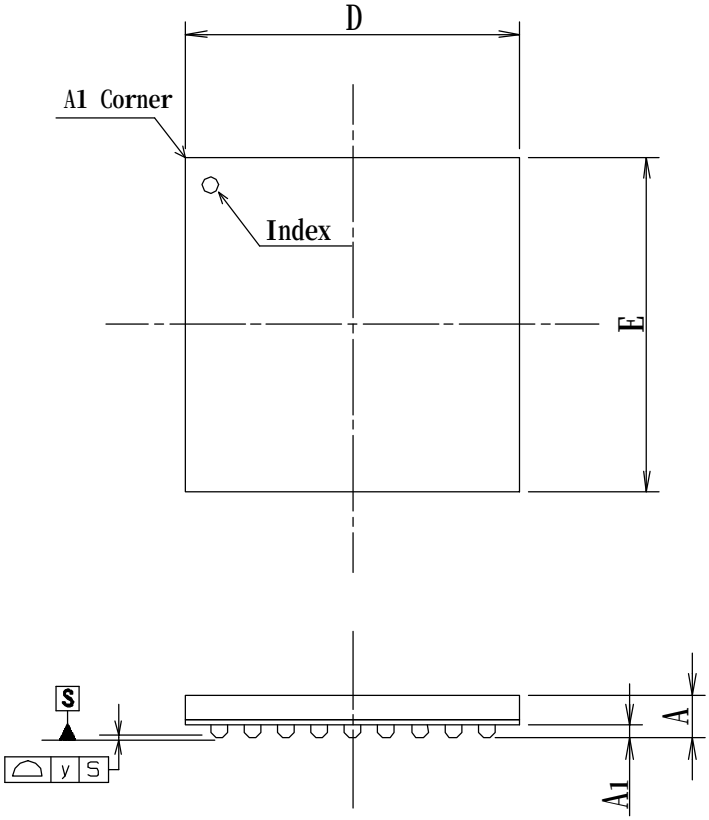


Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	5	-
E	-	5	-
A	-	-	1.2
A1	-	0.23	-
e	-	0.5	-
b	0.26	-	0.36
X	-	-	0.08
Y	-	-	0.1
SD	-	0.25	-
SE	-	0.25	-

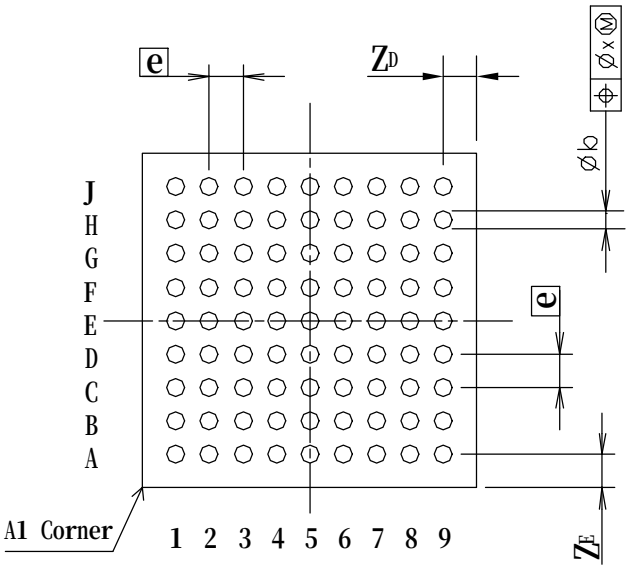
1 = 1mm

1.0	2005.03.01	C. SHOJI	M. SONE	T. OTSUKI	-
REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
TITLE	P-TFBGA-060-0505-0.50(PFBGA5U-60)				-
					CAD FILE -
SEIKO EPSON CORP.					DWG No. 4900-0394
					SCALE Free SHEET 1 of 1

Top View



Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	8	-
E	-	8	-
A	-	-	1.2
A_1	-	0.3	-
e	-	0.8	-
b	0.38	-	0.48
x	-	-	0.08
y	-	-	0.1
Z_D	-	0.8	-
Z_E	-	0.8	-

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
2.0	2004.10.19	C. SHOJI	M. SONE	T. OTSUKI	—

TITLE: P-TFBGA-081-0808-0.80(PFBGA8U-81)

CAD FILE: —

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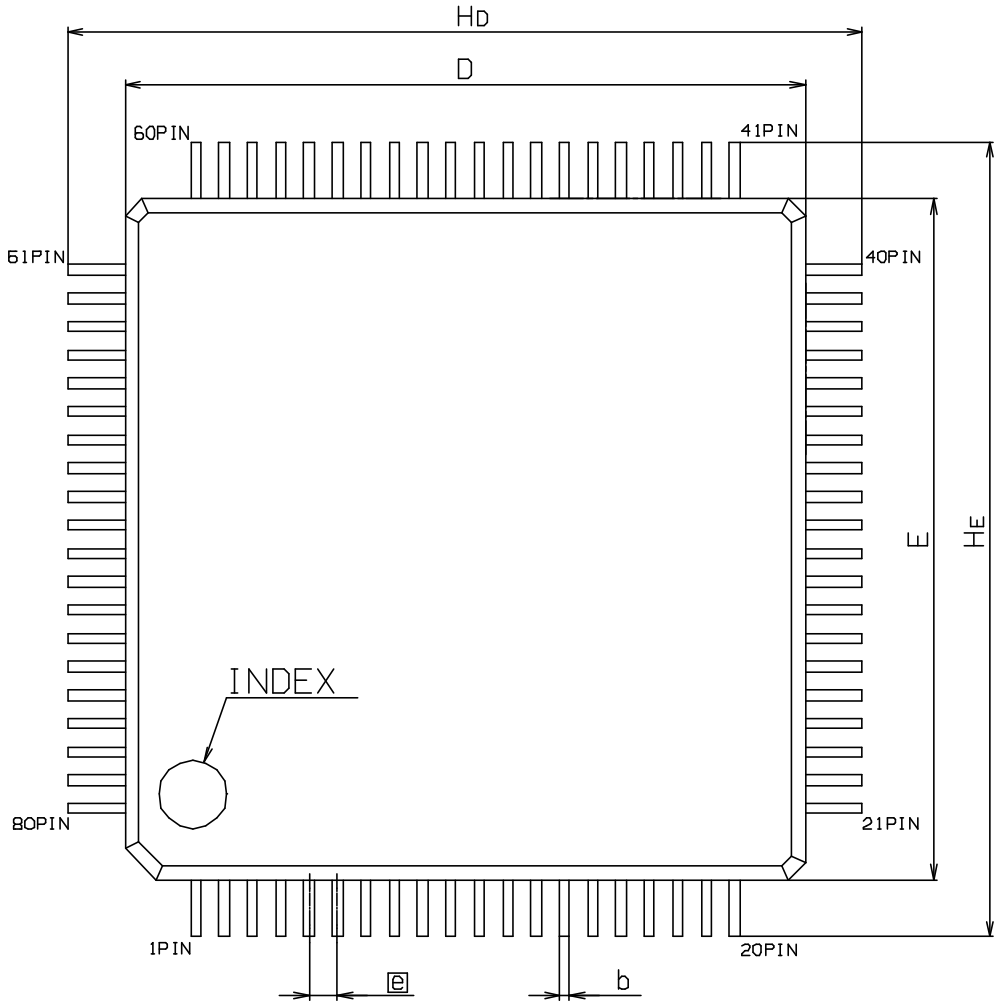
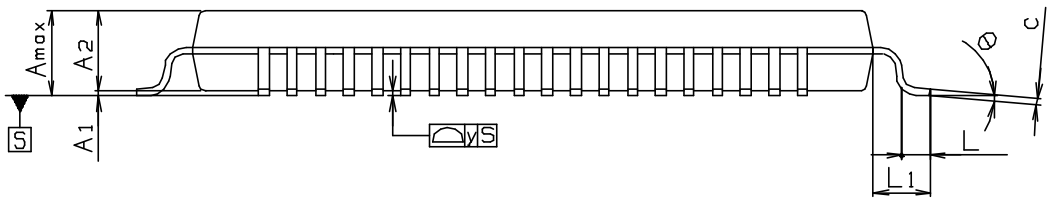
SCALE: Free SHEET: 1 of 1





Symbol	Dimension in Millimters		
	Min	Nom	Max
E	-	12	-
D	-	12	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L_1	-	1	-
H_E	-	14	-
H_D	-	14	-
y	-	-	0.08

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
2.0	2004.08.03	C.SAITO	M.SONE	T.OTSUKI	-

TITLE: P-LQFP080-1212-0.50(QFP14-80PIN)

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