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NTE2107
Integrated Circuit
NMOS, 4K Dynamic RAM (DRAM)

Description:

The NTE2107 is a 4096 word by 1 bit dynamic random access memory (RAM) that incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the primary criteria.

The NTE2107 must be refreshed every 2ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0 – A5). The chip select input can be either high or low for refresh.

This device has been designed with minimum production costs as a prime criterion. It is fabricated using N–channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The NTE2107 uses a single transistor cell to minimize the device area. The single cell, along with unique design features in the on–chip peripheral circuits, yeilds a high performance memory device.

Features:

- Organization: 4096 x 1
- Access Time: 200ns Min
- Cycle Time: 400ns Min
- Easy System Interface:
  - One High Voltage Input – Chip Enable
  - TTL Compatible – All Other Inputs and Outputs
- Address Registers On–Chip
- Simple Read–Modify–Write Operation
- Industry Standard Pin Configuration

Absolute Maximum Ratings: (Note 1)

All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB} . . . . –0.3 to +25V
Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . –0.3 to +20V
Power Dissipation, P_D 1.25W
Operating Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Recommended Operating Conditions:

Parameter	Min	Typ	Max	Unit
V_{DD} Voltage	10.8	–	13.2	V
V_{CC} Voltage	4.5	–	5.5	V
V_{BB} Voltage	–5.5	–	–4.5	V
Operating Temperature Range	0	–	70	°C

Electrical Characteristics: (Note 2, T_A = 0° to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{SS} = 0V, V_{BB} (Note 3) = −5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Load Current	I_{LI}	V_{IN} = 0V to V_{IN}max, (All Inputs Except CE)	–	0.01	10	µA
	I_{LC}	V_{IN} = 0V to V_{IHC}max	–	0.01	10	µA
Output Leakage Current Up for High Impedance State	$\|I_{LO}\|$	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V	–	0.01	10	µA
V_{DD} Supply Current During CE "OFF"	I_{DD1}	CE = −1V to +6V, Note 4	–	110	300	µA
V_{DD} Supply Current During CE "ON"	I_{DD2}	CE = V_{IHC}, T_A = +25°C	–	20	40	mA
Average V_{DD} Current	$I_{DD\ AV1}$	Cycle Time = 400ns, t_{ce} = 230ns, T_A = +25°C	–	35	60	mA
	$I_{DD\ AV2}$	Cycle Time = 1000ns, t_{ce} = 230ns, T_A = +25°C	–	15	30	mA
V_{CC} Supply Current During CE "OFF"	I_{CC1}	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, Note 5	–	0.01	10	µA
V_{BB} Supply Current Average	I_{BB}		–	5	100	µA
Input Low Voltage	V_{IL}	t_T = 20ns	−1.0	–	0.6	V
Input High Voltage	V_{IH}		2.4	–	V_{CC}+1	V
CE Input Low Voltage	V_{ILC}		−1.0	–	1.0	V
CE Input High Voltage	V_{IHC}		V_{DD}−1	–	V_{DD}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0.0	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −2mA	2.4	–	V_{CC}	V

Note 2., Typical values are for T_A = +25°C and nominal power supply voltages.

Note 3. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 4. The I_{DD} and I_{CC} current flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5. During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics: (T_A = 0° to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = −5V ±10% unless otherwise specified)

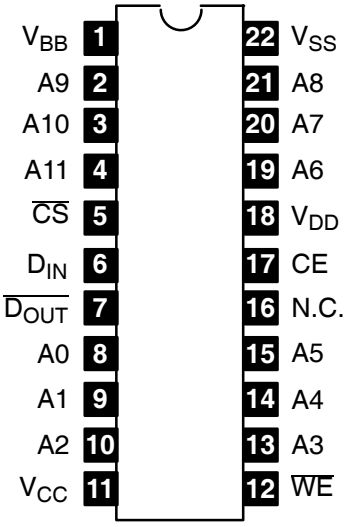
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read, Write, Read/Modify/Write, and Refresh Cycle						
Time Between Refresh	t_{REF}		–	–	2	ms
Address to CE Set–Up Time	t_{AC}	t_{AC} is Measured From End of Address Transition	0	–	–	ns
Address Hold Time	t_{AH}		50	–	–	ns
CE "OFF" Time	t_{CC}		130	–	–	ns
CE Transition Time	t_T		10	–	40	ns
CE "OFF" to Output High Impedance State	t_{CF}		0	–	–	ns
Read Cycle						
Cycle Time	t_{CY}	C_{LOAD} = 50pF, Load = 1 TTL Gate, Ref = 2V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	400	–	–	ns
CE "ON" Time	t_{CE}		230	–	3000	ns
CE Output Delay	t_{CO}		–	–	180	ns
Address to Output Access	t_{ACC}		–	–	200	ns
CE to $\overline{WE}$	t_{WL}		0	–	–	ns
$\overline{WE}$ to CE "ON"	t_{WC}		0	–	–	ns

AC Electrical Characteristics (Cont'd): (T_A = 0° to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = –5V ±10% unless otherwise specified)

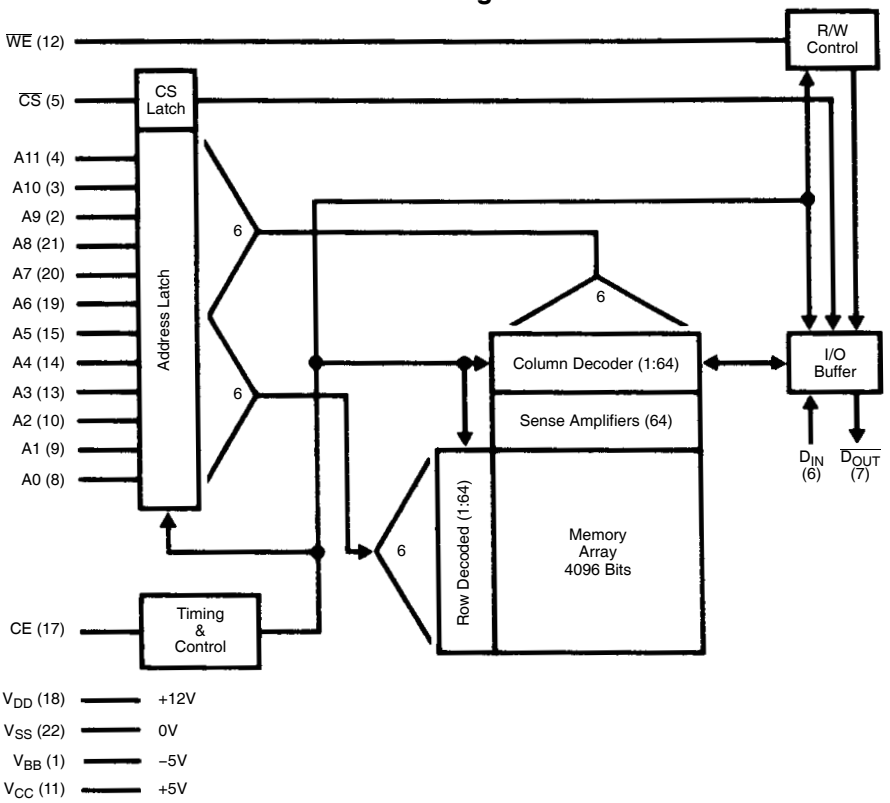
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Write Cycle						
Cycle Time	t_{CY}		400	–	–	ns
CE "ON" Time	t_{CE}		230	–	3000	ns
$\overline{WE}$ to CE "OFF"	t_W		150	–	–	ns
CE to $\overline{WE}$	t_{CW}	t_T = 20ns	100	–	–	ns
D_{IN} to CE Set–Up	t_D		150	–	–	ns
D_{IN} Hold Time	t_{DH}		0	–	–	ns
$\overline{WE}$ Pulse Width	t_{WP}		50	–	–	ns
Read/Modify/Write Cycle						
Read Modify Write (RMW) Cycle Time	t_{RWC}	t_t = 20ns, C_{LOAD} = 50pF, Load = 1 TTL Gate, Ref = 2V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	520	–	–	ns
CE Width During RMW	t_{CRW}		350	–	3000	ns
$\overline{WE}$ to CE "ON"	t_{WC}		0	–	–	ns
$\overline{WE}$ to CE "OFF"	t_W		150	–	–	ns
$\overline{WE}$ Pulse Width	t_{WP}		50	–	–	ns
D_{IN} to CD Set–Up	t_D		150	–	–	ns
D_{IN} Hold Time	t_{DH}		0	–	–	ns
CE to Output Delay	t_{CO}		–	–	180	ns
$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid	t_{WD}		0	–	–	ns
Access Time	t_{ACC}		–	–	200	ns
Capacitance (T_A = +25°C, Note 6)						
Address capacitance, $\overline{CS}$	C_{AD}	$V_{IN} = V_{SS}$	–	2	–	pF
CE Capacitance	C_{CE}	$V_{IN} = V_{SS}$	–	15	–	pF
Data Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	5	–	pF
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}	$V_{IN} = V_{SS}$	–	4	–	pF

Note 6. Capacitance measured with Boonton Meter of effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20mA.

Pin Connection Diagram



Block Diagram



Memory Inverts From Data In to Data Out