# Low Skew, 1-to-4, LVCMOS/LVTTL-to-LVDS Fanout Buffer

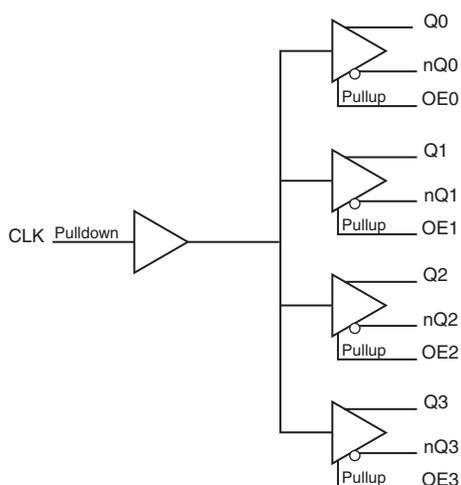# ICS854105I

## General Description

The ICS854105I is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS), the ICS854105I provides a low power, low noise solution for distributing clock signals over controlled impedances of 100Ω. The ICS854105I accepts an LVCMOS/LVTTL input level and translates it to LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS854105I ideal for those applications demanding well defined performance and repeatability.

## Features

- Four differential LVDS output pairs
- One single-ended LVCMOS/LVTTL input
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Translates single-ended input signals to LVDS levels
- Additive phase jitter, RMS: 0.16ps (typical)
- Output skew: 72ps (maximum)
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 1.75ns (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



**ICS854105I**

**16-Lead TSSOP**
**4.4mm x 5.0mm x 0.925mm package body**
**G Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | OE0 | Input | Pullup | Output enable pin for Q0, nQ0 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 2 | OE1 | Input | Pullup | Output enable pin for Q1, nQ1 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 3 | OE2 | Input | Pullup | Output enable pin for Q2, nQ2 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 4 | $V_{DD}$ | Power | | Positive supply pin. |
| 5 | GND | Power | | Power supply ground. |
| 6 | CLK | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 7 | nc | Unused | | No connect. |
| 8 | OE3 | Input | Pullup | Output enable pin for Q3, nQ3 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 9, 10 | nQ3, Q3 | Output | | Differential output pair. LVDS interface levels. |
| 11, 12 | nQ2, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 13, 14 | nQ1, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 15, 16 | nQ0, Q0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | k$\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k$\Omega$ |

## Function Table

### Table 3. Output Enable Function Table

| Inputs | Outputs |
|---|---|
| OE[3:0] | Q[3:0], nQ[3:0] |
| 0 | High-Impedance |
| 1 | Active (default) |

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (LVDS)<br>Continuos Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 100.3°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 75 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK | $V_{DD} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | OE[3:0] | $V_{DD} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | OE[3:0] | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4C. LVDS DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.15 | 1.3 | 1.5 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

**Table 5. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | 0.9 | | 1.75 | ns |
| $f_{jit}$ | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: (12kHz – 20MHz) | | 0.16 | | ps |
| $tsk$(o) | Output Skew; NOTE 2, 4 | | | | 72 | ps |
| $tsk$(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 350 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 115 | | 715 | ps |
| odc | Output Duty Cycle | $f \leq$ 100MHz | 45 | | 55 | % |
| | | 100 < $f \leq$ 200MHz | 40 | | 60 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at $f_{MAX}$ unless noted otherwise.

NOTE 1: Measured from $V_{DD}$/2 of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing point.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of input on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

# Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Top -60 dBc/Hz

**Additive Phase Jitter @ 155.52MHz
12kHz to 20MHz = 0.16ps (typical)**
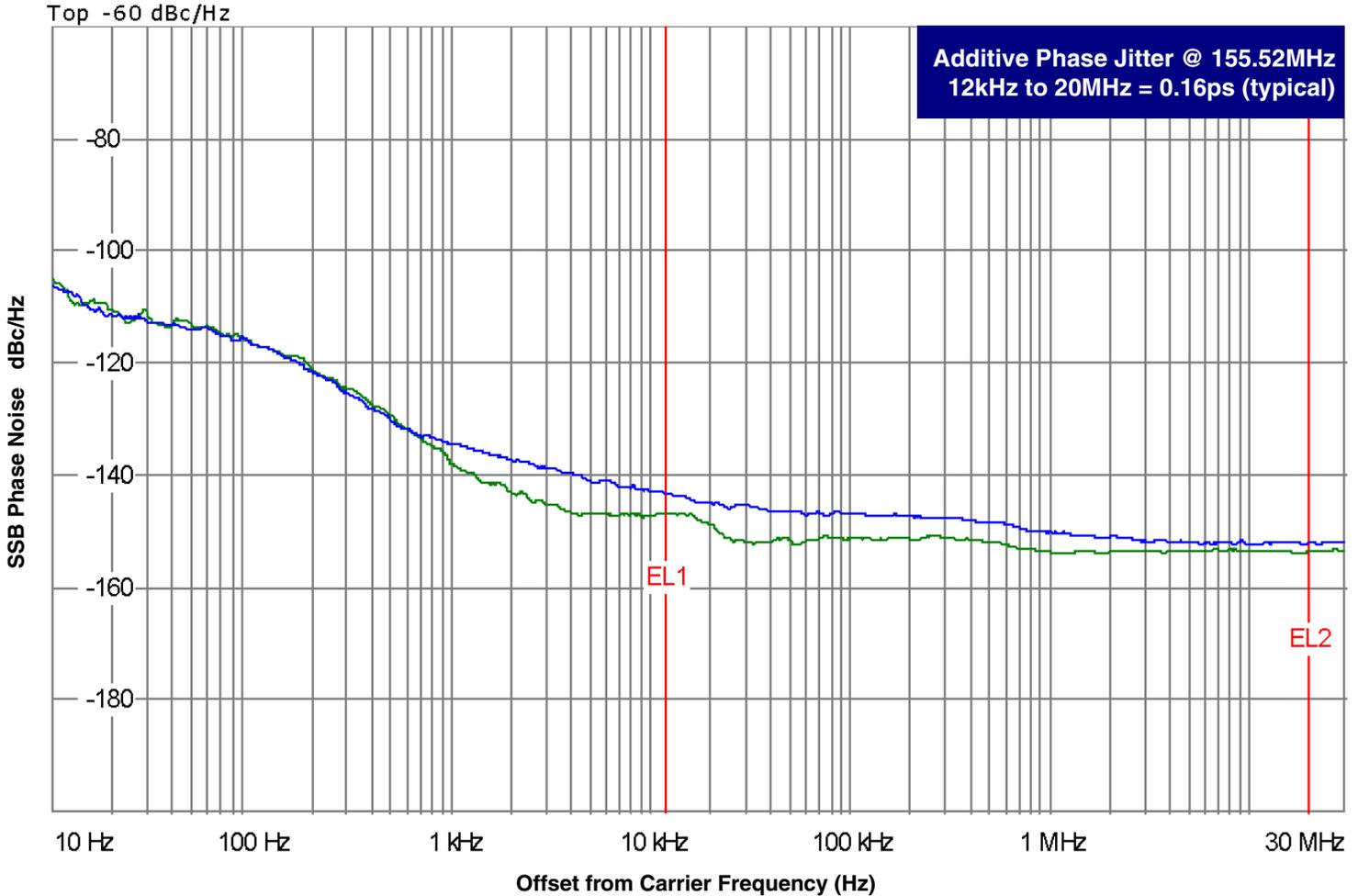


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "Rohde & Schwarz SMA100 Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".
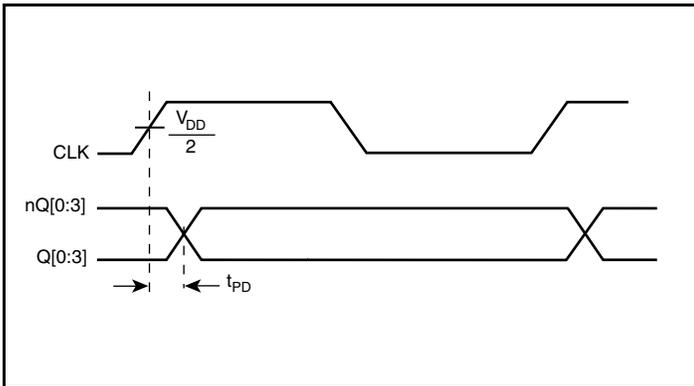
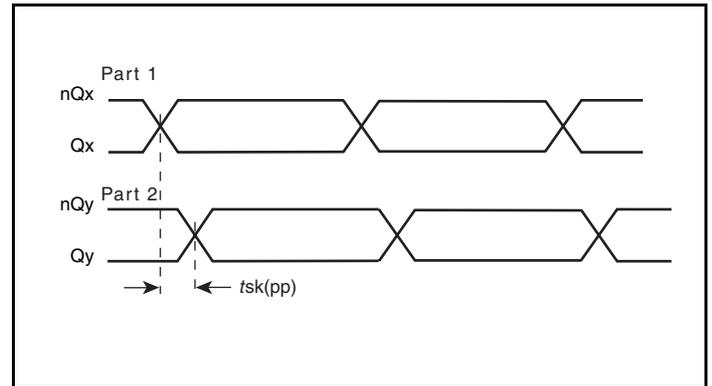# Parameter Measurement Information
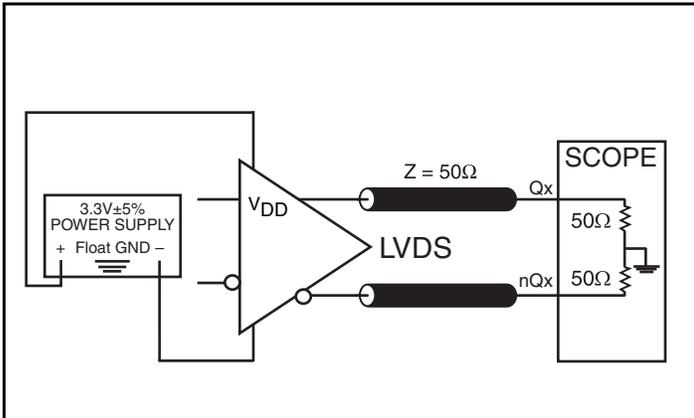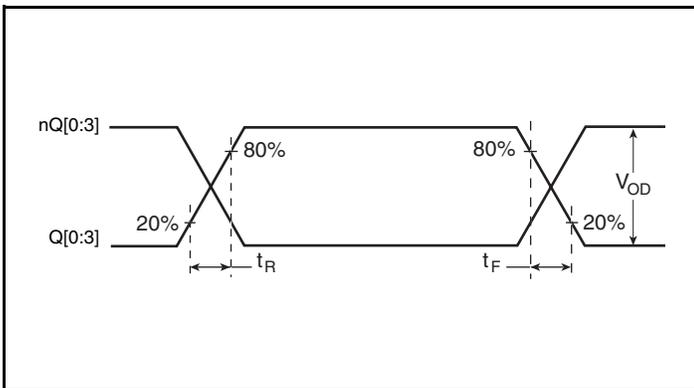


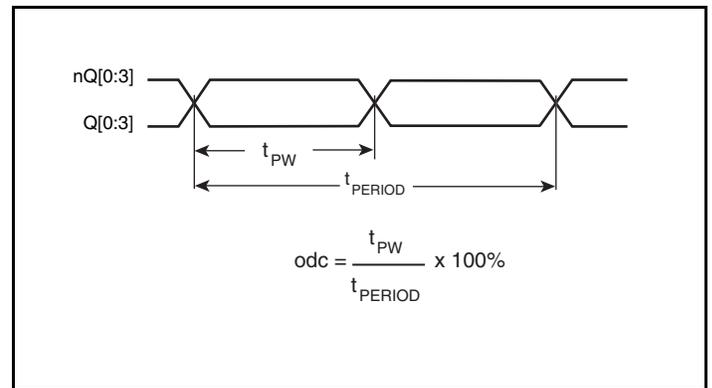**3.3V LVDS Output Load AC Test Circuit**
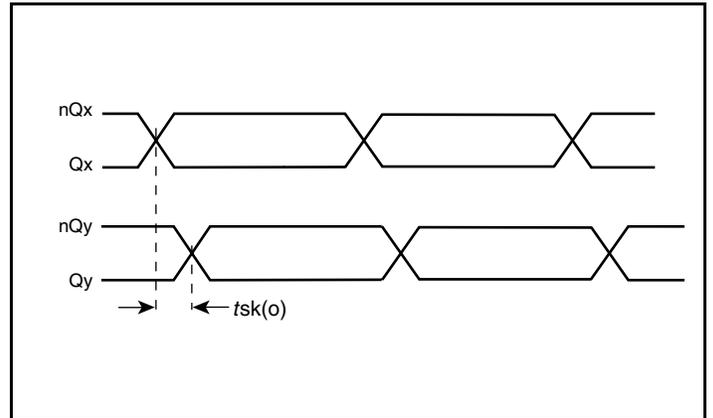


**Output Skew**



**Propagation Delay**



**Part-to-Part Skew**



**Output Rise/Fall Time**
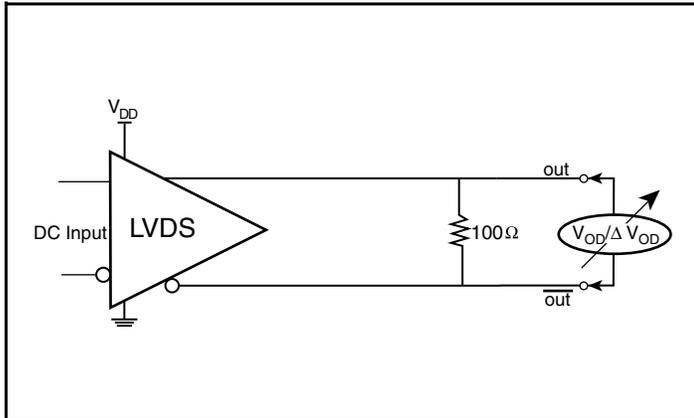


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

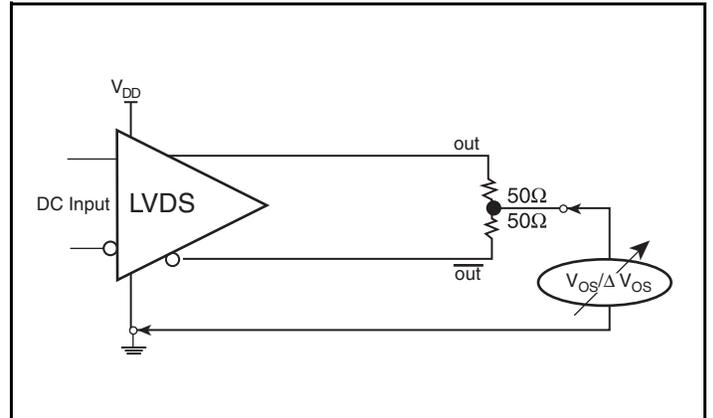**Output Duty Cycle/Pulse Width/Period**

# Parameter Measurement Information, continued



**Differential Output Voltage Setup**



**Offset Voltage Setup**

# Application Information

## Recommendations for Unused Input and Output Pins

### Inputs:

**LVCMOS Control Pins**

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

**LVDS Outputs**

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## 3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 1.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.
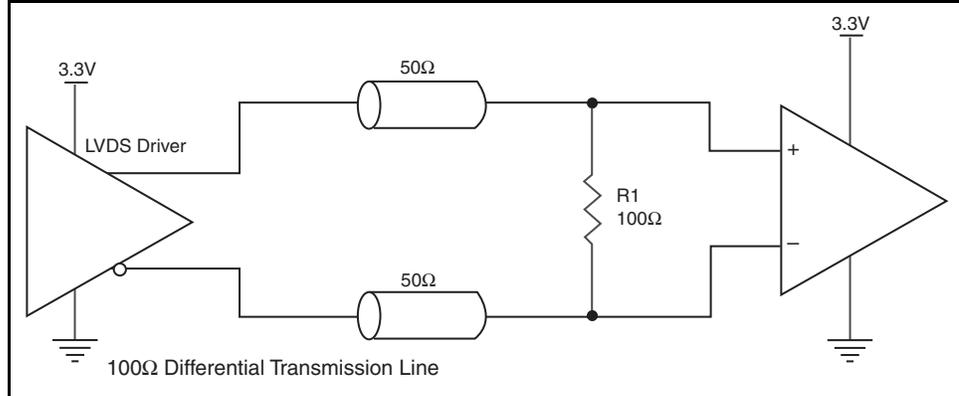


**Figure 1. Typical LVDS Driver Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854105I.
Equations and example calculations are also provided.

### 1.  Power Dissipation.

The total power dissipation for the ICS854105I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * $I_{DD\_MAX}$ = 3.465V * 75mA = **259.875mW**

### 2.  Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.260W * 100.3°C/W = 111.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

## Table 6. Thermal Resistance $\theta_{JA}$ for 16 Lead TSSOP, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

# Reliability Information

**Table 7. θ$_{JA}$ vs. Air Flow Table for a 16 Lead TSSOP**

| θ$_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

# Transistor Count

The transistor count for ICS854105I is: 286

# Package Outline and Package Dimensions
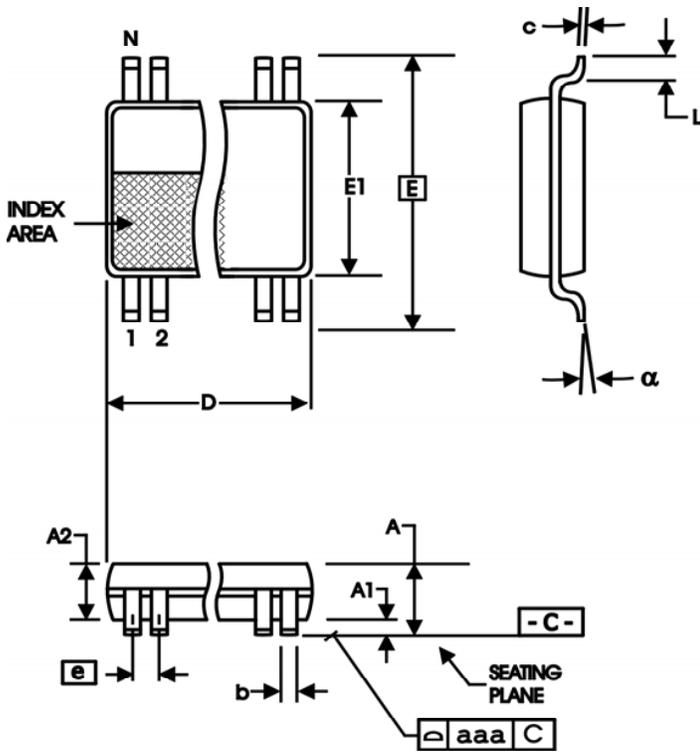
**Package Outline - G Suffix for 16 Lead TSSOP**



**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 16 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 4.90 | 5.10 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| **α** | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

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# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 854105AGILF | 54105AIL | "Lead-Free" 16 Lead TSSOP | Tube | -40°C to 85°C |
| 854105AGILFT | 54105AIL | "Lead-Free" 16 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support**
netcom@idt.com
+480-763-2056