ALD810023/ALD810024/ALD810025/
ALD810026/ALD810027/ALD810028

QUAD SUPERCAPACITOR AUTO BALANCING (SAB™) MOSFET ARRAY

GENERAL DESCRIPTION

The ALD8100xx and ALD9100xx family of Supercapacitor Auto Balancing MOSFETs, or SAB™ MOSFETs, are EPAD® MOSFETs designed to address leakage balance of supercapacitors connected in series. Supercapacitors, also known as ultracapacitors or supercaps, when connected two in series, can be balanced with an ALD9100xx dual package. Supercaps connected two, three or four in series can be balanced with an ALD8100xx quad package.

ALD SAB MOSFETs have unique electrical characteristics for active continuous leakage current regulation and self-balancing of stacked series-connected supercaps and, at the same time, dissipate near zero leakage currents, practically eliminating extra power dissipation. For many applications, SAB MOSFET automatic charge balancing offers a simple, economical and effective method to balance and regulate supercap voltages. With SAB MOSFETs, each supercap in a series-connected stack is continuously and automatically controlled for precision effective supercap leakage current and voltage balancing.

SAB MOSFETs offer a superior alternative solution to other passive resistor-based or operational amplifier based balancing schemes, which typically contribute continuous power dissipation due to linear currents at all voltage levels. They are also a preferred alternative to many other active supercap charging and balancing regulator ICs where tradeoffs in cost, efficiency, complexity and power dissipation are important design considerations.

The SAB MOSFET provides regulation of the voltage across a supercap cell by increasing its drain current exponentially across the supercap when supercap voltages increase, and by decreasing its drain current exponentially across the supercap when supercap voltages decrease. When a supercap in a supercap stack is charged to a voltage less than 90% of the desired voltage limit, the SAB MOSFET across the supercap is turned off and there is zero leakage current contribution from the SAB MOSFET. On the other hand, when the voltage across the supercap is over the desired voltage limit, the SAB MOSFET is turned on to increase its drain currents to keep the over-voltage from rising across the supercap. However, the voltages and leakages of other supercaps in the stack are lowered simultaneously to maintain near-zero net leakage currents.

The ALD8100xx/ALD9100xx SAB MOSFET family offers the user a selection of different threshold voltages for various supercap nominal voltage values and desired leakage balancing characteristics. Each SAB MOSFET generally requires connecting its V+ pin to the most positive voltage and its V- and IC pins to the most negative voltage within the package. Note that each Drain pin has an internal reverse biased diode to its Source pin, and each Gate pin has a reverse biased diode to V-. All other pins must have voltages within V+ and V- voltage limits. Standard ESD protection facilities and handling procedures for static sensitive devices must also be used.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range* 0°C to +70°C	
16-Pin SOIC Package	
ALD810023SCL	ALD810026SCL
ALD810024SCL	ALD810027SCL
ALD810025SCL	ALD810026SCL

* Contact factory for industrial temp. range or user-specified threshold voltage values.

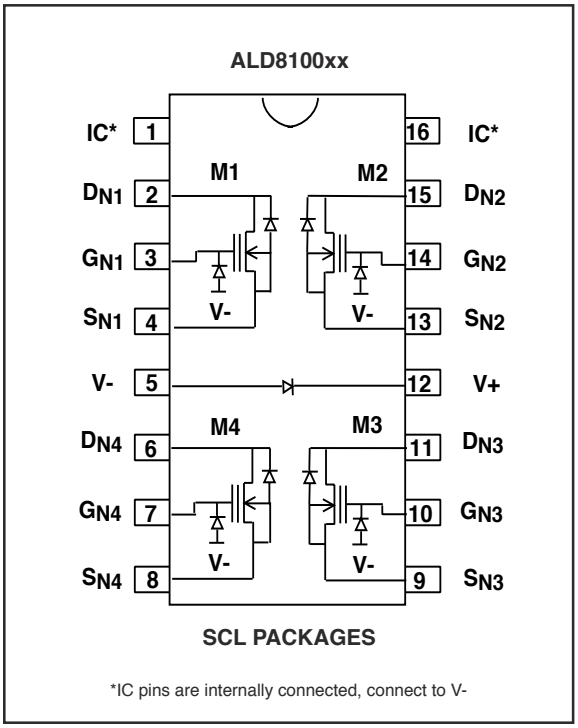
FEATURES & BENEFITS

- Simple and economical to use
- Precision factory trimmed
- Automatically regulates and balances leakage currents
- Effective for supercapacitor charge-balancing
- Balances up to 4 supercaps with a single IC package
- Balances 2-cell, 3-cell, 4-cell series-connected supercaps
- Scalable to larger supercap stacks and arrays
- Near zero additional leakage currents
- Zero leakage at 0.3V below rated voltages
- Balances with series-connect and parallel-connect
- Leakage currents are exponential fuction of cell voltages
- Active current ranges from < 0.3nA to > 1000μA
- Always active, always fast response time
- Minimizes leakage currents and power dissipation

APPLICATIONS

- Series-connected supercapacitor cell leakage balancing
- Energy harvesting
- Zero-power voltage divider at selected voltages
- Matched current mirrors and current sources
- Zero-power mode maximum voltage limiter
- Scaled supercapacitor stacks and arrays

PIN CONFIGURATION

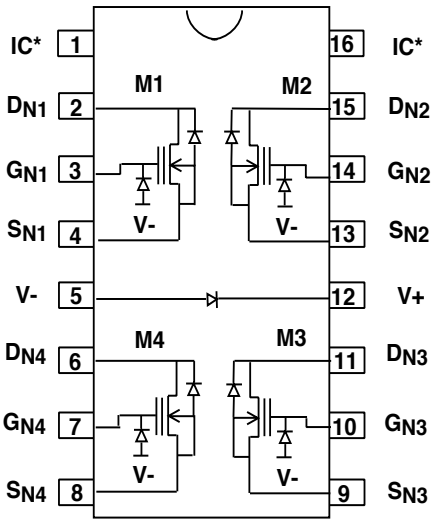


SCL PACKAGES

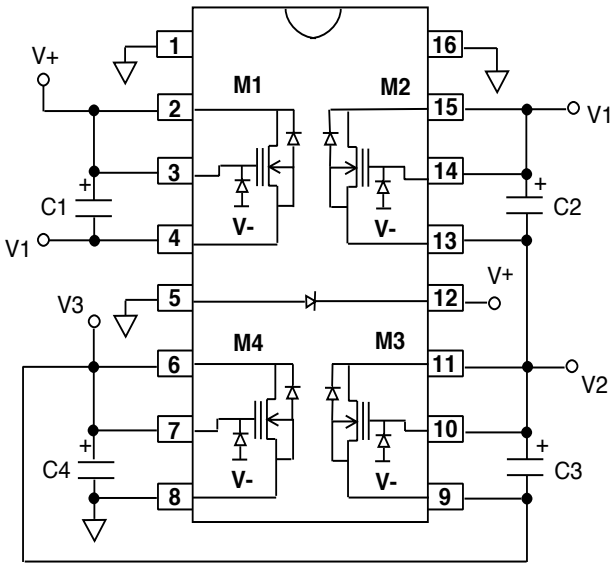
*IC pins are internally connected, connect to V-

TYPICAL APPLICATIONS

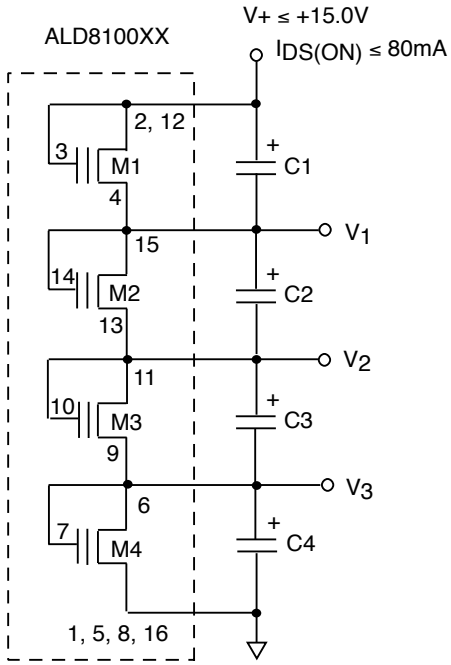
ALD8100xx PIN DIAGRAM



TYPICAL CONNECTION FOR A FOUR-SUPERCAP STACK

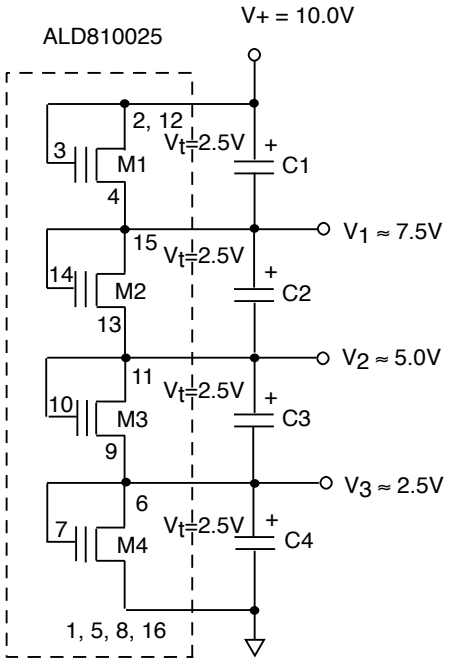


SCHEMATIC DIAGRAM OF A TYPICAL CONNECTION FOR A FOUR-SUPERCAP STACK



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C4 DENOTES SUPERCAPACITORS

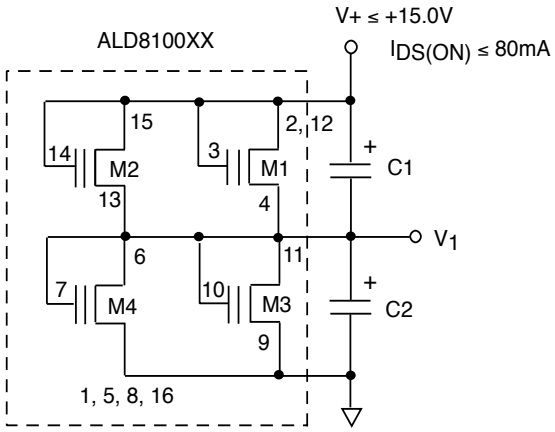
EXAMPLE OF ALD810025 CONNECTION ACROSS FOUR SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C4 DENOTES SUPERCAPACITORS

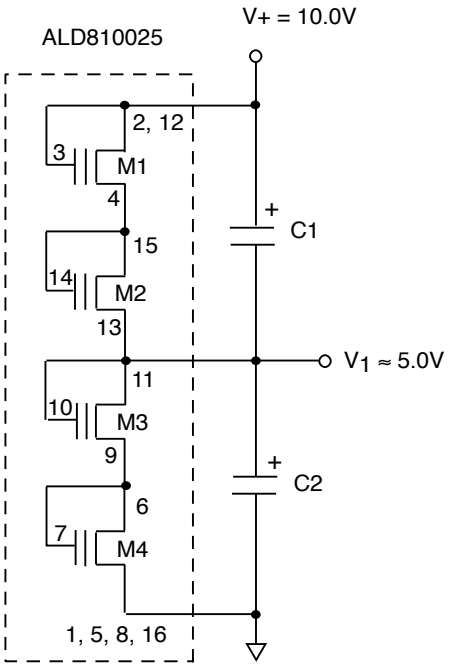
TYPICAL APPLICATIONS (cont.)

TYPICAL PARALLEL CONNECTION OF SAB MOSFETS WITH TWO SUPERCAPS



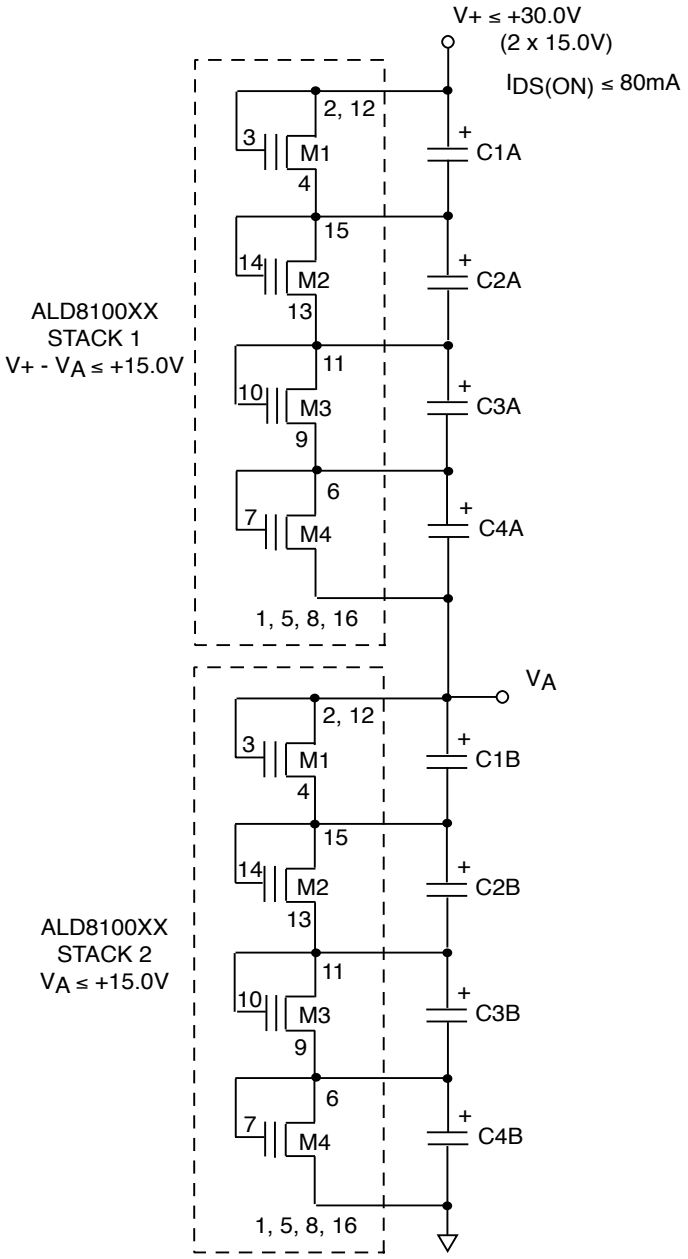
1-16 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

EXAMPLE OF ALD810025 CONNECTION ACROSS TWO SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

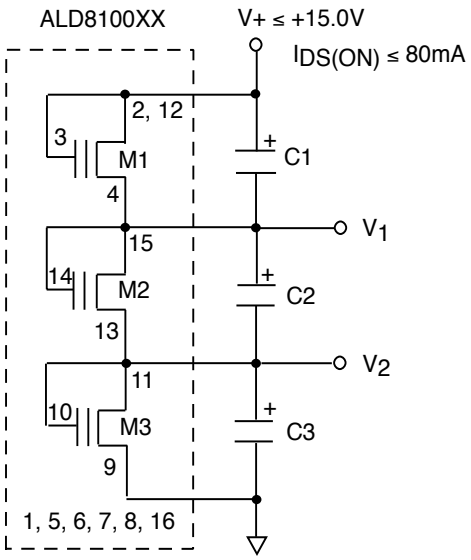
SERIES CONNECTION OF TWO FOUR-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE



1-16 DENOTES PACKAGE PIN NUMBERS
C1A-C4B DENOTES SUPERCAPACITORS

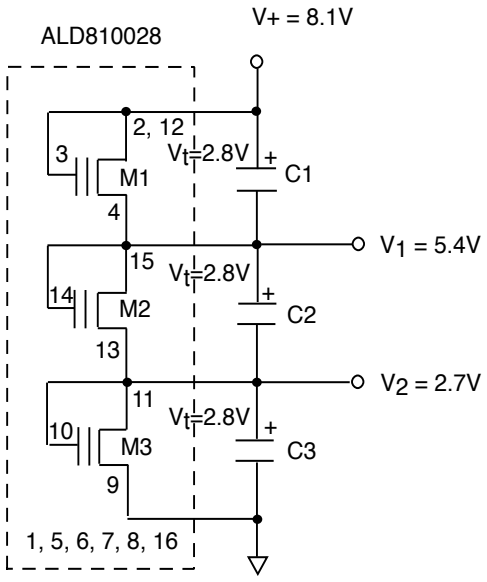
TYPICAL APPLICATIONS (cont.)

TYPICAL SERIES CONNECTION OF SAB MOSFETS WITH THREE SUPERCAPS



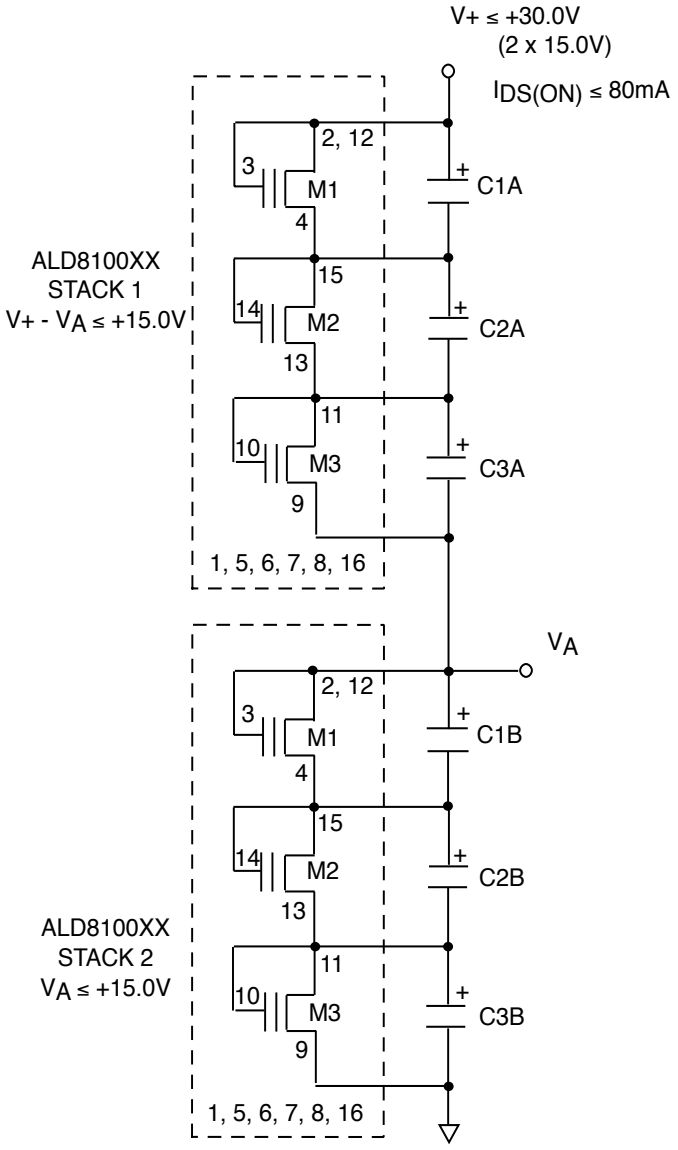
1-16 DENOTES PACKAGE PIN NUMBERS
C1-C3 DENOTES SUPERCAPACITORS

EXAMPLE OF ALD810028 CONNECTION ACROSS THREE SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C3 DENOTES SUPERCAPACITORS

SERIES CONNECTION OF TWO THREE-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE



1-16 DENOTES PACKAGE PIN NUMBERS
C1A-C3B DENOTES SUPERCAPACITORS

TABLE 1. SUPERCAP AUTO BALANCING (SAB™) MOSFET EQUIVALENT ON RESISTANCE AT DIFFERENT DRAIN-GATE SOURCE VOLTAGES AND DRAIN-SOURCE ON CURRENTS

ALD Part Number	Gate-Threshold Voltage V_t (V)	Drain-Gate Source Voltage (V)[2] Equivalent ON Resistance (MΩ)	SAB MOSFET DRAIN-SOURCE ON CURRENT $I_{DS(ON)}$ (μA)[1] T_A = 25°C										
			0.0001	0.001	0.01	0.1	1	10	100	300	1000	3000	10000
ALD910028	2.80	$V_{GS} = V_{DS}$ (V)	2.4	2.5	2.6	2.7	2.8	2.9	3.02	3.1	3.24	3.3	3.8
		$R_{DS(ON)}$ (MΩ)	24000	2500	260	27	2.8	0.29	0.030	0.01	0.003	0.001	0.0004
ALD910027	2.70	$V_{GS} = V_{DS}$ (V)	2.3	2.4	2.5	2.6	2.7	2.8	2.92	3.0	3.14	3.2	3.7
		$R_{DS(ON)}$ (MΩ)	23000	2400	250	26	2.7	0.28	0.029	0.01	0.003	0.001	0.0004
ALD910026	2.60	$V_{GS} = V_{DS}$ (V)	2.2	2.3	2.4	2.5	2.6	2.7	2.82	2.9	3.04	3.1	3.6
		$R_{DS(ON)}$ (MΩ)	22000	2300	240	25	2.6	0.27	0.028	0.01	0.003	0.001	0.0004
ALD910025	2.50	$V_{GS} = V_{DS}$ (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.72	2.8	2.94	3.0	3.5
		$R_{DS(ON)}$ (MΩ)	21000	2200	230	24	2.5	0.26	0.027	0.01	0.003	0.001	0.0004
ALD910024	2.40	$V_{GS} = V_{DS}$ (V)	2.0	2.1	2.2	2.3	2.4	2.5	2.62	2.7	2.84	2.9	3.4
		$R_{DS(ON)}$ (MΩ)	20000	2100	220	23	2.4	0.25	0.026	0.009	0.003	0.001	0.0003
ALD910023	2.30	$V_{GS} = V_{DS}$ (V)	1.9	2.0	2.1	2.2	2.3	2.4	2.52	2.6	2.74	2.8	3.3
		$R_{DS(ON)}$ (MΩ)	19000	2000	210	22	2.3	0.24	0.025	0.009	0.003	0.001	0.0003

ALD Part Number	Gate-Threshold Voltage V_t (V)	Drain-Gate Source Voltage (V)[2] Equivalent ON Resistance (MΩ)	SAB MOSFET DRAIN-SOURCE ON CURRENT $I_{DS(ON)}$ (μA)[1] T_A = 25°C										
			0.0001	0.001	0.01	0.1	1	10	100	300	1000	3000	10000
ALD810028	2.80	$V_{GS} = V_{DS}$ (V)	2.4	2.5	2.6	2.7	2.8	2.9	3.04	3.14	3.32	3.62	4.22
		$R_{DS(ON)}$ (MΩ)	24000	2500	260	27	2.8	0.29	0.030	0.01	0.003	0.001	0.0004
ALD810027	2.70	$V_{GS} = V_{DS}$ (V)	2.3	2.4	2.5	2.6	2.7	2.8	2.94	3.04	3.22	3.52	4.12
		$R_{DS(ON)}$ (MΩ)	23000	2400	250	26	2.7	0.28	0.029	0.01	0.003	0.001	0.0004
ALD810026	2.60	$V_{GS} = V_{DS}$ (V)	2.2	2.3	2.4	2.5	2.6	2.7	2.84	2.94	3.12	3.42	4.02
		$R_{DS(ON)}$ (MΩ)	22000	2300	240	25	2.6	0.27	0.028	0.01	0.003	0.001	0.0004
ALD810025	2.50	$V_{GS} = V_{DS}$ (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.74	2.84	3.02	3.32	3.92
		$R_{DS(ON)}$ (MΩ)	21000	2200	230	24	2.5	0.26	0.027	0.01	0.003	0.001	0.0004
ALD810024	2.40	$V_{GS} = V_{DS}$ (V)	2.0	2.1	2.2	2.3	2.4	2.5	2.64	2.74	2.92	3.22	3.82
		$R_{DS(ON)}$ (MΩ)	20000	2100	220	23	2.4	0.25	0.026	0.009	0.003	0.001	0.0004
ALD810023	2.30	$V_{GS} = V_{DS}$ (V)	1.9	2.0	2.1	2.2	2.3	2.4	2.54	2.64	2.82	3.12	3.72
		$R_{DS(ON)}$ (MΩ)	19000	2000	210	22	2.3	0.24	0.025	0.009	0.003	0.001	0.0004

Selection of a SAB MOSFET device depends on a set of desired voltage vs. current characteristics that closely match the selected nominal bias voltage and bias currents that provide the best leakage and regulation profile of a supercap load. The V_t table, where Drain-Gate Source Voltage ($V_{GS} = V_{DS}$) gives a range of $V_{GS} = V_{DS}$ bias voltages as different $V_{supercap}$ load voltages. At each $V_{GS} = V_{DS}$ bias voltage, a corresponding Drain-Source ON Current ($I_{DS(ON)}$) is produced by a specific SAB MOSFET, which can be viewed as the amount of current available to compensate for supercap leakage current imbalances and results in an Equivalent ON Resistance ($R_{DS(ON)}$)across a supercap cell. Selection of a supercap bias voltage with a SAB MOSFET $I_{DS(ON)}$ that corresponds to the maximum supercap leakage current would result in the best possible tradeoff between leakage current balancing and voltage regulation.

Notes: 1) The SAB MOSFET Drain Source ON Current ($I_{DS(ON)}$) is the maximum current available to offset the supercapacitor leakage current.

2) The Drain-Gate Source Voltage (V_{GS}=V_{DS}) is normally the same as the voltage across the supercapacitor.

GENERAL DESCRIPTION (cont.)

SUPERCAPS

Supercaps are typically rated with a nominal recommended working voltage established for long life at their maximum rated operating temperature. Excessive supercap voltages that exceed its rated voltage for a prolonged time period will result in reduced lifetime and eventual rupture and catastrophic failure. To prevent such an occurrence, a means of automatically adjusting (charge-balancing) and monitoring the maximum voltage is required in most applications having two or more supercaps connected in series, due to their different internal leakage currents that vary from one supercap to another.

The supercap leakage current itself is a variable function of its many parameters such as aging, initial leakage current at zero input voltage, the material and construction of the supercap. Its leakage is also a function of the charging voltage, the charging current, operating temperature range and the rate of change of many of these parameters. Supercap balancing must accommodate these changing conditions.

SUPERCAP CHARGING AND DISCHARGING

During supercap charging, consideration must be paid to limit the rate of supercap charging so that excessive voltage and current do not build up across any two pins of the SAB MOSFETs, even momentarily, to exceed their absolute maximum rating. In most cases though, this is not an issue, as there may be other design constraints elsewhere in the circuit to limit the rate of charging or discharging the supercaps. For many types of applications, no further action, other than checking the voltage and current excursions, or including a simple current-limiting charging resistor, is necessary.

CHARACTERISTICS OF SUPERCAP AUTO BALANCING (SAB™) MOSFETS

The principle behind the Supercap Auto Balancing MOSFET in balancing supercaps is basically simple. It is based on the natural threshold characteristics of a MOSFET device. The threshold voltage of a MOSFET is the voltage at which a MOSFET turns on and starts to conduct a current. The drain current of the MOSFET, at or below its threshold voltage, is an exponentially non-linear function of its gate voltage. Hence, for small changes in the MOSFET's gate voltage, its on-current can vary greatly, by orders of magnitude. ALD's SAB MOSFETs are designed to take advantage of this fundamental device characteristic.

SAB MOSFETs can be connected in parallel or in a series, to suit the desired leakage current characteristics, in order to charge-balance an array of supercaps. The combined SAB MOSFET and supercap array is designed to be self-regulating with various supercap array leakage mismatches and environmental temperature changes. The SAB MOSFETs can also be used only in the subthreshold mode, meaning the SAB MOSFET is used entirely at min., nominal and max. operating voltages in voltage ranges below its specified threshold voltage.

For the ALD8100xx/ALD9100xx family of SAB MOSFETs, the threshold voltage V_t of a SAB MOSFET is defined as its drain-gate source voltage at a drain-source ON current, $I_{DS(ON)} = 1\mu A$ when its gate and drain terminals are connected together ($V_{GS} = V_{DS}$). This voltage is specified as xx, where the threshold voltage is in 0.10V increments. For example, the ALD810025 features a 2.50V threshold voltage MOSFET with drain-gate source voltage, $V_t = 2.50V$, and $I_{DS(ON)} = 1\mu A$. The SAB MOSFET has a precision trimmed threshold voltage where the tolerance of the threshold voltage is very tight, typically 2.50V +/-0.005V. When a 2.50V drain-gate source voltage bias is applied across an ALD810025/ ALD910025 SAB MOSFET, it conducts an $I_{DS(ON)} = 1\mu A$.

As all ALD8100xx and ALD9100xx devices operate the same way, an ALD810025 is used in the following illustration. At voltages below its threshold voltage, the ALD810025 rapidly turns off at a rate of approximately one decade of current per 104mV of voltage drop. Hence, at $V_{GS} = V_{DS} = 2.396V$, the ALD810025 has drain current of $0.1\mu A$. At $V_{GS} = V_{DS} = 2.292V$, the ALD810025 drain current becomes $0.01\mu A$. At $V_{GS} = V_{DS} = 2.188V$, the drain current is $0.001\mu A$. It is apparent that at $V_{GS} = V_{DS} \leq 2.10V$, the drain leakage current $\leq 0.00014\mu A$, which is essentially zero when compared to $1\mu A$ initial threshold current. When individual $V_{GS} = V_{DS}$ voltages fall below 1.9V, the SAB MOSFET leakage current essentially goes to zero (~70pA).

This exponential relationship between the Drain-Gate Source Voltage and the Drain-Source ON Current is an important consideration for replacing certain supercap charge balancing applications currently using fixed resistor or operational amplifier charge balancing. These other conventional charge-balancing circuits would continue to dissipate a significant amount of current, even after the voltage across the supercaps had dropped, because the current dissipated is a linear function, rather than an exponential function, of the supercap voltage (I = V/R). For supercap stacks consisting of more than two supercaps, the challenge of supercap balancing becomes more onerous.

For other IC circuits that offer charge balancing, active power is still being consumed even if the supercap voltage falls below 2.0V. For a four-cell supercap stack, this translates into a 2.0V x 4 ~= 8.0V power supply for an IC charge-balancing circuit. Even a two-cell supercap stack would be operating such an IC circuit with 2.0V x 2 = 4V. A supercap stack with SAB MOSFET charge-balancing, on the other hand, would be the only way to lose exponentially decreasing amount of charge with time and preserve by far the greatest amount of charge on each of the supercaps, by not adding charge loss to the leakages contributed by the supercaps themselves.

At $V_{GS} = V_{DS}$ voltages of the ALD810025 above its V_t threshold voltage, its drain current behavior has the opposite near-exponential effect. At $V_{GS} = V_{DS} = 2.60V$, for example, the ALD810025 $I_{DS(ON)}$ increases tenfold to $10\mu A$. Similarly, $I_{DS(ON)}$ becomes $100\mu A$ for a $V_{GS} = V_{DS}$ voltage increase to 2.74V, and $300\mu A$ at 2.84V. (See Table 1)

As $I_{DS(ON)}$ changes rapidly with applied voltage on the Drain-Gate to Source pins, the SAB MOSFET device acts like a voltage limiting regulator with self-adjusting current levels. When this SAB MOSFET is connected across a supercap cell, the total leakage current across the supercap is compensated and corrected by the SAB MOSFET.

Consider the case when two supercap cells are connected in series, each with a SAB MOSFET connected across it in the V_t mode ($V_{DS} = V_{GS}$), charged by a power supply to a voltage equal to 2 x V_S.

If the top supercap has a higher internal leakage current than the bottom supercap, the voltage $V_{S(top)}$ across it tends to drop lower than that of the bottom supercap. The SAB MOSFET $I_{DS(ON)}$ across the top supercap, sensing this voltage drop, drops off rapidly. Meanwhile, the bottom supercap $V_{S(bottom)}$ voltage tends to rise, as $V_{S(bottom)} = (2 \times V_S) - V_{S(top)}$. This tendency for the voltage rise also increases $V_{GS} = V_{DS}$ voltage of the SAB MOSFET across the bottom supercap. This increased $V_{GS} = V_{DS}$ voltage would cause the $I_{DS(ON)}$ current of the bottom SAB MOSFET to increase rapidly as well. The excess leakage current of the top supercap would now leak across the bottom SAB MOSFET, reducing the voltage rise tendency of the lower supercap. With this self-regulating mechanism, the top supercap, $V_{S(top)}$, voltage tends to rise while the bottom supercap, $V_{S(bottom)}$, voltage tends to drop, creating simultaneously opposing actions of the supercap leakage currents.

GENERAL DESCRIPTION (cont.)

With appropriate design and selection of a specific SAB MOSFET device for a given pair of supercaps, it is now possible to have regulation and balancing of two series-connected supercaps, at essentially no extra leakage current, since the SAB MOSFET only conducts the difference in leakage current between the two supercaps.

Likewise, the case of the bottom supercap having a higher leakage current than that of the top supercap works in similar fashion, with the tendency of the bottom supercap, $V_{S(bottom)}$, voltage to drop, compensated by the tendency of the top supercap, $V_{S(top)}$, voltage to drop as well, effected by the top SAB MOSFET. This SAB MOSFET charge balancing scheme also extends to up to four supercaps in a series network by using four SAB MOSFETs in a single ALD8100xx SAB MOSFET package.

As ambient temperature increases, the supercap leakage current, as a function of temperature, increases. The SAB MOSFET threshold voltage is reduced with temperature increase, which causes the drain current to increase with temperature as well. This drain current increase compensates for the leakage current increase within the supercap, reducing the overall supercap temperature leakage effect and preserving charge balancing effectiveness. This temperature compensation assumes that all the supercaps and the SAB MOSFETs are in the same temperature environments.

Each drain pin of a SAB MOSFET has an internal reverse biased diode to its source pin, which can become forward biased if the drain voltage should become negative relative to its source pin. This forward-biased diode clamps the drain voltage to limit the negative voltage relative to its source voltage, and is limited to 80mA max. rated current between any two pins.

SPECIFYING SAB™ MOSFETS

The process of selecting SAB MOSFETs begins by analyzing the parameters and the requirements of a given selection of supercaps:

1) For better leakage current matching results, pick the same make and model of supercaps to be connected in a series. If possible, select supercaps from the same production batch. (Note: SAB MOSFETs are precisely set at the factory and specified such that their lot-to-lot and MOSFET-to-MOSFET variation is not a concern.)

2) Determine the leakage current range of the supercaps.

3) Determine the desired nominal operating voltage of the supercaps.

4) Determine the maximum operating voltage rating of the supercaps.

5) Calculate or measure the maximum leakage current of the supercap at the maximum rated operating voltage.

6) Determine the operating temperature range of the supercaps.

7) Determine any additional level of operating leakage current in the system.

Next, determine the normalized drain current of a SAB MOSFET at a pre-selected operating voltage. For example, the ALD810025 has a rated leakage, or drain, current of 1μA at applied drain-gate source voltage of 2.50V. If the desired normalized drain current is 0.01μA, then the ALD810025 would give a bias drain-gate source voltage of approximately 2.3V at that current, which produces an equivalent ON resistance of 2.3V/0.01μA ~= 230MΩ (using the rule of thumb of one decade of current change per 0.10V of $V_{GS} = V_{DS}$ change).

A DESIGN EXAMPLE

A single 5V power supply using two 2.7V rated supercaps connected in a series and a single SAB MOSFET array package.

For a supercap with:

1) max. operating voltage = 2.70V and
2) max. leakage current = 10μA at 70°C.
3) At 2.50V, the supercap max. leakage current = 2.5μA at 25°C.

Next, pick ALD810026, a SAB MOSFET with V_t = 2.60V. For this device, at $V_{GS} = V_{DS}$ = 2.60V, the nominal $I_{DS(ON)}$ = 1μA. Per the leakage current table, at $V_{GS} = V_{DS}$ = 2.50V, $I_{DS(ON)}$ ~= 0.1μA.

At a nominal operating voltage of 2.50V, the additional leakage current contribution by the ALD810026 is therefore 0.1μA. The total current for the supercap and the SAB MOSFET = 2.5μA + 0.1μA ~= 2.6μA @ 2.50V operating voltage. At an operating voltage of 2.40V, the additional ALD810026 leakage current decreases to about 0.01μA.

At a max. voltage of 2.70V across the ALD810026 SAB MOSFET, $V_{GS} = V_{DS}$ = 2.70V results in $I_{DS(ON)}$ = 10μA. 10μA is also the max. leakage current margin, the difference between top and bottom supercap leakage currents that can be compensated.

If a higher max. leakage current margin is desired for an application, then the selection may need to go to the next SAB MOSFET down in the series, ALD810025. For an ALD810025 operating at a max. rated voltage of 2.70V, the max. leakage current margin is ~= 50μA. For this device, the nominal operating current at 2.50V is ~= 1μA, which is the average current consumption for the series-connected stack. The total current for the supercap and the SAB MOSFET is = 2.5μA + 1μA ~= 3.5μA @ 2.50V operating voltage.

Because the SAB MOSFET is always active and always in “on” mode, there is no circuit switching or sleep mode involved. This may become an important factor when the time interval between the supercap discharging or recharging, and other events happening in the application, is long, unknown or variable.

In real life situations, the actual circuit behavior is a little different, further reducing overall leakage currents from both supercaps and SAB MOSFETs, due to the automatic compensation for different leakage current levels by both the supercaps themselves and in combination with the SAB MOSFETs. Take the above example of two supercaps in series, assuming that the top supercap is leaking 10μA and the bottom one leaking 4μA (both at the rated 2.7V max.) while the power supply remains at 5V DC. The actual voltage across the top supercap tends to be less than 50% of 5.0V, due to its internal leakage current, and results in a lowered current level because the voltage across it tends to be lower as well. The total voltage across both supercaps is still 5.0V, so each supercap would experience a lowered voltage at less than maximum rated voltage of 2.7V, thereby resulting in reduced overall leakage currents in each of the two supercaps.

These leakage currents are then further regulated by the SAB MOSFETs connected across each of the supercaps. The end result is a compensated condition where the top supercap has ~2.4V and the bottom cap has a voltage of ~2.6V. The excess leakage current of the top supercap is bypassed across the bottom SAB MOSFET, so that there is little or no net additional leakage current introduced by the bottom SAB MOSFET. Meanwhile the top SAB MOSFET, with ~2.4V across it, is biased to conduct (or leak) very little drain current. Note also that the top supercap is now biased at ~2.4V and, therefore, would experience less current leakage than

when it is at 2.7V. The primary benefit here is that this process of leakage balancing is fully automatic and works for a variety of supercaps, each with a different leakage characteristic profile of its own.

A second benefit to note is that with ~2.4V and ~2.6V across the two supercaps, in this example, the actual current level difference between the top and the bottom SAB MOSFETs is at about a 100:1 ratio (~2 orders of magnitude). The net additional leakage current contributed by the ALD8110026 in the design example above would, therefore, be approximately 0.01μA. In this case, the difference in leakage currents between the two supercaps can have a ratio of 100:1 and could still have charge balancing and voltage regulation.

The dynamic response of a SAB MOSFET circuit is very fast, and the typical response time is determined by the R C time constant of the equivalent ON resistance value of the SAB MOSFET and the capacitance value of the supercap. In many cases the R value is small initially, responding rapidly to a large voltage transient by having a smaller R C time constant. As the voltages settle down, the equivalent R increases. As these R and C values can become very large, it can take a long time for the voltages across the supercaps to settle down to steady state leakage current levels. The direction of the voltage movements across the supercap, however, would indicate the trend that the supercap voltages are moving away from the voltage limits.

PARALLEL-CONNECTED AND SERIES-CONNECTED SAB MOSFETS

In the previous design example, note that the ALD810026 is a quad pack, with four SAB MOSFETs in a single SOIC package. For a standard configuration of two supercaps connected in series, the ALD9100xx dual SAB MOSFET is recommended for charge balancing. If a two-stack supercap requires charge balancing, then there is also an option to parallel-connect two SAB MOSFETs of a quad ALD8100xx for each of the two supercaps. Parallel-connection generally means that the drain, gate and source terminals of each of two SAB MOSFETs are connected together to form a MOSFET with a single drain, a single gate and a single source terminal with twice the output currents. In this case, at a nominal operating voltage of 2.50V, the additional leakage current contribution by the SAB MOSFET is equal to 2 x 0.1μA = 0.2μA. The total current for the supercaps and the SB MOSFET is = 2.5μA + 0.2μA ~= 2.7μA @ 2.50V operating voltage. At max. voltage of 2.70V across the SAB MOSFET, V_{GS} = V_{DS} = 2.70V results in a drain current of 2 x 10μA = 20μA. So this configuration would be chosen to increase max. charge balancing leakage current at 2.70V to 20μA, at the expense of an additional 0.1μA leakage at 2.50V.

This method also extends to four supercaps in series, although this may require two separate ALD810026 packages, if the maximum voltage ratings of the SAB MOSFET are exceeded.

For stacks of series-connected supercaps consisting of more than three or four supercaps, it is possible to use a single SAB MOSFET array for every three or four supercap stacks connected in series. Multiple SAB MOSFET arrays can be arrayed across multiple supercap stacks to operate at higher operating voltages. It is important to limit the voltage across any two pins within a single SAB MOSFET array package to be less than its absolute maximum voltage and current ratings.

ENERGY HARVESTING APPLICATIONS

Supercaps offer an important benefit for energy harvesting applications from a low energy source, buffering and storing such energy to drive a higher power load.

For energy harvesting applications, supercap leakage currents are a critical factor, as the average energy harvesting input charge must exceed the average supercap internal leakage currents in order for any net energy to be harvested and saved. Often times the input energy is variable, meaning that its input voltage and current magnitude is not constant and may be dependent upon a whole set of other parameters such as the source energy availability, energy sensor conversion efficiency, etc.

For these types of applications, it is essential to pick supercaps with low leakage specifications and to use SAB MOSFETs that minimize the amount of energy loss due to leakage currents.

For up to 90% of the initial voltages of a supercap used in energy harvesting applications, supercap charge loss is lower than its maximum leakage rating, at less than its max. rated voltage. SAB MOSFETs used for charge balancing, due to their high input threshold voltages, would be completely turned off, consuming zero drain current while the supercap is being charged, maximizing any energy harvesting gathering efforts. The SAB MOSFET would not become active until the supercap is already charged to over 90% of its max. rated voltage. The trickle charging of supercaps with energy harvesting techniques tends to work well with SAB MOSFETs as charge balancing devices, as it is less likely to have high transient energy spurts resulting in excessive voltage or current excursions.

If an energy harvesting source only provides a few μA of current, the power budget does not allow wasting any of this current on capacitor leakage currents and power dissipation of resistor or operational amplifier based charge-balancing circuits. It may also be important to reduce long term leakage currents, as energy harvesting charging at low levels may take up to many days.

In summary, in order for an energy harvesting application to be successful, the input energy harvested must exceed all the energy required due to the leakages of the supercaps and the charge-balancing circuits, plus any load requirements. With their unique balancing characteristics and near-zero charge loss, SAB MOSFETs are ideal devices for use in supercap charge-balancing in energy harvesting applications.

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD810023 Min	ALD810023 Typ	ALD810023 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.28	2.30	2.32	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 19000		μA MΩ	V_{GS} =V_{DS} =1.90V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2000		μA MΩ	V_{GS} =V_{DS} =2.00V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 210		μA MΩ	V_{GS} =V_{DS} =2.10V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 22		μA MΩ	V_{GS} =V_{DS} =2.20V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.3		μA MΩ	V_{GS} =V_{DS} =2.30V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.24		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.025		μA MΩ	V_{GS} =V_{DS} =2.54V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.009		μA MΩ	V_{GS} =V_{DS} =2.64V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =2.82V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.12V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =3.72V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD810024 Min	ALD810024 Typ	ALD810024 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.38	2.40	2.42	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 20000		μA MΩ	V_{GS} =V_{DS} =2.00V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2100		μA MΩ	V_{GS} =V_{DS} =2.10V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 220		μA MΩ	V_{GS} =V_{DS} =2.20V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 23		μA MΩ	V_{GS} =V_{DS} =2.30V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.4		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.25		μA MΩ	V_{GS} =V_{DS} =2.50V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.026		μA MΩ	V_{GS} =V_{DS} =2.64V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.009		μA MΩ	V_{GS} =V_{DS} =2.74V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =2.92V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.22V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =3.82V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD810025 Min	ALD810025 Typ	ALD810025 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.48	2.50	2.52	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 21000		μA MΩ	V_{GS} =V_{DS} =2.10V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2200		μA MΩ	V_{GS} =V_{DS} =2.20V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 230		μA MΩ	V_{GS} =V_{DS} =2.30V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 24		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.5		μA MΩ	V_{GS} =V_{DS} =2.50V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.26		μA MΩ	V_{GS} =V_{DS} =2.60V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.027		μA MΩ	V_{GS} =V_{DS} =2.74V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.01		μA MΩ	V_{GS} =V_{DS} =2.84V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =3.02V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.32V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =3.92V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V V- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD810026 Min	ALD810026 Typ	ALD810026 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.58	2.60	2.62	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 22000		μA MΩ	V_{GS} =V_{DS} =2.20V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2300		μA MΩ	V_{GS} =V_{DS} =2.30V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 240		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 25		μA MΩ	V_{GS} =V_{DS} =2.50V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.6		μA MΩ	V_{GS} =V_{DS} =2.60V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.27		μA MΩ	V_{GS} =V_{DS} =2.70V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.028		μA MΩ	V_{GS} =V_{DS} =2.84V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.01		μA MΩ	V_{GS} =V_{DS} =2.94V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =3.12V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.42V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =4.02V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD810027 Min	ALD810027 Typ	ALD810027 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.68	2.70	2.72	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 23000		μA MΩ	V_{GS} =V_{DS} =2.30V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2400		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 250		μA MΩ	V_{GS} =V_{DS} =2.50V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 26		μA MΩ	V_{GS} =V_{DS} =2.60V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.7		μA MΩ	V_{GS} =V_{DS} =2.70V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.28		μA MΩ	V_{GS} =V_{DS} =2.80V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.029		μA MΩ	V_{GS} =V_{DS} =2.94V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.01		μA MΩ	V_{GS} =V_{DS} =3.04V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =3.22V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.52V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =4.12V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage ——— 15.0V
Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

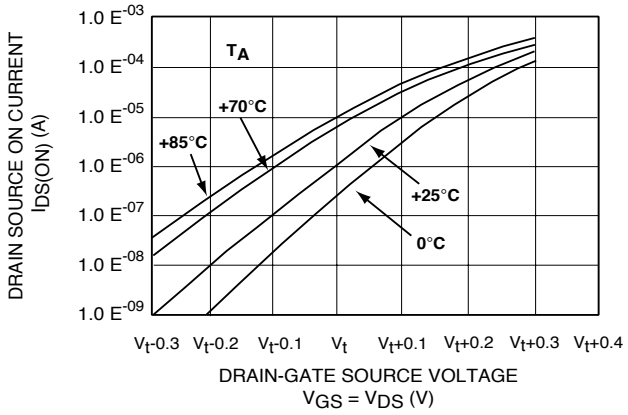
OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

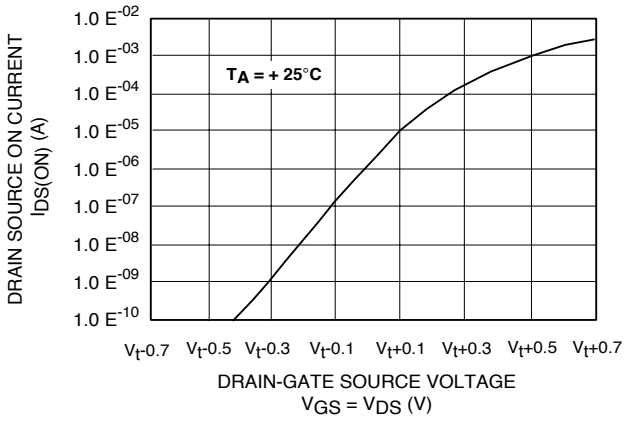
Parameter	Symbol	ALD810028 Min	ALD810028 Typ	ALD810028 Max	Unit	Test Conditions
Gate Threshold Voltage	V_t	2.78	2.80	2.82	V	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Offset Voltage	V_{OS}		5	20	mV	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Offset Voltage Tempco	TC_{VOS}		5		μV/C	V_{t1} - V_{t2} or V_{t3} - V_{t4}
Gate Threshold Voltage Tempco	TC_{Vt}		-2.2		mV/C	V_{GS} =V_{DS}; $I_{DS(ON)}$ =1μA
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.0001 24000		μA MΩ	V_{GS} =V_{DS} =2.40V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.001 2500		μA MΩ	V_{GS} =V_{DS} =2.50V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.01 260		μA MΩ	V_{GS} =V_{DS} =2.60V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		0.1 27		μA MΩ	V_{GS} =V_{DS} =2.70V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1 2.8		μA MΩ	V_{GS} =V_{DS} =2.80V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10 0.29		μA MΩ	V_{GS} =V_{DS} =2.90V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		100 0.030		μA MΩ	V_{GS} =V_{DS} =3.04V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		300 0.01		μA MΩ	V_{GS} =V_{DS} =3.14V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		1000 0.003		μA MΩ	V_{GS} =V_{DS} =3.32V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		3000 0.001		μA MΩ	V_{GS} =V_{DS} =3.62V
Drain Source On Current Drain Source On Resistance	$I_{DS(ON)}$ $R_{DS(ON)}$		10000 0.0004		μA MΩ	V_{GS} =V_{DS} =4.22V
Drain Source Breakdown Voltage	BV_{DSX}	10.6			V	
Drain Source Leakage Current[1]	$I_{DS (OFF)}$		10	400 4	pA nA	V_{GS} =V_{DS} =V_t - 1.0 V_{GS} =V_{DS} =V_t - 1.0, T_A = +125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1	pA nA	V_{GS} =5.0V, V_{DS} =0V V_{GS} =5.0V, V_{DS} =0V, T_A = +125°C
Input Capacitance	C_{ISS}		15		pF	V_{GS} =0V, V_{DS} =5.0V
Turn-on Delay Time	t_{on}		10		ns	
Turn-off Delay Time	t_{off}		10		ns	
Crosstalk			60		dB	f = 100KHz

TYPICAL PERFORMANCE CHARACTERISTICS

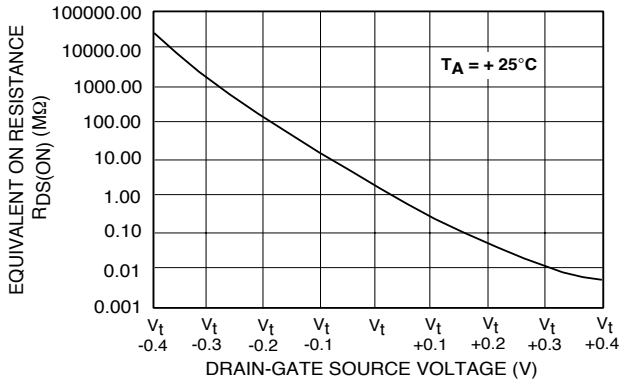
DRAIN-GATE SOURCE VOLTAGE vs. DRAIN SOURCE ON CURRENT



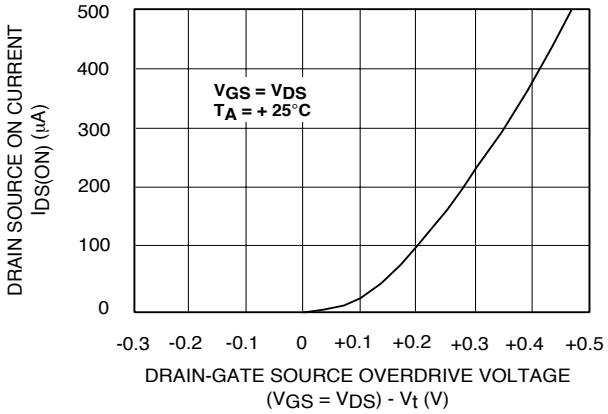
DRAIN-GATE SOURCE VOLTAGE vs. DRAIN SOURCE ON CURRENT



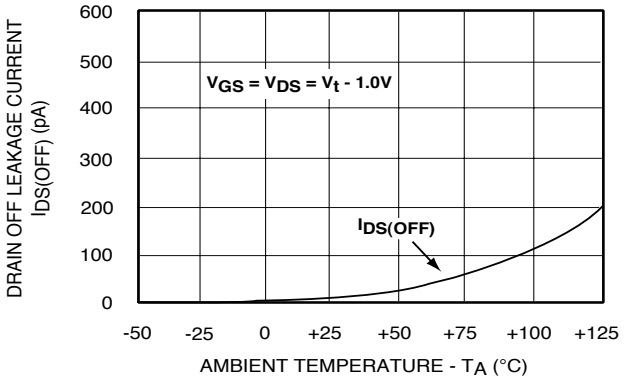
EQUIVALENT ON RESISTANCE vs. DRAIN-GATE SOURCE VOLTAGE



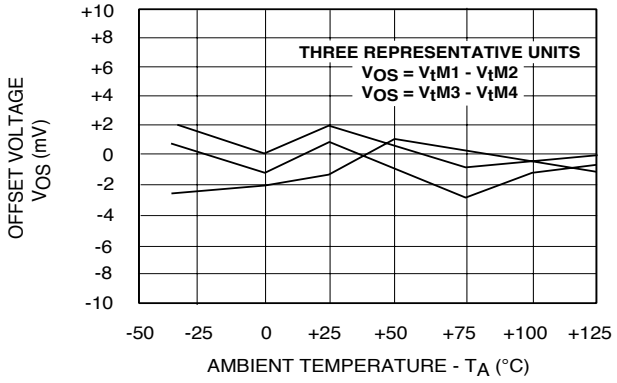
FORWARD TRANSFER CHARACTERISTICS LOW VOLTAGE



DRAIN OFF LEAKAGE CURRENT $I_{DS(OFF)}$ vs. AMBIENT TEMPERATURE

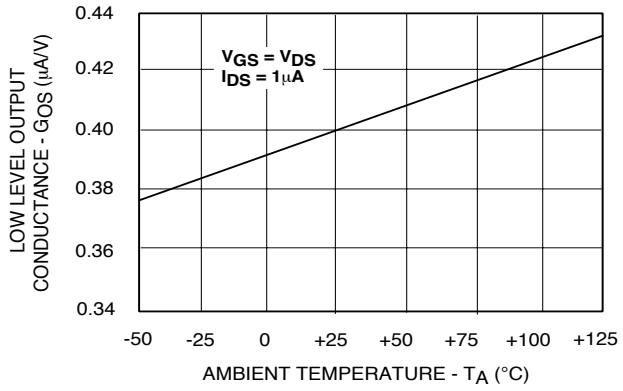


OFFSET VOLTAGE vs. AMBIENT TEMPERATURE

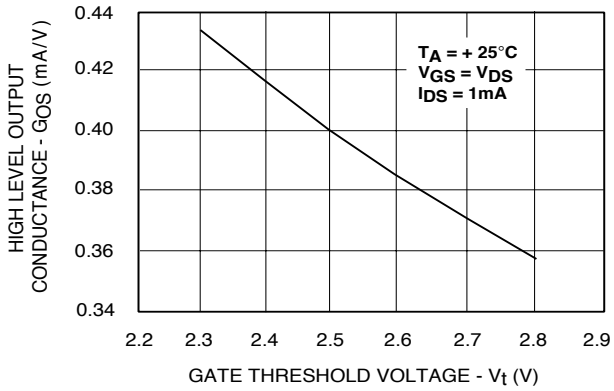


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

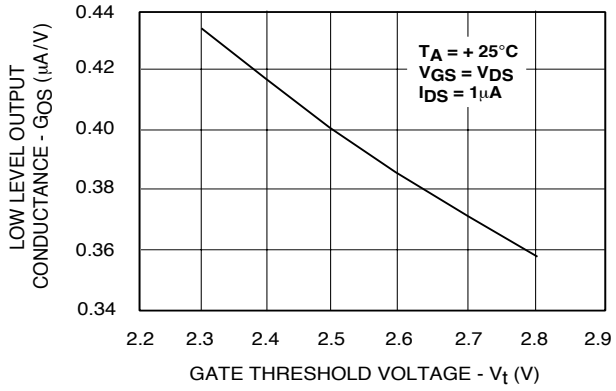
LOW LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



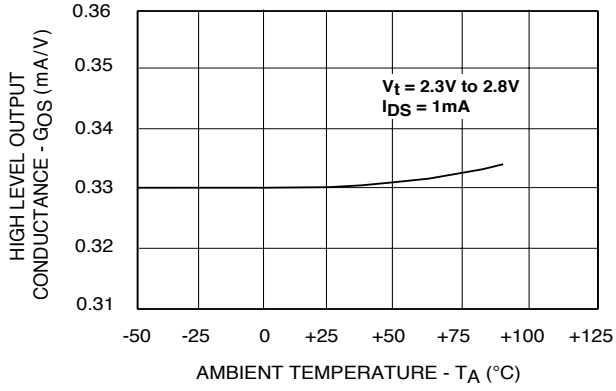
HIGH LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE



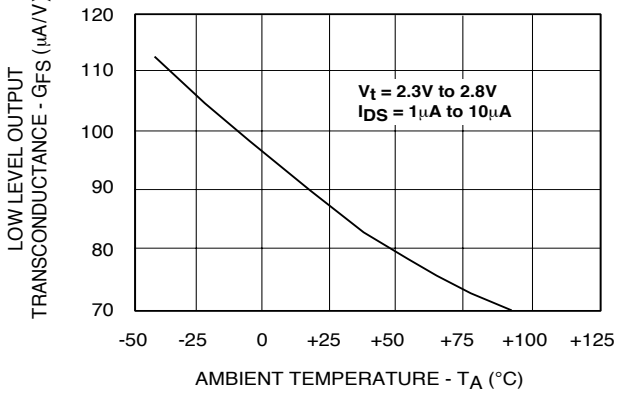
LOW LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE



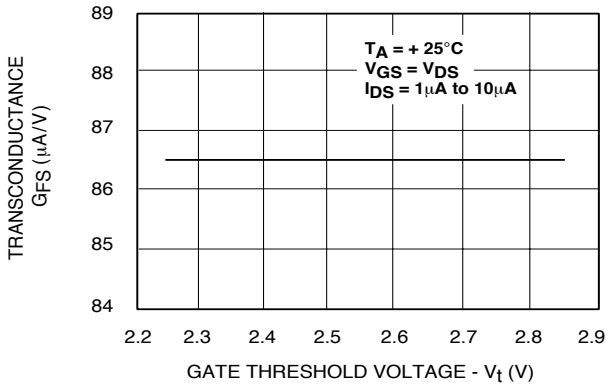
HIGH LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



LOW LEVEL OUTPUT TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE

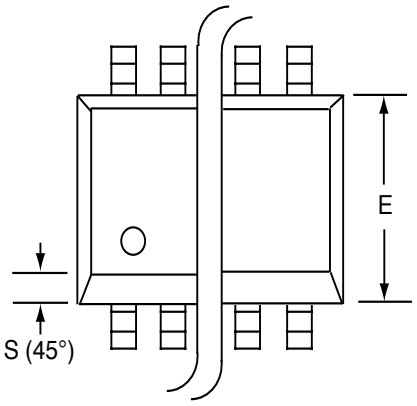


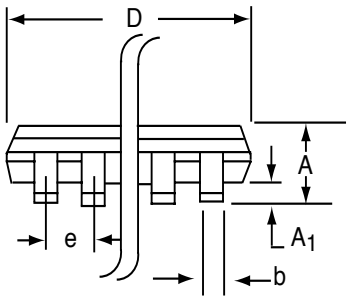
TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE

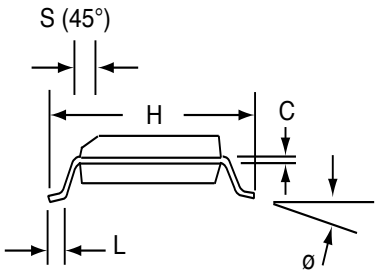


SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-16	9.80	10.00	0.385	0.394
E	3.50	4.05	0.140	0.160
e	1.27 BSC		□0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

□

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